Design Consideration of An Multimode, Power-controllable Transmitter for UHF Mobile RFID Reader

Gao Tongqiang
Department of Electronic Engineering
Tsinghua University
Beijing, China
gtq03@mails.tsinghua.edu.cn

Institute of Microelectronics
Tsinghua University
Beijing, China

Abstract—Aiming at the expansive application of RFID technology, design considerations are expatiated to a highly-integrated, multimode, power-controllable transmitter in mobile UHF RFID reader with CMOS process. The transmitter consists of digital section, a baseband circuit, an up-conversion mixer and a gain-variable power amplifier. Multiple data modes can be generated. The direct-conversion RF section is proposed to minimize the off-chip components and provide a low-cost, highly efficient solution. The RF power amplifier can achieve a maximum output power of 26dBm and maintain a power-added efficiency (PAE) higher than 40% over the 18dBm-26dBm output power range. Feasibility of the transmitter is validated by ADS simulator.

Keywords – CMOS, power amplifier, RFID, transmitter

I. INTRODUCTION

To be a kind of wireless communication technology, radio frequency identification application (RFID) has become indispensable as the worldwide RFID market has been growing tremendously. Potential applications of RFID are currently driving hardware developers to merge RFID readers into mobile devices such as PDAs and cell phones, which will enable individual customers to acquire product information through their own RFID readers [1], [2].

In general, mobile device has inherent problems such as battery, output power and tx-rx isolation. In the integrated-circuit (IC) design field, CMOS-based solutions are very competitive in power consumption and large scale integration, but it is placed at a disadvantageous position in output power and isolation. Great efforts are directed to develop a fully-integrated CMOS single-chip solution for an RFID system. Although a great deal of success comes forth on the integration of RFID tags with CMOS process [3], there is still fewer CMOS-based RFID reader chip. It is a great challenge to fulfill a fully-integrated CMOS reader.

In a fully-integrated CMOS transceiver, one of the most difficult tasks is to implement a power amplifier (PA) with high output power, efficiency, and suitable linearity. The focus of this paper is to demonstrate techniques that would allow for a highly-integrated, multiple data mode CMOS transmitter for mobile RFID reader applications. Circuit design considerations are presented aiming at the specified protocol of EPC global Class 1 Generation 2 [4].

II. TRANSMITTER ARCHITECTURE

A typical mobile RFID system is comprised of reader, tags and communication system [5]. Communication between reader and tags is half duplex. A reader first sends a modulated wave to tags, if tag lies within the interrogation range of the reader. When the reader waits replies it must transmit the un-modulated carrier continuously in order to provide the power supply for tag operation. When the reader receives information from tags, it verifies errors, determines their validity, and sends them to computer for further process.

![Diagram of a typical RFID system.](image)

It is apparent that the reader transmits and receives signals at the same time with the same frequency. When the receiver works, proportions of transmitted carrier will be leaked into the received channel. The large leakage signal from transmitter due to the low isolation of circulator can reduce the sensitivity of the receiver, and even saturate the receiver components. So it is critical to cancel out the carrier leakage in the receiver frontend.

In the design of transmitter, the emitted signal should comply with the local frequency regulatory. Based on the given protocol [4], different data mode emitted from reader are ASK (DSB, SSB or PR-ASK) and continuous wave (CW).
The bandwidth of RF signal can be 200 kHz, 250 kHz, or 500 kHz. The main demands of linearity are the envelope of the RF signal and the transmitted signal spectrum.

A. Topology of Transmitter

When designing the transmitter of a single-chip transceiver, restrictions on unwanted emissions, and the trade-offs between the output power, efficiency, and the linearity directly impacts the choice of topology and each circuit block. Topology of the proposed transmitter is illustrated in Fig. 2. It consists of three parts: digital unit, baseband circuit (DAC, LPF), and RF section (mixer, PA).

The proposed architecture minimizes the number of the building blocks, leading to a high-efficient solution. The baseband section is chosen to be quadric I/Q-branches for the reason of SSB transmission and different modulation modes. A common direct up-conversion and RF amplification section is adopted to perform data modulation, up-conversion, and power amplification. The power-controllable architecture is introduced to provide high efficiency over a broad range of output power. The variation of output power is fulfilled by selecting the number of amplification units and the modulation of power supply.

III. GENERATION OF TRANSMITTED SIGNALS

In forward link, the data coding is in the PIE mode. All the transmitted signals are generated in DSP module. The transmission types can be chosen among SSB, DSB, PR-ASK and CW carrier by operation of the controller switches. The in-phase (I) and quadrature (Q) baseband digital signals pass through DAC and baseband filter before the signal is up-converted to RF domain. System level simulation is carried out using ADS2005A simulator.

Fig. 3 is a specific case to generate a PIE code with a symbol rate of 80kbps. For an ideal band-limited signal without intersymbol interference, Nyquist criterion should be satisfied. A raised cosine filter is introduced to suppress the off-band spectrum. The filter has an over-sample ratio of 32 and a time delay of 4 times of symbol time. To meet the stringent waveform bound of the modulated signal, roll-off factor of the filter is chosen as 1.

A Hilbert transformation is introduced to convert the input signal into an analytical signal using a phase splitter. SSB-AM signal is derived by removing one of the sideband of DSB-AM. The advantage of SSB-AM is it occupies half the bandwidth compared to DSB-AM to save the frequency resources. Its delay parameter is set to be 32.

PR-ASK signal is generated when data is input into a D-type trigger first. Then additional raised-cosine filter, DAC and filter are utilized to process the digital signal.

In baseband analog domain, DAC unit will convert digital signals into analog, which introduces an unavoidable quantization error. The low pass filter (LPF) after DAC is to smooth the waveform and suppress the high order harmonics.

IV. RF TRANSMITTER

Mixer and PA are the main modules in RF transmitter. They perform the functions of data modulation, up-conversion and power amplification.

A. Direct up-conversion Mixer

Fig. 4 shows the schematic of the differential active mixer. The mixer is realized as Gilbert cells with their outputs added in the current domain. The voltages of the differential I and Q input signals are converted to currents by the transconductors, M1-M4. These current signals are then added at points ‘a’ and ‘b’. The other transistors, M5-M12, act as switches driven by external differential LO signals. Two inductors, L1
and L2, along with the capacitors C1, C2, and the parasitic capacitors of transistors M5-M12, form the LC tank for the differential RF output. Inductor loads are used for high frequency output to increase the output voltage swing.

![Figure 4](image)

**Figure 4.** Direct-up-conversion mixer architecture.

The designed active mixer provides a conversion gain of 1.05 dB, IIP3 of 11.2 dBm, OIP3 of 5.7 dBm, and the single-side noise figure (SSB-NF) of 15.8 dB.

**B. Power-controllable Amplification**

To be the power boosting component in transmitter, PA is the largest power dissipation device in a wireless transceiver. The working life of a mobile system is mostly determined by PA’s efficiency. Also linearity of the transmitted signal is largely influenced by PA.

The proposed PA architecture is as shown in Fig. 5. The input differential RF signal is derived from mixer. The amplifier module includes two CMOS class-E PAs with different output power, each with a phase shifter before it. A class-S amplifier modulates the duty cycle of the pulse signal from DSP unit and then modulates the supply voltage for the amplifier module. The total output power can be provided by one amplifier individually or by two amplifiers simultaneously. In order to obtain the different output power regions, it must be able to switch between the different amplifiers and combine their output efficiently.

![Figure 5](image)

**Figure 5.** Power-controllable power amplifier.

C. **Class-E Power Amplifier**

Recent studies have demonstrated the viability of a linear CMOS PA in mobile RFID reader application, but its maximum efficiency is only 28% [6]. In order to obtain higher efficiency, two Class-E PAs with different output power are designed for its circuit simplicity and high frequency performance [7]. The implemented 2-stage PA is shown in Fig. 6. The 2 stages work at class AB and class E, respectively. Each stage provides a gain of about 10 dB.

In the output stage, a cascode structure is adopted to enhance the supply voltage and protect the transistors. The value of $V_{dd}$ is 2.5 V and $V_{dd}$ of 1.8 V. The $\lambda/4$ transmission line TL0, which is implemented with a microstrip line in printed circuit board, transforms the antenna resistance (50 Ω) into a lower value (13.5 Ω or 27 Ω), the equivalent resistance of the corresponding output stage. It is obvious that the phase delay of the two PAs is not equal. So a phase matching mechanism should be considered to implement the power combination.

![Figure 6](image)

**Figure 6.** Schematic of class-E PA.

The PA has been designed with UMC 0.18um CMOS process. From the simulated results of PAE versus input power shown, it can be seen that the two amplifiers can provide the output power of 23 dBm and 20 dBm individually with the PAE about 50%.

D. **Class-S Modulator and Drain Modulation**

The purpose of class-S modulator is to fulfill power control by varying the supply voltage for amplification unit. Usually a class-S amplifier consists of a Class D amplifier as an inverter and a low pass filter (LPF) [8]. By varying the duty cycle of pulse signal derived from DSP, a square wave is generated and applied to LPF, leading to a slowly varying or dc voltage appearing in the load.

The class-S modulator is designed to drive a 7 ohm load, representative of the impedance seen from the drain of class-E PA. Based on the process parameters the width of PMOS transistors was selected to be about 3 times that of NMOS transistors. The LPF is realized with off-chip components and its -3dB frequency is about 2 MHz.

E. **Phase Shifter**

Cascades of N segments of low-pass filters in a π-configuration can be used to replace a transmission line with quarter wavelength ($\pi/4$) at frequency $f_c$ and characteristic
impedance $Z_0$ by using inductors and capacitances with values as follows [9]-[11]:

$$L = \frac{Z_0}{N \cdot 2\pi f_c}$$

(1)

and

$$C = \frac{1}{N \cdot 2\pi f_c Z_0}.$$

(2)

The transmission phase of the filter can be controlled by varying the capacitance $C$, using varactors with a variable capacitance value from $C_{\text{max}}$ up to $C_{\text{min}}$. Thus, realizing the LC components using on-chip inductors and varactors, makes it possible to vary the phase of the RF signal by changing the value of $C$ using a control voltage $V_{\text{PS}}$ as shown in Fig. 7.

Figure 7. Architecture of the phase shifter.

In this work, the phase shifter is comprised of 4 segments LPFs in $\pi$-configuration to emulate a $\lambda/2$ filter. It is designed in a 0.18um CMOS technology operating at the frequency $f_c=915$MHz and the characteristic impedance $Z_0=50$ $\Omega$. Varactors are realized using N+/N-well MIS varactors with the drain-bulk-source terminals tied together and acting as the cathode and the gate terminal acting as the anode. The cathode in the phase shifter is tied to ground and the anode is tied to the control voltage.

The values of L and C in phase shifter are 4.34nH and 1.72pF respectively. By changing the control voltage $V_{\text{PS}}$, the capacitance of varactors varies between two extremes $C_{\text{max}}$ and $C_{\text{min}}$, resulting in the different phase delay of the RF signals. The designed phase shifter can provides a phase shift from $110^\circ$ up to $220^\circ$.

F. Power Control

Fig. 8 shows a simplified scheme of the amplification architecture. Switched cascode transistors as well as the series resonating circuit L2-C2 are used as low impedance sources, driving the corresponding load impedance through $\lambda/4$ transmission line. Each amplifier can be turned off without interfering the other one, as long as sufficient low output impedance is maintained by the off amplifier. This problem is overcome by introducing a PMOS switch that pulls the output of the non-amplifying branch to the positive supply rail [12].

The function of PMOS transistor is as follows. When the branch amplifier is in amplification mode, the gate of the corresponding PMOS transistor is tied to $V_d\bar{d}$. The parasitic capacitance introduced by this PMOS transistor is absorbed into the capacitance at the output node. The total capacitance at the node is resonated out by the drain inductive load of the amplifier. When the amplifier is in non-amplifying mode, PMOS transistor is turned on by tying its gate to ground. Thus, high impedance is maintained at the output terminal of the corresponding $\lambda/4$ transmission line. Meanwhile, the gate of the PA transistor is tied to ground to decrease the power dissipation of the off-mode amplifier, leading to a higher PAE.

Figure 8. Implemented power amplification unit.

In order to hold the phase match of two paths, phase shifter is added before each PA. Only one phase shifter is controlled by the adjustable voltage $V_{\text{PS}}$, and the other keeps constant. Power adjustment is implemented by combining the output of the class-E PAs through $\lambda/4$ lines and varying the supply voltage of PAs. The larger output power variation is determined by the digital control signal $b_0/b_1$ from DSP unit. The little adjustment is accomplished by changing the supply voltage of PAs by the introduction of class-S modulator.

The measured curve of PAE versus output power is shown in Fig. 9. The circle-line shows the desired efficiency of the proposed structure at the various output power level. The dashed lines show the simulation results of different PAs without modulation. Simulation shows the amplification unit can provides a maximum output power of 26dBm. The circuit can maintains a maximum PAE of 47.9% and maintains PAE higher than 41% for the output power range of 18dBm-26dBm.

Figure 9. PAE versus output power of the amplification module.
V. SIMULATION RESULTS

The RF transmitter including mixer and PAs has been implemented in 0.18um 1P6M CMOS process. Based on the protocol of EPC global Class-1 Gen-2, behavior-level simulation of overall transmitter includes DSP and RF section is tested. Fig. 10 shows the normal envelope of the output signal and the spectrum of the transmitted DSB signal. Simulation results show the feasibility of the designed transmitter. Similar results can be obtained to SSB-ASK and PR-ASK signal.

VI. CONCLUSION

In this paper, critical design considerations of a integrated, multimode, power-controllable CMOS transmitter are presented. The objective is to implement a UHF band, mobile RFID single-chip reader. The different data mode is supported in both digital and baseband analog domain. A direct up-conversion transmitter minimizes the required off-chip components and provides a low-cost, high-efficient solution. Simulation results verify the feasibility of the proposed transmitter.

REFERENCES