A low-power readout circuit for nanowire based hydrogen sensor

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ABSTRACT

This paper presents a fully integrated lock-in amplifier intended for nanowire gas sensing. The nanowire will change its conductivity according to the concentration of an absorbing gas. To ensure an accurate nanowire impedance measurement, a lock-in technique is implemented to attenuate the low frequency noise and offset by synchronous demodulation or phase-sensitive detection (PSD). The dual-channel lock-in amplifier also provides both resistive and capacitive information of the nanowire in separate channels. Measurement results of test resistors and capacitors show a 2% resolution in the resistance range 10–40 kΩ and a 3% resolution in the capacitance range 0.5–1.8 nF. Moreover, a 28.7–32.1 kΩ impedance variation was measured through the lock-in amplifier for a single palladium nanowire that was exposed to a decreasing hydrogen concentration (10% H2 in N2 to air). The chip has been implemented with UMC 0.18 µm CMOS technology and occupies an area of 2 mm². The power consumption of the readout circuit is 2 mW from a 1.8 V supply.

1. Introduction

Integrated sensor systems are becoming more popular in the worldwide market because of their intensive use in portable applications and lower price compared to the commercial instruments. For example, as the use of hydrogen fuel becomes more common, there is an increasing need for reliable, inexpensive and low-power hydrogen sensors for various applications, such as hydrogen leak detection. Nanowire based devices are promising as a new sensor generation due to their large surface-to-volume ratio which may lead to short response times and high sensitivity, while maintaining a low power consumption and small form factor. Therefore, one of our target sensors is a palladium nanowire based sensor for hydrogen detection [1].

It is a long-term goal to integrate the nanowire processing as a post-processing step on a standard CMOS substrate. For this propose, we have developed a generic impedance measurement circuit which can be combined with such a nanowire sensor to form a fully integrated gas-sensing system.

There have been several reports on resistive or capacitive impedance measurement circuits. Resistance-to-time and frequency-to-digital conversion techniques lead to a wide dynamic range [2,3]. Capacitive readout circuits using dynamic techniques greatly reduce noise and offset [4,5]. Although monitoring the conductivity change of nanowires upon gas exposure generally requires a resistance measurement, the use of a lock-in amplifier offers a more generic approach which enables the measurement of the complex impedance within a certain range while maintaining high measurement accuracy by the use of synchronous demodulation.

In this paper, we describe the design and measurement of an integrated lock-in amplifier, which realizes both resistive and capacitive impedance measurement. This work is outlined as follows. Section 2 briefly describes the lock-in architecture and its building blocks, and then analyzes the design details of the major sub-circuits. Section 3 presents the measurement results of the implemented silicon prototype. We demonstrate the use of the prototype circuit for the readout of nanowire sensors by measuring the response of a single palladium nanowire to a changing hydrogen concentration. Finally, conclusions are drawn in Section 4.

2. Lock-in amplifier

Fig. 1 shows the lock-in amplifier architecture. The nanowire is placed between the input sinusoidal voltage and virtual ground of the voltage amplifier. The I–V converter output voltage, which contains the amplitude and phase information of the nanowire, is filtered by a bandpass filter to remove high-order harmonic interferences. A mixer and low pass filter demodulate the sinusoidal voltage, and provide a DC output proportional to the sinusoidal voltage under investigation. I channel is used for...
nanowire resistance demodulation; Q channel with 90° phase shift is used for nanowire capacitance demodulation.

Fig. 1 also compares the spectrum of sinusoidal signal, noise and offset before and after modulation. Noise and offset errors, which are not synchronized to the reference, are clearly rejected after modulation.

2.1. I–V converter

An input sinusoidal reference signal is applied to the nanowire, or the variable resistor/capacitor under test. The current flowing through the nanowire also passes through the feedback resistor $R_f$. The potential at the negative input of the amplifier is maintained at “virtual ground”, i.e. the reference voltage level. Ideally, without any phase shift of the operational amplifier, the voltage across $R_f$ is proportional to the current flowing through the nanowire. Thus, the phase and amplitude of the output voltage $V_{out}$ contain the information of the nanowire’s complex impedance. This voltage is related to the feedback resistor $R_f$ and the input voltage from the oscillator $V_{osc}$

$$V_{out} = \frac{R_f}{Z_{nanowire}} V_{osc}$$

$R_f$ is selected based on the impedance range of the nanowire and the oscillator output. Generally, the palladium nanowire impedance is in the range from a few kΩ to tens of kΩ, and the tunable oscillator output from a few mV to hundreds of mV. The possible value of the feedback resistor $R_f$ is therefore quite broad. However, considering the input dynamic range limitation of the bandpass filter (BPF) at the next stage (few hundreds of mV), the chip area for implementing the resistor (110–350 Ω per square); and the low power consumption requirement for opamp (in μW range when active), we selected the feedback resistor $R_f = 10$ kΩ.

The operational amplifier should be designed with high enough gain and bandwidth to achieve an accurate closed-loop gain. A two-stage folded-cascade opamp [6,9] has been implemented as depicted in Fig. 2. The $–3$ dB bandwidth is around 100 kHz, and the low frequency gain is over 70 dB.
2.2. Bandpass filter (BPF)

The bandpass filter removes much of the unwanted signals while passing the signal which contains the impedance information. A tunable bandpass filter is necessary for impedance measurement at different frequencies when capacitive measurement is performed. For this reason, the central frequency should have a large tuning range, and the Q factor should be high enough to filter out unwanted signals and noise. A switched-capacitor technique is selected because of its good tuning ability. However, the accuracy of the frequency response of switched-capacitor filters depends on the accuracy of the sampling frequency, the capacitor matching and finite opamp dc gain.

A biquad bandpass filter in Fig. 3 [10] is simulated with resistors to check the frequency response. The circuit transfer function $H(s)$ shows that the filter has a second-order bandpass response with two poles and a zero at the center frequency

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{-R_f C_f s - R_f}{R_f R_f C_f^2 s^2 + R_f R_f C_f s + R_f}$$

The center frequency and 3-dB bandwidth are given by

$$f_0 = \frac{1}{2\pi R_f C_f}$$

$$BW_{3\text{d}B} = \frac{C_f}{R_f C_f^2}$$

The central frequency $f_0$ can be tuned by varying $R_f$ and/or $C_f$. $R_f$ is implemented with an equivalent switched-capacitor circuit, so that $f_0$ can be tuned by varying the sampling clock frequency. Simulation results show that, when $R_f$ is swept from 5 to 50 MΩ, the central frequency $f_0$ varies from 10 to 100 kHz, which fully covers the measuring frequencies. The gain of the bandpass filter is fixed by the ratio of the feedback capacitors, and it is independent of central frequency tuning

$$G_C = \frac{C_i}{C_f}$$

The switched-capacitor implementation of the BPF is shown in Fig. 4. An extra feedback path is introduced to reduce opamp input offset [7].

2.3. Mixer

The mixer is a linear multiplier whose output is the product of two sinusoidal inputs $V_{RF}$ and $V_{LO}$. There are two components in the synchronous mixer output: a double frequency component and a phase-sensitive DC term. A double-balanced mixer (Gilbert multiplier) is often used in RF applications due to the good LO-IF feed-through characteristics. However, the voltage gain of Gilbert cell is input dependent. The mixer in this lock-in amplifier, in contrast, requires more flexibility in the sense that both $V_{RF}$ and $V_{LO}$ are desired to be the gain independent inputs.

Therefore, we propose an alternative mixer circuit topology. The principle is shown in Fig. 5. The mixer is composed of a thermometer code generator, followed with control switches and an analog adder. The thermometer code generator digitizes $V_{RF}$ in a similar way as the input stage of a flash ADC. The resulting

![Fig. 3. Biquad bandpass filter schematic.](image-url)

![Fig. 4. Switched-capacitor bandpass filter.](image-url)
thermometer code controls the switches and modulates the local oscillator signal. Finally, the summation of all modulated signals realizes the frequency multiplication function. This type of mixer has a fixed gain, which only depends on the capacitor ratio. The transfer function of the analog mixer can be written as follows:

$$V_{\text{out}}(t) = \text{int}\left[ \frac{V_{RF} - V_{LO}}{V_{HI} - V_{LO}} \right]^{2N} \frac{C_1}{C_2} V_{LO}(t)$$

where the int[] function indicates that the total number of 1’s generated in the thermometer code. From this transfer function we can derive the relationship between the resolution $N$ and the maximum voltage dynamic range $V_{HI} - V_{LO}$. $V_{HI} - V_{LO}$ is limited by the maximum input voltage dynamic range. The larger $N$, the smaller the least significant bit (LSB) and the higher the resolution of the A/D conversion. This results in a lower harmonic content of the signal at the mixer output, which also reduce the requirements on LPF in the next stage However, the larger $N$, the higher the power consumption, which is proportional to $2^N$.

Traditional thermometer code generators, which use a resistor ladder to make the reference voltage, are power consuming, and are limited in accuracy by resistor mismatch. A replacement circuit using a capacitive divider network is more power efficient, and achieves better matching accuracy. As shown in Fig. 6, two phases are used for calibration and capacitive division respectively [7,13]. During the phase 1, the capacitors $C_1$ and $C_2$ are connected in series and form a close loop, the offset of the opamp are stored in both capacitors. During the phase 2, the offset is cancelled, and the input RF signal is compared with a capacitive divided reference level

$$V_{\text{ref,n}} = C_{1,n} V_{HI} - C_{2,n} V_{LO}$$

Each comparator generates one bit of the thermometer code. If we simply copy the unit shown in Fig. 6 with different $C_1/C_2$, a high resolution thermometer code generator can be obtained. For our lock-in amplifier, a 5-bit resolution mixer with 32 units was implemented.

2.4. Low pass filter (LPF)

The DC output voltage of the mixer, which contains the amplitude information of the resistive or the capacitive part of the nanowire impedance, is separated from higher-order harmonic components by passing the output through a second-order low pass filter in Fig. 7

$$H(s) = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{R_f^2}{R_f^2 R_c^2 s^2 + 2R_f R_c C_f s + R_c^2}$$

Fig. 5. Mixer schematic.

Fig. 6. Thermometer code generator unit using capacitor divider network.

Fig. 7. 2nd order low pass filter.

Fig. 8. Switched-capacitor low pass filter.
$$\omega_0 = \frac{1}{R_fC_f}$$

$$G = \frac{R_f^2}{R_i^2}$$

The switched-capacitor implementation of the LPF is shown in Fig. 8. Capacitors $C_0$ and the associated switches are introduced for offset cancellation [8].

3. Measurement results

The proposed readout circuit implemented with UMC 0.18 μm technology is shown in Fig. 9. It occupies 2 mm² area and consumes 2 mW from a 1.8 V power supply. Each single measurement takes 1 ms, which corresponds to a measurement rate of 1 kHz.

Fig. 10 depicts the measurement testbench including main test PCB, DC source, source generator, Xilinx FPGA and a voltage shifter.

The test PCB consists of test probes, signal connectors and jumper switches on board. Two DC sources provide a power supply of 1.8 V and the opamp reference voltage of 1.0 V. A source generator generates an external sinusoid voltage signal and the pulse master clock of 1 MHz. This master clock applied to FPGA input is able to provide all external sampling and calibration clocks at FPGA I/O ports, and it is easy to switch between different test modes by selecting proper SPI codes. The voltage level shifter PCB consists of series of variable resistors to convert Xilinx FPGA output from 1.5 to 1.8 V.

Measurement results (with resistor and capacitor under test) are shown in Figs. 11 and 12. Ideally, the output DC voltage is linearly proportional to the conductance $1/R$ and the capacitance $C$, as indicated by the dashed curves. Measurement results show that for a 10 kΩ feedback reference resistor, the optimum linear resistance measurement range is from 10 to 40 kΩ with a $6e^{-7}$ S/mV sensitivity. The optimum linear capacitance measurement range is from 0.5 to 1.8 nF with a 13.3 pF/mV sensitivity. Both the resistor and capacitor measurements show a maximum peak-to-peak noise level of 3 mV, which is equivalent to a 2% and a 3% resolution, respectively. Table 1 shows the specifications compared with other works. Although the input referred noise density of this work is higher, the power consumption has been reduced dramatically.

We used the prototype circuit to demonstrate the feasibility of integrated readout of nanowire sensors by measuring the response of a single palladium nanowire to a changing hydrogen concentration.

Palladium nanowires were fabricated on a silicon wafer with an insulation layer of silicon dioxide by using a technique called deposition and etching under angles (DEA) [11]. Each fabricated chip contains an array of Pd nanowires, which are individually addressable by macro scale platinum two-point contacts. Post-processing these nanowires on an integrated circuit may enable compact, ultra-low-power and inexpensive hydrogen gas sensor.
devices. The Pd nanowires used in this work have a typical diameter of about 50–80 nm and lengths of ca. 7 μm. A SEM image of a nanowire is shown in Fig. 13.

The chip containing the nanowires is glued and wire bonded to a standard 24 pins DIL package, which is inserted in a stainless steel flow chamber with electrical feed-through. A single nanowire was connected to the readout circuit. Prior to the measurement, the chamber was filled with 10% hydrogen in nitrogen. Hydrogen is absorbed in palladium by dissociation of molecular hydrogen at the surface and diffusion into the bulk where it forms a solid solution of Pd/H (α-phase) at low hydrogen pressures, and a hydride (β-phase) at high hydrogen pressures [12], leading to an increase in nanowire impedance.

At the start of the measurement, the chamber was opened, allowing the hydrogen to leak from the chamber, causing the nanowire impedance to decrease in response to the drop in hydrogen concentration, until it was stabilized in air.

Fig. 14 shows the result of a measurement performed with a palladium nanowire. The measured DC voltage variation is around 17 mV, which indicates a decrease in the nanowire impedance from 32.1 to 28.7 kΩ. This agrees with a decrease of about 10% of the nanowire impedance as expected from previous measurements [1]. The peak-to-peak noise level is around 3 mV, which turns into a resolution of 0.6 kΩ (2% of the nanowire resistance of 30 kΩ).

4. Conclusion

An integrated lock-in amplifier for complex impedance measurement has been developed and characterized. The circuit was implemented in a 0.18 μm CMOS technology. It was shown that the amplifier can measure a 10–40 kΩ resistor with 2% resolution and a 0.5–1.8 nF capacitance with 3% resolution. We demonstrated the use of the lock-in amplifier for the detection of the impedance variation of 28.7–32.1 kΩ for a palladium nanowire in response to a varying hydrogen concentration of 10–0%.

Table 1
Comparison table with other works.

<table>
<thead>
<tr>
<th>Specification overview</th>
<th>This work</th>
<th>Azzolini [14]</th>
<th>SR830</th>
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<tr>
<td>Voltage gain (dB)</td>
<td>0–20</td>
<td>0–20</td>
<td>&gt;100</td>
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<td>Bandwidth (kHz)</td>
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<td>800</td>
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<td>Preamplifier input referred noise</td>
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<td>15 nV/sqrt(Hz) @ 30 kHz</td>
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<td>Supply voltage (V)</td>
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<td>Power</td>
<td>2 mW</td>
<td>110 mW</td>
<td>40 W</td>
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Acknowledgments

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References


