Ubiquitous Evolvable Hardware System for Heart Disease Diagnosis Applications

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Abstract. This paper presents a stand-alone ubiquitous evolvable hardware (u-EHW) system that is effective for automated heart disease diagnosis applications. The proposed u-EHW system consists of a novel reconfigurable evolvable hardware (rEHW) chip, an evolvable embedded processor, and a hand-held terminal. Through adaptable reconfiguration of the filter components, the proposed u-EHW system can effectively remove various types of noise from ECG signals. Filtered signals are sent to a PDA for automated heart disease diagnosis, and diagnosis results with filtered signals are sent to the medical doctor's computer for final decision. The rEHW chip features FIR filter evolution capability, which is realized using a genetic algorithm. A parallel genetic algorithm evolves FIR filters to find the optimal filter combination configuration, associated parameters, and the structure of the feature space adaptively to noisy environments for adaptive signal processing. The embedded processor implements feature extraction and a classifier for each group of signal types.

1 Introduction

The electrocardiogram (ECG) signal is a tracing of electrical activity signal generated by rhythmic contracting of the heart, and affords crucial information to detect heart disease [1]. Since the ECG signal varies from patient to patient, and according to measured time and environmental conditions, an adaptable heart disease diagnosis algorithm based on context-aware computing has been proposed in which a genetic algorithm (GA) finds the optimal set of preprocessing, feature extraction, and classifier for each group of signal types [1].

This paper presents a stand-alone ubiquitous evolvable hardware (u-EHW) system to process the adaptable heart disease diagnosis algorithm and detect heart disease. The u-EHW system consists of a reconfigurable evolvable hardware (rEHW) chip, an evolvable embedded processor, and a PDA. The rEHW chip

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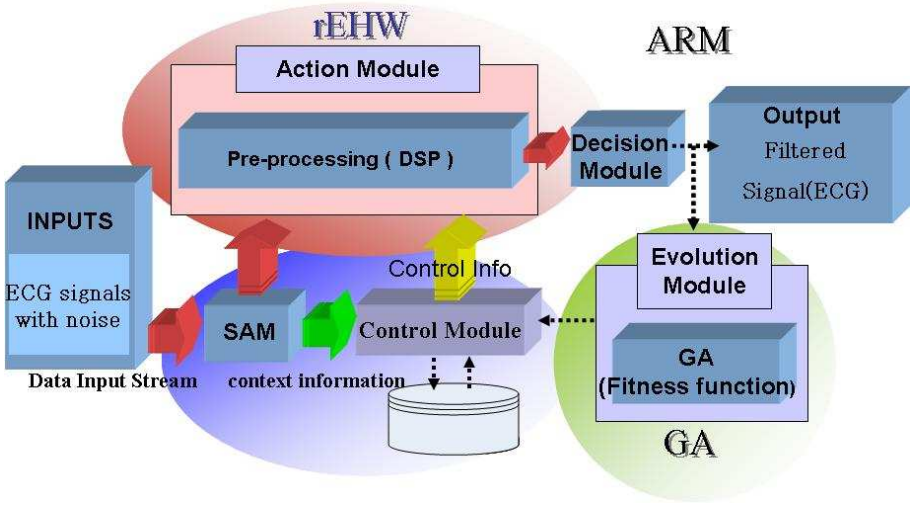

Fig. 1. Block diagram of adaptable heart diseases diagnosis system

can effectively find the optimal set of preprocessing, and processes the adaptive digital signal processing (DSP). That is, the rEHW chip processes the low-pass, band-pass, and high-pass FIR filter algorithms with various frequencies. The evolvable embedded processor operates GA, feature extraction, and a classifier for each group of signal type. Currently, many DSP and smart health care applications are implemented on digital signal processors and embedded processors by software. Effective DSP algorithms require computing architectures that are less complicated, highly flexible, and more cost-effective for smart health care applications. Currently, complex and fast computation can be performed by dedicated hardware instead of digital signal processor since dedicated hardware can operate in parallel. The concept of reconfigurable hardware and evolvable hardware has been studied actively [2-4]. Since evolvable hardware can evolve in real time, it can maintain optimal performance in a variety of unexpected environments. The configurations that optimize the device output responses are combined so as to make better configurations until an optimal architecture can be realized [6]. Evolvable hardware continues to reconfigure itself in order to achieve better performance.

In contrast to the conventional ECG signal measurement system, the proposed u-EHW system can measure and analyze the ECG signal in a ubiquitous environment. For this, a GA based rEHW chip effectively reconfigures the filter components to remove noise components. Filtered signals are sent to a PDA for automated heart disease diagnosis, and diagnosis results with filtered signals are sent to the medical doctor's computer where a final decision can be made. Through this, patient customized healthcare service in ubiquitous environments can be realized.

2 Adaptable Heart Disease Diagnosis Algorithm

The adaptable heart disease diagnosis algorithm mainly consists of six modules; a noise context estimation module, a control module for filter block design at running mode, a rEHW module for a 3-stage filter block, a GA module for filter design at evolution mode, a decision module for fitness calculation at evolution mode, and a disease diagnosis module, as shown in Figure 1.

Accurate estimation of ECG signal noise in a dynamic environment is impossible since signal artifacts from respiration, motion activity, and their coupled signal noise are not predictable. For this reason, noisy signals are grouped into several categories by environmental context estimation. Baseline wander noise and muscle noise are then quantized based on environmental context information.

In order to identify the adaptable filter composition, the outputs of the noise context estimation module are fed to the inputs of the control module. The control module consists of two parts, an evolutionary knowledge accumulator (EKA) and a neural network for the filter design. The EKA stores the optimal filter design results for six-clustered dynamic measurement environments. For network construction, two types of outputs from the context estimation module are used as network inputs and six outputs are used to cluster the dynamic measurement environment into six groups. The 6 best filter combinations for each cluster are a 0.8 45 Hz band pass filter, a 0.8 Hz high pass filter, a 50 Hz low pass filter, a combination of a 0.8 Hz high pass filter and a 50 Hz low pass filter, a combination of a wavelet interpolation filter (WIF) and a 0.8 45 Hz band pass filter, and a combination of WIF, a 0.8 Hz high pass filter and a 50 Hz low pass filter. For clustering of environmental noise, a three layered feed-forward error back-propagation neural network (BPNN) is applied and network weights are updated after each training vector (by "training by vector" method).

For a continuous performance update, every filtered output from the 3-stage filter block is evaluated by fitness function at decision module. The fitness function is defined as the detection percentage of five ECG signal features, i.e., P-R interval, QRS duration, Q-T interval, R-R interval, and S peak point, using So & Chan and Kim's feature extraction method [1].

3 Ubiquitous Evolvable Hardware System

The overall u-EHW system consists of a rEHW chip, an evolvable embedded processor, and a hand-held terminal, as shown in Figure 2. The input data of the rEHW and evolvable embedded processor is the measured ECG signal data, which may contain muscle noise, baseline noise, in-coupling noise, and 60 Hz power line noise.

3.1 Reconfigurable Evolvable Hardware Chip

The rEHW chip processes the DSP algorithms, i.e., low- pass, band-pass, and high- pass filter algorithms with various frequencies. This chip consists of a

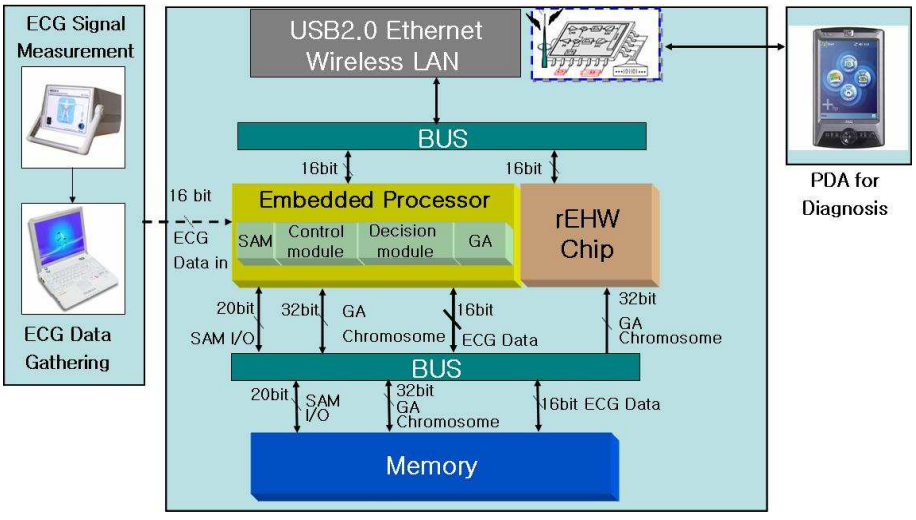

Fig. 2. Block diagram of ubiquitous evolvable hardware system

reconfigurable processing unit, a configuration manager, and coefficient memory, as shown in Figure 3. The reconfigurable processing unit has a 3-stage reconfigurable filter block in which the optimal FIR filter function can be searched and selected by GA chromosome data obtained using a GA running on an embedded processor. Each reconfigurable filter block includes 20 reconfigurable processing modules (RPMs).

The GA has been used to evolve digital circuits. A chromosome represents a component of order. The 30-bit GA chromosome data has 3-stage 30-bit chromosome data, which defines the type of optimal filter, cutoff frequency, and filter order, as shown in Fig. 4. The first 2-bit data decides the optimum filter type, such as a low-pass, band-pass, or high-pass filter. If a high-pass filter or low-pass filter is selected by the GA, cutoff frequency#1 or #2 has the data, respectively. If the band-pass filter is selected, cutoff freqeuncy#1 and #2 have the data. The last 3-bit data defines the filter order, which decides the number of filter taps, from 6- to 20-taps. The configuration manager consists of the order distributor, stage selector, and memory address decoder. The order distributor analyzes the filter order information and the stage selector selects the filter stage to be used. Coefficient memory stores the coefficients, which are used in each filter.

The rEHW chip is responsible for providing the best solution for realization and autonomous adaptation of FIR filters, and is used to process the optimal DSP algorithms for noise removal operation prior to feature extraction and classification steps. Generally, low-pass, band-pass, and high-pass filters are used separately in many preprocessing algorithms [1].

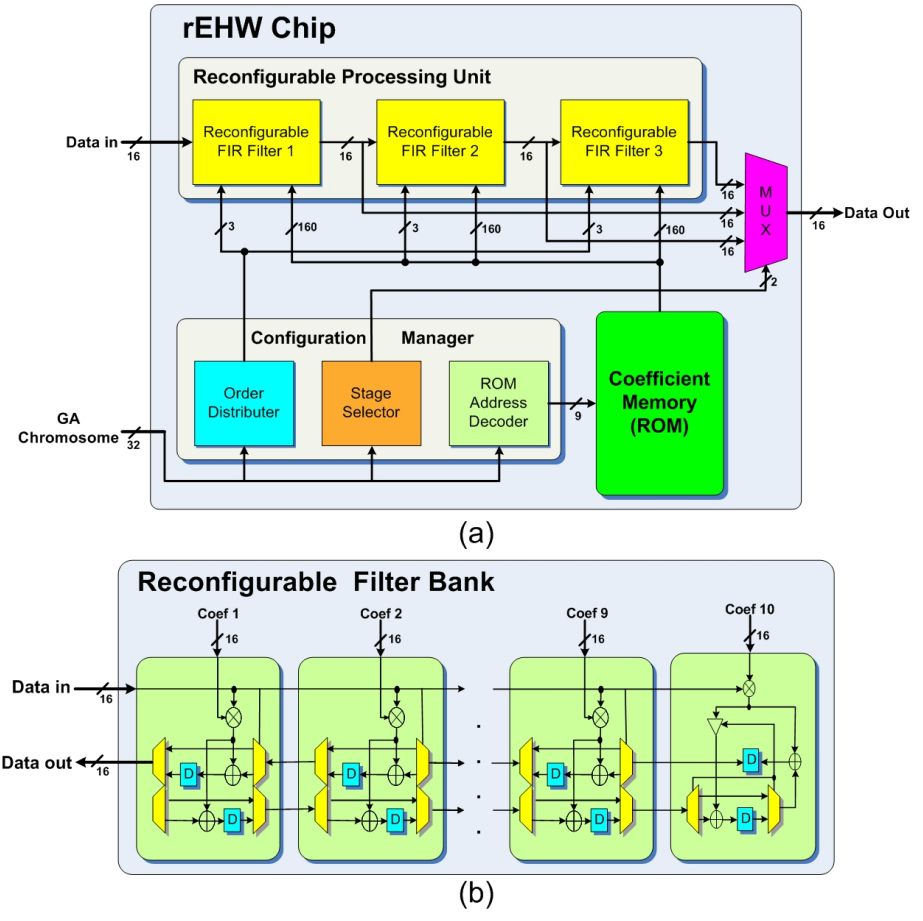

Fig. 3. Block diagram of (a) reconfigurable evolvable hardware and (b) reconfigurable filter block

3.2 Evolvable Embedded Processor

The evolvable embedded processor implements a noise context estimation module, decision module, and control module to process the feature extraction and classifier algorithms by software. Also, embedded processor processes the GA, which is a search procedure inspired by populating genetics, and has excellent search capabilities for finding a good solution to a problem without a priori information about the nature of the problem [7].

For a continuous performance update, every filtered output from the rEHW chip is evaluated by a fitness function at the decision module. To determine the adaptable filter composition, the outputs of the noise context estimation module are fed as inputs of the control module. The fitness function is defined as the detection percentage of five ECG signal Features; P-R interval, QRS duration,

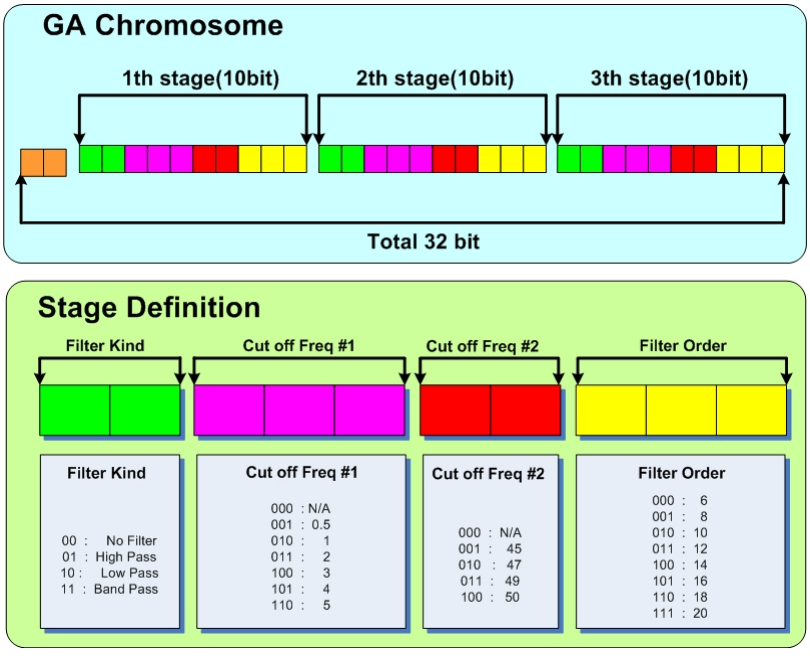

Fig. 4. GA chromosome data definition

Q-T interval, R-R interval, and S peak point, using So & Chan and Kim's feature extraction method [1]. In order to confirm the fitness function, the filtered signals are fed into the noise context estimation module again. If the fitness value is greater than 0.8, the ECG feature extraction results are considered to be acceptable values. The noise context estimation module can estimate the noise context using a neural network for filter design. For this, pre-determined optimal filter design results for six-clustered dynamic measurement environments are stored. For network construction, two types of outputs from the noise context estimation module are used as network inputs and six outputs are used to cluster the dynamic measurement environment into six groups. For clustering of environmental noise, a three layered feed-forward error back-propagation neural network (BPNN) is applied and network weights are updated after each training vector (by the "training by vector" method).

4 Implementation and Result

The rEHW architecture was modeled in Verilog HDL and functionally verified using a ModelSim simulator. The output data from the Verilog coded architecture was validated against a bit-accurate MATLAB model. The rEHW chip was implemented using standard 0.18-μm CMOS technology. Figure 5 shows the rEHW chip layout and Table 1 shows the rEHW chip summary.

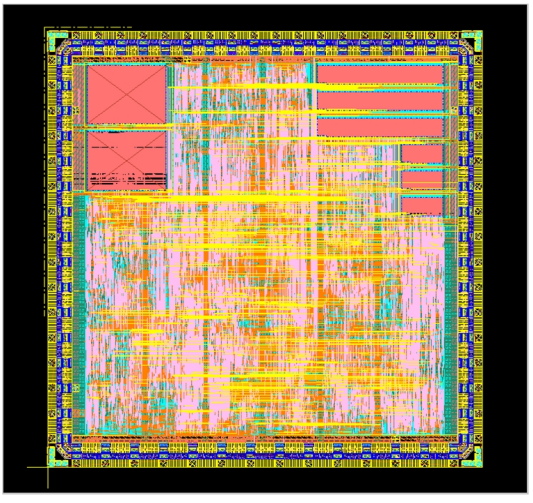

Fig. 5. rEHW chip layout

Table 1. rEHW chip summary

	Chip Summary
Technology	Standard 0.18-μm CMOS 1.8V core, 3.3V I/O
Die size	3.75×3.75 mm^2
Package	64-pin LQFP
Gate Count	582,182
Clock Speed	80 MHz

The rEHW chip consists of 582,182 gate excluding memories and the operating clock frequency is about 80 MHz. There are five control/status registers in the rEHW chip, a control register, interrupt status register, interrupt clear register, and two chromosome registers. Besides these control/status registers, 4Kbytes of input and output buffer memory are allocated for data transfer between the rEHW chip and embedded processor. Each ECG data consists of 1024 samples and they are processed by the rEHW chip. The chromosome used by the rEHW chip is selected by the GA algorithm in the embedded processor and set in the chromosome register. The rEHW chip processes 1024 items of data every 15 sec. After processing data, the rEHW chip generates interrupt the embedded processor in order to update processed data.

The complete stand-alone u-EHW system for adaptable heart disease diagnosis was tested on an embedded system test-bed including the rEHW chip and evolvable embedded processor. The noise context estimation module, control module, decision module, and GA have been implemented by a bit-accurate C-model and implemented on an embedded processor.

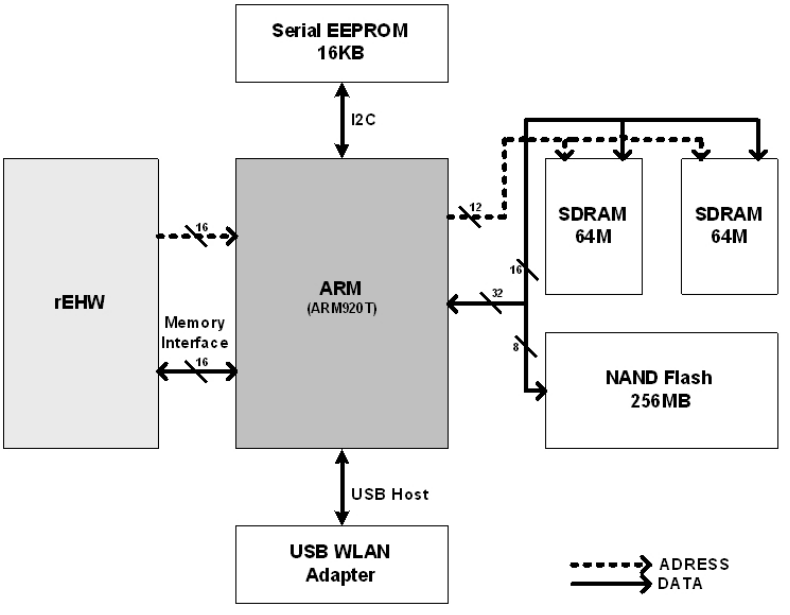

Fig. 6. Block diagram of u-EHW test-bed

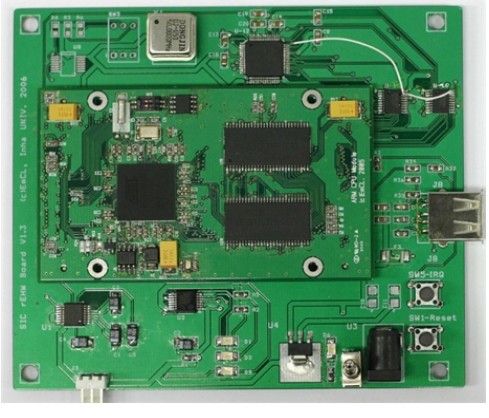

Fig. 7. Implemented u-EHW system test-bed

The implemented test-bed consists of an ATMEL AT91RM9200 ARM processor, of which the performance is 200 MIPS, a rEHW chip, external memories, and a LAN interface, as shown in Figure 6. To avoid coupling noise when running at a high speed of 200 MHz, the whole system is divided into two sections of a 6-layer PCB; a CPU board and a communication/rEHW chip board. Figure 7 shows the implemented u-EHW test-bed including the embedded processor

Fig. 8. u-EHW system platform for automated heart disease diagnosis applications

board and rEHW chip board. Embedded Linux version 2.6.12 is ported to support application software such as the noise context estimation module, control module, and decision module. A standard Linux-hosted Pentium PC is used as a development environment. GCC 3.4 is used for cross compiling and targeting to the embedded processor system. A 100 Mbps LAN network is used for the software development and debugging and a wireless LAN provides connectivity to the handheld application devices.

To demonstrate the u-EHW system, a set of sample ECG data were gathered from various patients and stored in the embedded processor board. The raw data and diagnosis results were transmitted to the hand-held terminal (PDA) in real-time over a wireless LAN. The PDA is used to display ECG data and diagnostic results. It displays the raw data wave and the processed wave as well as one out of four diagnostic results; SB, ST, RBBB, and LBBB. Figure 8 shows the stand alone prototype system of u-EHW.

5 Conclusion

In this paper, we present a ubiquitous evolvable hardware (u-EHW) system, which implements a stand-alone adaptable heart disease diagnosis system. The u-EHW system consists of a rEHW chip, an evolvable embedded processor, and a PDA. The rEHW chip is used for adaptive digital signal processing and the embedded processor implements feature extraction and a classifier for each group of signal type. The proposed stand-alone u-EHW system performs well, especially in changing noisy environments, since it can adapt itself to the external environment. The proposed u-EHW system is a promising solution for various applications such as DSPs, communications, and smart healthcare systems in a ubiquitous environment.

Acknowledgement

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