Panel 2

Should logic SER be solved at the circuit level?

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SER is one of the problems associated with continued scaling. Traditionally, logic SER is solved at the system/architecture level (e.g., DMR, TMR, checkpointing/recovery). There has also been some work at the process level (e.g., SOI), but recently, there is also some research work on circuit level (e.g., cell hardening, BISER), but there has not been a wide spread adoption yet. Can logic SER be solved at the circuit level? Should they be? We have a team of experts from system, architecture and circuit area to debate this topic.