High performance printed N and P-type OTFTs enabling digital and analog complementary circuits on flexible plastic substrate


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Abstract
This paper presents a printed organic complementary technology on flexible plastic substrate with high performance N and P-type Organic Thin Film Transistors (OTFTs), based on small-molecule organic semiconductors in solution. Challenges related to the integration of both OTFT types in a common complementary flow are addressed, showing the importance of surface treatments. Stability on single devices and on an elementary complementary digital circuit (ring oscillator) is studied, demonstrating that a robust and reliable flow with high electrical performances can be established for printed organic devices. These devices are used to manufacture several analog and digital building blocks. The design is carried out using a model specifically developed for this technology, and taking into account the parametric variability. High-frequency measurements of printed envelope detectors show improved speed performance, resulting from the high mobility of the OTFTs. In addition, a compact dynamic flip-flop and a low-offset comparator are demonstrated, thanks to availability of both n-type and p-type OTFTs in the technology. Measurement results are in good agreement with the simulations. The circuits presented establish a complete library of building blocks for the realization of a printed RFID tag.

1. Introduction
Organic electronics has attracted significant interest as possible inexpensive and flexible alternative to conventional electronic technologies. Indeed, tremendous progress has been made in this field during the last decade, opening promising perspectives for applications such as flexible displays, logic circuits for radio-frequency identification (RFID) tags and sensing devices [1]. Processing materials in solution makes possible to use printing processes that are well appropriate for large area flexible substrates and thus for low cost production.

Recently, significant advances have been made on the development of solution processable organic semiconductors (OSCs) and both P- and N-type materials that present high performance and good air-stability are now available [2,3]. The integration of both P- and N-type OSC enables the fabrication of complementary circuits which are characterized by better speed and reliability when compared to their unipolar counterparts [4,5].

Several organic complementary circuits made with solution deposited materials have been reported already [3,4,6,7], but there is still no work presenting a fully printed complementary technology on flexible substrate featuring at the same time high mobility P- and N-type semiconductors. In addition, the circuits demonstrated in printed technologies are mainly limited to digital design and switch matrices [7–12].

In previous work [8], we presented fully printed organic complementary circuits on plastic substrates with a first generation of P- and N-type semiconductors and lower mobilities ($\mu_N < 0.06 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$/$\mu_P < 0.04 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$). In this paper we present a printed organic complementary technology made on flexible foils (sheet-to-sheet technology) employing N- and P-type small-molecule semiconductors [9] with higher mobilities (Table 1) and that are more suitable for applications like radio frequency identification (RFID). In Section 2 the process optimizations needed to achieve higher mobilities for N- and P-OTFTs and to enable the integration of both P- and N-type transistors in a common flow.
are presented in detail, together with a study of the technology stability on single devices and elementary complementary circuits.

In order to implement organic electronic applications like RFIDs using printed production processes, three main challenges need to be overcome: first, the transistor switching speed (which is basically determined by the OTFT mobility) must be sufficient to enable RF rectification using diode-connected OTFTs. Second, digital electronics with a complexity of at least 100 logic gates and sufficient yield (which is limited by hard faults and OTFT parameter variations) must be enabled. Third, analog circuits with sufficient accuracy to discriminate small input signals (mainly limited by mismatch) must be realized to implement the receiver radio. To show that our technology is suitable to realize RFID applications, several mask sets containing a large set of analog and digital building blocks have been processed. The digital and analog building blocks implemented in these masks [13] were specifically chosen and optimized for RFID applications, to address the mentioned challenges. The design was carried out using a physical compact model developed specifically for n-type and p-type OTFT devices manufactured with this printed complementary technology [14], and taking into account the measured parametric variability. The various circuits are described in detail in Section 3. The first circuit block discussed is an envelope detector/rectifier, in which the potential effect of increased OTFT mobility on high-frequency rectification is evident. Then the design and measurements of several combinatorial and sequential digital blocks, needed to implement the RFIDs logic, are presented. Different realizations of complementary logic circuits including fully-static, dynamic, and transmission-gate design styles are shown. Finally, in the analog circuit domain, the availability of both n-type and p-type transistors has made possible to employ simple but effective offset canceling techniques, and to demonstrate a low-offset comparator. This comparator together with an envelope detector can provide the basis for AM modulation, which is required to implement RFID protocols of the reader-talks-first kind.

### Table 1

<table>
<thead>
<tr>
<th></th>
<th>P-type</th>
<th>N-type</th>
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<tr>
<td>$V_{tst}$ (V)</td>
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<td>18</td>
</tr>
<tr>
<td>$V_{ren}$ (V)</td>
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<td>1</td>
</tr>
<tr>
<td>$\mu$ (cm$^2$V$^{-1}$s$^{-1}$)</td>
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<td>0.35</td>
</tr>
<tr>
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<td>$-2 \times 10^{-6}$</td>
<td>$-5 \times 10^{-14}$</td>
</tr>
<tr>
<td>$I_{off}$/L/W ($A$)</td>
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<td>$-2 \times 10^{-7}$</td>
</tr>
<tr>
<td>Subthreshold slope (V/dec)</td>
<td>2.4</td>
<td>1.2</td>
</tr>
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#### 2. Complementary technology

##### 2.1. Complementary process flow

The organic complementary circuits are fabricated on 11 cm × 11 cm flexible foils using a top-gate bottom-contact structure for both N and P-type devices (Fig. 1). The process starts on a 125 µm-thick polyethylene-naphthalate (PEN) foil. Gold is sputtered to a thickness of 30 nm and then patterned either by photolithography directly or by laser ablation, forming the source and drain electrodes as well as the 1st level of interconnection lines between gates. Then, a Self-Assembled Monolayer (SAM) is deposited to optimize electron injection in the Lowest Unoccupied Molecular Orbital (LUMO) of the N-type organic semiconductor [15]. The N-type OSC (Polyera ActivInk) is first patterned by printing methods, in order to form the individual devices, leading to a fixed thickness in the range of 50–200 nm. Then, the source/drain electrodes and the PEN in P-type areas are cleaned with an O$_2$ UV-free plasma during 180 s to prepare the surface for the SAM deposition and P-type OSC (TIPS-pentacene) printing. The thickness of P-type OSC patterns is also in the 50–200 nm range. The common fluoropolymer dielectric (CYTOP) is screen-printed on top of both semiconductors and then annealed, leaving open areas for via holes, with a final thickness of 750 nm. Finally, a silver-ink conductor is screen-printed on the top of the dielectric and annealed at 100 °C, forming.
in the same step the gate electrodes for devices and the 2nd level for interconnection.

Transfer curves of N- and P-type devices with $L = 100 \mu m$ and $W = 2000 \mu m$ processed with our complementary technology are plotted on Fig. 2, exhibiting mobilities of 1.5 cm$^2$ V$^{-1}$ s$^{-1}$ for P-OTFTs and 0.55 cm$^2$ V$^{-1}$ s$^{-1}$ for N-OTFTs. The typical electrical characteristics of transistors are listed in Table 1. In addition to high mobility, both P and N-type transistors present high ratio between the On and Off currents as well as steep subthreshold slopes.

2.2. Process optimizations

The first step was to find the best process point for P- and N-OTFTs, separately. After this, the integration of both transistor types in a common flow without deteriorating their electrical performance has been addressed, leading to additional optimizations.

2.2.1. Morphology of the P-type semiconductor layer

An important part of the work on P-OTFTs has consisted in optimizing the P-type layer crystallization by improving the formulation of the semiconductor. In particular, the effect of the solvent on the semiconductor morphology and on the electrical characteristics of the P-type transistors after annealing has been studied. Fig. 3a shows that each solvent leads to a specific crystal morphology and grain size, which highly impacts the mobility of transistors (Fig. 3b). The formulation with dichlorobenzene presents a poor morphology with small grains and high roughness, giving a mobility around 0.4 cm$^2$ V$^{-1}$ s$^{-1}$. A larger grain size as well as smaller crystal roughness make the mobility increase. With the tetralin or cyclopentanone solvents, the mobility becomes higher than 1.5 cm$^2$/V s. Due to the high boiling temperature of these solvents, the grains of the layer are much larger after annealing and the roughness of the crystals is also much smaller.

2.2.2. N-OTFT contact injection

To improve the injection of electrons from the source/drain electrodes, four different SAMs (2M2PT:2-Methyl-2-propanethiol DT:1-Decanethiol PT:1-Propanethiol 4MTP:4-Methylthiophenol) in 3 different solvents (ethanol, toluene, dichlorobenzene) have been investigated by plotting the mobility of the corresponding N-OTFTs (Fig. 4). The first observation is that both SAM nature and solvent have a strong impact on mobility. With the dichlorobenzene solvent, both 4MTP and DT SAMs give a similar mobility around 0.15 cm$^2$ V$^{-1}$ s$^{-1}$, whereas the 2M2PT and PT SAMs give lower mobilities in the range of 0.06 cm$^2$ V$^{-1}$ s$^{-1}$. When coming to the toluene solvent, the use of the 4MTP SAM becomes more evident, giving a mobility around 0.35 cm$^2$ V$^{-1}$ s$^{-1}$. Coupled with the ethanol solvent, the 4MTP provides the best results with a mobility of 0.64 cm$^2$ V$^{-1}$ s$^{-1}$.
treatments: Reactive Ion Etching (RIE) plasma with two exposure times (60 s and 100 s), UV ozone exposure of 5 min and no treatment. The electrical performances of N-type transistors obtained in the different cases are compared in Fig. 5a, showing that all the treatments induce a decrease of the mobility. In particular, the UV ozone treatment leads to a strong deterioration of the N-OTFT electrical characteristics, demonstrating that the N-OSC is damaged under UV rays exposure. Fig. 5b also shows that the onset voltage is shifted towards negative voltages when the exposure time of RIE plasma increases from 60 s to 100 s, which confirms that RIE plasma treatments must be avoided to obtain the best performance from the N-OSC.

Further to previous conclusions, another plasma treatment with an UV-free option has been tested, with several exposure times from 150 s to 240 s. Firstly, we have studied the capability of this treatment to clean sufficiently the PEN/gold electrodes surface of P-type OTFTs. For this, the ON resistance ($R_{ON}$) of P-type devices has been calculated from the output characteristics $I_{D}-V_{D}$ shown on Fig. 6a according to (1).

$$R_{ON}(V_{GS}) = \frac{\partial I_D}{\partial V_D}\bigg|_{V_D=0V}$$  

The transistors tested have identical geometries (especially same channel length) and identical intrinsic mobilities, which means their channel resistance is also comparable. As $R_{ON}$ is the sum of channel and contact resistances, comparing it is equivalent to compare the contact resistance of the different P-type transistors, which is a good indicator of the gold electrodes cleaning. Fig. 6b shows that without any plasma treatment, $R_{ON}$ is 1.5–6 times higher (and also a non-linear behavior of the output characteristics – Fig. 6a), demonstrating the necessity of a surface treatment for P-OTFTs. Moreover, we see that there is an optimum point for 180 s exposure time.

In addition, Fig. 6c and d shows that the threshold voltage and mobility of N-type devices exposed to UV-free plasma are the same than without plasma treatment whatever the exposure time, validating that the N-OSC is not damaged by the UV-free plasma treatment.

2.3. Stability of the complementary technology

2.3.1. Single devices

After optimizing the process flow, the question of stability and repeatability of our complementary technology has been addressed. Fig. 7 represents the threshold voltage and mobility of several P- and N-OTFTs on nine sheets processed between October 2011 and March 2012 with our complementary flow (only minor process changes between the different sheets). The on-sheet variability is shown using error boxes and bars. We observe that the threshold voltage is pretty constant for N-type devices but there is some dispersion for P-type OTFTs from sheet to sheet. The mobility of P-OTFTs on the same sheet presents a larger dispersion than for N-OTFTs devices. From sheet to sheet, the mobility is quite repeatable for both P- and N-type transistors.

The yield has also been studied, considering the ratio between the Ion and Ioff currents as figure of merit. A transistor is considered functional if the Ion/Ioff ratio is higher than a given value. The yield of P- and N-type transistors has been computed on five target Ion/Ioff (from $I_{on}/I_{off} > 10^3$ to $I_{on}/I_{off} > 10^6$) and for a long (100 μm) and a shorter (20 μm) channel length (Fig. 8). Transistors exhibit high yield values. Assuming a target $I_{on}/I_{off} > 10^3$ (which guarantees functional circuits), the yield is higher than 98% for both N- and P-OTFTs and is similar for $L = 100 \mu m$ and $L = 20 \mu m$. The yield remains high for more severe targets till $I_{on}/I_{off} = 10^3$.

2.3.2. Elementary complementary circuits

Several mask sets including different analog and digital circuits have been processed on 11 cm × 11 cm foils – Fig. 9a. The circuits were measured in air and during several weeks: this shows that
operational and shelf-life times are not critical. Details on the design and on the measurements are presented in the next section. In addition, the stability of the technology on a longer period has been studied using a seven-stage ring oscillator (Fig. 9b).

The seven-stage ring oscillator reaches high oscillation frequencies varying from 1.2 kHz @ 40 V to 200 Hz @ 20 V, corresponding to delay/gate values of 60 \( \mu \)s and 350 \( \mu \)s, respectively (Fig. 10). Moreover, as shown on Fig. 11, after 6 months in ambient air, the oscillation frequency remains basically unchanged (1.4 kHz@40 V). We observe a modification of the pull down behavior, which may derive from the fact that our plastic sheets are not protected by a barrier layer.

3. Complementary circuits for RFID applications

One of the most interesting applications of organic electronics is in the RFID field. Organic TFT production processes based on printing, like the one described in this paper, make it indeed possible to print RFIDs on the packaging of retail items and offer potential low cost. Different building blocks in both digital and analog domain are needed to implement an RFID tag. Fig. 12 depicts a simplified diagram of an RFID for a reader-talks-first protocol. In this architecture, the reader sends a high-frequency carrier on which data is AM modulated. The carrier is rectified first to generate the power for the rest of the tag circuitry. Then the input signal is demodulated to obtain the data sent by the reader. These data are compared with part of the RFID code and, depending on the result of the comparison, a response is sent back (or not) after a random delay. Therefore, three main tasks are performed in this kind of RFID: high-frequency (HF) rectification, AM demodulation, logic comparison and code generation. In this section the main building blocks needed to realize each of these functions are presented in detail, together with the advantages and challenges that our printed technology brings to their implementation.

3.1. High-frequency (HF) rectification

As discussed before, the performance of organic transistors at RFID frequency is very critical for the aimed applications (in our case we want to focus on the HF band, 13.56 MHz). A significant improvement is expected from the technology described here compared to the results obtained with the printed organic complementary technology presented in [8], since the mobility has been improved by a more than a factor of 10. To explore this point, several samples of transistors have been measured in a diode-connected configuration with an external load, to simulate an envelope detector or a small-size rectifier.

![Graph showing the performance of organic transistors at RFID frequency](image)

Fig. 6. Effect of UV-free plasma treatment done on P-type areas after N-OSC deposition on the cleaning of P-OTFT contacts (a) (b) and also on the saturation threshold voltage (c) and mobility (d) of N-OTFTs. L = 100 \( \mu \)m W = 2000 \( \mu \)m. |Vgs| = 60 V. (Reprinted, with permission, from [9].)
istor, based on its measured static characteristics. The DC output voltage \( V_{\text{out}} \) of the Gen. 2 envelope detector is significantly higher than that achieved with Gen. 1 TFTs. In addition, the difference between the two output voltages increases as the frequency is raised. This demonstrates that the increased mobility of Gen. 2 has significantly improved the high-frequency performance of the p-type OTFTs used as rectifier. The last issue to solve in order to use diode-connected transistors in the rectifier needed to power an RFID at HF (13.56 MHz), is to minimize the voltage drop due to the large TFT threshold. This can be done using circuit-based threshold cancelation techniques and will be the objective of further research.

3.2. Digital and analog circuit design

Combinatorial and sequential logic are essential for data comparison and code generation tasks in an RFID tag. For the AM demodulation task, together with an envelope detector, a compar-

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**Fig. 7.** Repeatability of threshold voltage (a) and mobility (b) in saturation regime \(|V_{ds}| = 60 \text{ V}\) of P and N-type transistors on nine sheets processed between October 2011 and March 2012. For each sheet, 8 P-OTFTs and 8 N-OTFTs with \( L = 100 \mu \text{m} \) \( W = 2000 \mu \text{m} \) have been tested. (Reprinted, with permission, from [9]).

**Fig. 8.** Yield of P- (a) and N-type (b) OTFTs for two channel lengths \( (L = 100 \mu \text{m} \) and \( L = 20 \mu \text{m} \)) with \( I_{\text{on}}/I_{\text{off}} \) ratio as a figure of merit for functional circuits. Median values are calculated on 60 transistors for \( L = 100 \mu \text{m} \) and 85 transistors for \( L = 20 \mu \text{m} \), processed on five foils. (Reprinted, with permission, from [9]).
ator is needed. To design and simulate these building blocks, a physically based compact model able to describe both n- and p-type OTFTs [14] has been used. A single set of “typical” parameters is often not sufficient to enable a reliable design of printed organic circuits. The reason for this is the limited uniformity typical of OTFT manufacturing processes based on printing.

For this reason, to obtain a more reliable estimation of the circuit performance taking into account parametric variability, we carried out simple Monte Carlo (MC) simulations of our circuit designs. The MC simulations were performed based on the variability measured for the channel parameters in a suitable set of devices, and keeping all parameters uncorrelated. The experimental results and the simulations based on the described model are in good agreement. Although in some cases the experimental results may be quantitatively different from the “nominal” simulations, they fit very well in the range of performance predicted by the MC simulations. The channel length of all the transistors in the designs presented is 20 μm.

3.2.1. Fully-static logic

In this subsection, the simulation and characterization of different static digital building blocks including inverters, NAND gates and a NAND-based flip–flop are presented. Monte Carlo (MC) sim-
Simulations were performed on an inverter with different values of p- and n-type transistor widths. Fig. 14 illustrates 50 MC launches on an inverter with \( \frac{W_p}{W_n} = 1/2 \), at supply voltage \( V_{dd} \) of 40 V. Fig. 14 shows that despite the observed variability, the inverter is functional with acceptable noise margin in all the simulated cases and its transfer characteristic curves are centered at \( V_{dd}/2 \). We can thus conclude that good robustness is achieved thanks to the use of complementary OTFTs.

The comparison between simulations and measurement results for different circuits shows that the model predicts well the behavior of the circuit. Fig. 15 shows in particular the nominal simulation and experimental results of a fully static NAND gate (depicted in the inset), for \( V_A = 40 \) V and \( V_B \) swept from 0 to 40 V. The measured hysteresis is negligible.

In the domain of sequential logic, a fully static JK-FF as shown in Fig. 16a was designed. Each three-input NAND gate is made of six transistors, and the FF consists of 20 transistors in total. The circuit was measured at \( f_{clk} = 100 \) Hz and keeping the input “\( J \)” equal to negated “\( K \)” \( (j = R) \) to obtain a D flip-flop truth table. The results are shown in Fig. 16b, when the CLK goes high Q follows the input value, and when the CLK goes low the FF is in hold state.

The fully-static realization, though robust in the presence of injected noise, is expensive in terms of area. This is an important drawback in printing technologies where conservative design rules and a large distance between n-type and p-type semiconductor areas must be observed. The high transistor count results then in a strong increase in the area of printed fully static digital circuits with higher complexity, e.g. master-slave (MS) FFs, and makes difficult to use them in real applications, because it enhances their sensitivity to hard faults. For this reason we investigated alternative digital design styles which enable more compact circuits, namely dynamic and transmission-gate based logic.

### 3.2.2. Dynamic and transmission gate logic

To be able to implement dynamic logic, the technology needs to feature p-type OTFTs with a negative threshold and n-type OTFTs with a positive one, so that both types of transistors can be well switched-off. A dynamic NAND gate (followed by a static inverter used to buffer the output for measurement purposes) was designed and measured. The schematic of the gate and the measurement results for the input values \( AB = 01 \) and \( AB = 11 \), are shown in Fig. 17. When the clock signal (CLK) is low, the dynamic output (Outd) goes high, driving the static output (Out) to ground. As expected, when Clock is high, Out goes high only if both of the inputs (A and B) are high. So the overall gate works as an AND. The frequency of Clock \( (f_{clk}) \) is 150 Hz and \( V_{dd} \) is 40 V.

A dynamic true single phase clock (TSPC) FF [16] has also been designed and measured. The TSPC FF (Fig. 18a) consists of only 11 transistors, compared to the 36 transistors needed for a typical static MS D-FF. For the reason discussed before, this leads to a much smaller footprint, almost 10 times smaller than the fully-static DFF designed in our technology.

Fig. 18b shows the experimental results of TSPC-FF measurements. When the clock signal (CLK) is low, the first stage is trans-
parent and its output (X1) is equal to the complement of D, while the second stage is precharging (X2 = high) and thus, the third stage (X3) is in hold state. When the Clk switches to high, the second stage evaluates the input and depending on the value of X1, X2 stays high (for X1 = low) or goes to low (for X1 = high). Therefore, at the positive edge of Clk, Q changes state depending on the value of D, while Q remains constant when the Clk goes low. The measurement clock frequency (f_{clk}) in the figure is 100 Hz.

Another option for implementing logic circuits is to exploit transmission gates (TG), which can also easily be built in our complementary technology. Flip-flops based on TGs have a lower area compared to fully-static ones, and are less vulnerable to soft failures compared to dynamic designs. Fig. 19a shows the FF based on TG which consists of two consecutive latches, each of which is active in half a clock cycle. The Clk and Clk signals are generated from an external clock (Clk_ext) using two inverters. When the Clk
is high, the FF is on hold mode. In the master stage, the TG is on and the output is equal to \( D \). In the slave stage, the TG is off, but depending on the output level (high or low), one of the feedback loops is closed, to keep the value at the output node of TG. In this way, for all the nodes there is always a path to \( V_{dd} \) or ground. When the Clk goes low, the master is on hold and the slave is active, so the output will change depending on the value of input at the falling clock edge.

### 3.2.3. Comparators

The correct functionality of an envelope detector at RFID HF frequency has been demonstrated in Section 3.1. In a reader-talks-first protocol, an AM demodulator of the power carrier on the tag is also needed. Therefore, a comparator will be needed to extract the data from the envelope of the high-frequency carrier.

In the analog domain, the main design challenge in printed technologies is to achieve the desired accuracy in the presence of the relatively large device mismatch typical of printed OTFTs. This point is better illustrated in Fig. 20, where the nominal simulation of a simple OTA (the simplest differential comparator we could think of) and measurements of three different samples are shown. The circuit in Fig 20a was measured statically with one of the inputs (In+) kept to 25 V DC, while the other input (In–) was swept. Fig. 20b shows the results: the output offset results in the measured samples varies from 1.5 to 4 V. Offset cancelation for a differential amplifier is rather complex due to several capacitors and switches needed, and could lead to yield problems. Therefore, a simpler approach, which does not involve matched OTFTs, has been attempted.

Fig. 21a shows the schematic of a simple dynamic comparator which is not based on a differential pair. The design extends a similar approach used in [17]. When Clk is high (reset phase), the transmission gate S1 and S2 put the inverter in unity-gain and charge the capacitor \( C \) to the voltage difference between the negative input \( (V_{in}^-) \) and the dc operating point of the inverter. When the Clk goes low (comparison phase), transmission gate S3 connects the top plate of \( C \) to \( V_{in}^+ \), and the signal voltage across \( C \), which is equal to \( (V_{in}^+ - V_{in}^-) \) is amplified by the inverter. Fig. 21b and c shows the dynamic measurement results of the comparator at 50 Hz and 20 Hz clock frequency and for different input values \( (V_{in} = V_{in}^+ - V_{in}^-) \). This simple comparator is able to detect input signals as small as 200 mV, as shown in Fig. 21c. This is a considerable performance for a printed circuit, and it has been enabled by the use of the pass-gates available in our complementary technology.

### 4. Conclusion

We have developed a printed organic complementary technology on flexible plastic substrate, compatible with large-area printing processes. Both P- and N-OTFTs are processed with small-molecule organic semiconductor solutions. The P-OSC layer crystallization has been optimized as well as the injection SAM of the N-OTFTs to increase the mobility. Several challenges related to the integration of both P- and N-type OTFTs in a common flow have been addressed. In particular, the importance of the surface treatment between the N- and P-OSC deposition has been demonstrated. Our organic complementary technology exhibits state of
the art electrical performance and stable electrical characteristics, with a yield going from 98% to 100% for both P- and N-OTFTs, depending on the chosen criterion. Several digital and analog circuits have been processed with this technology on plastic sheets and demonstrate the capability of this technology to enable organic electronic applications. Measurements of a ring oscillator show that switching frequencies over the kHz could be achieved. Shelf-lifetime results measured on the oscillator without passivation kept for 6 months in ambient air demonstrates that reaching long term stability with organic electronics is realistic. The frequency dependent measurements of an envelope detector show correct functionality at the HF RFID frequency (13.56 MHz), thanks to the high OTFT mobility. Other circuits including a small-footprint dynamic flip-flop and a 200 mV-offset dynamic comparator are also presented, showing how complementary technology leads to a step forward in improving functionality, yield and robustness to variability. The designed circuits realize a complete building block library for the design of RFID tags with integrated AM receivers. Further work is now needed to develop a low-drop rectifier and integrate all circuits together in order to implement a full RFID tag.

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References

