Abstract—Carbon nanotubes (CNT) can be an attractive candidate for vertical interconnects in 3D monolithic integration, due to their excellent thermal and electrical properties. In this paper we investigate the use of a true bottom-up approach to fabricate CNT vias, for application in 3D monolithic integration. This circumvents metal deposition in high aspect ratio holes, and also allows the use of bundle densification techniques to increase CNT density. Using this approach we fabricated four-point probe electrical measurement structures for both as-grown and densified CNT bundles, and performed I-V measurements. The resulting I-V curves display non-linearities due to a non-Ohmic top contact. The measured resistivities of 10-20 mΩ·cm are among the better values found in literature.

I. INTRODUCTION

Three dimensional integration can offer high integration density, shorter routing and increased functionality by combining for instance sensors and logic. Of the different approaches that exist for 3D integration, monolithic (device-level) integration offers the highest integration density and shortest interconnect length. In this approach transistor layers are stacked on top of each other on the same die across the entire wafer.

Many challenges still remain to be solved in order to achieve monolithic integration. One of the biggest is creating the active silicon layers. Our group has previously been working on monolithic integration using single-grain thin-film transistors (SG-TFTs) [1]. These transistors offer silicon-on-insulator (SOI) level performance, while processing temperature remains below 550 °C. Using two layers of transistors we demonstrated memory circuits and combined image sensor with read-out [2].

Two other major remaining challenges are manufacturing reliable low resistance vertical interconnects and thermal management. Already in modern circuits vertical interconnects (vias) display many reliability issues due to difficulties in filling the small openings. For monolithic integrated circuits we can expect these issues to be worse, as the oxide required to isolate the different active layers is relative thick. Thermal management is an issue as the amount of transistors is increased drastically, while the surface area of the die remains roughly the same.

Carbon nanotubes (CNT) can be an attractive candidate to tackle both issues. It has been shown that CNT can have unrivalled electric properties, allowing ballistic transport over a length of several µm [3], [4]. Moreover, CNT have been demonstrated to have very good reliability properties, allowing a current density up to three order of magnitude higher than copper [5]. Beside good electrical properties CNT can be grown with very high aspect ratios. Finally, CNT have been demonstrated to possess very good thermal properties with thermal conductivities reaching 3500 W/mK [6]. Much interest has already been shown in using CNT as vias for regular 2D integrated circuits [7]–[10].

We propose to use CNT as via material in monolithic integrated 3D circuits. For this a bottom-up approach as suggested by Li et al. [11] should be most suitable. In this approach the CNT are grown before the deposition of the dielectric layer, thus circumventing all the issues involved in filling high aspect ratio holes. As CNT can be grown vertically well aligned integration density can be high.

In this paper we created low-temperature and high density multi-walled CNT (MWCNT) using this bottom-up approach and performed electrical resistance measurements. Moreover, we investigated the use of a bundle densification technique in order to reduce via dimensions and resistivity by increasing the CNT tube density.

II. EXPERIMENTAL

As substrate 4” p-type Si wafers with (100) are used. These wafers are metallized using a Trikon Sigma sputter coater with 500 nm of Ti and 50 nm TiN, which acts as bottom contact to the CNT bundles. TiN is used as this is a standard barrier material in the IC industry, doesn’t oxidise during wafer transfer between machines (for catalyst deposition) and allows the growth of vertically aligned MWCNT at low temperatures in our CNT growth reactor.

Next a 5 nm thick Fe catalyst layer is deposited using an CHA Solution e-beam evaporator and patterned using lift-off. For this lift-off process we employ AZ nLOF pure negative resist, which is exposed by an ASML PAS 5500/80 waferstepper. The actual lift-off is performed in n-methyl pyrrolidone.
at 70 °C. After this CNT are grown using the commercially available AIXTRON BlackMagic Pro CNT reactor. The first phase of the growth process consists of a activation step with 700 sccm of H₂ for 3 min. at 500 °C and 80 mbar. After this 50 sccm of C₂H₂ is added to start the CNT growth phase. Total growth time equals 15 minutes.

After CNT growth 5 μm of PECVD oxide is deposited using a Novellus Concept One reactor at 400 °C. Before performing this step the CNT of some of the wafers are densified using isopropanol. Oxide deposition is followed by planarization using chemical mechanical polishing (CMP) with a silica slurry. A total of approximately 1 μm of oxide is removed in this process. Finally, the second electrode consisting of 100 nm of Ti and 2 μm of Al(1% Si) is deposited and patterned using wet etching. Finally, contact holes are etched through the oxide in order to contact the first electrode directly. In fig. 1 an overview is given of the bottom-up process. Samples were characterised using an FEI/Philips XL50 scanning electron microscope (SEM) and Agilent 4156C parameter analyser.

III. RESULTS AND DISCUSSION

In fig. 2a a SEM image taken from an array of five by five 2 μm wide CNT bundles with a spacing of 3 μm and height of roughly 5 μm. As can be observed the CNT and bundles display good vertical alignment. Fig. 2b displays a single 2 μm wide bundle with a length of almost 10 μm, demonstrating the ability to grow high aspect ratio (HAR) free standing bundles. The density of the CNT inside the bundles is ~10^{11} tubes/cm², while the average tube diameter is 5-15 nm. The CNT tube length can be changed by varying the deposition time, which has a linear dependency against length, with a growth rate of 350 nm/minute.

We use PECVD oxide as it can be deposited at low temperatures. Previously, we reported that we didn’t observe a major degradation in tube crystallinity due to plasma damage while depositing the oxide [12]. The CNT are uniformly covered by the PECVD oxide, as can be seen in fig. 2c. It can also be clearly seen that CMP is required to be able to contact the top of the CNT bundles.

Finally fig. 2d displays the array of CNT after approximately 1 μm of oxide was removed using CMP. As can be seen the CNTs are cut-off at the same height as the oxide. Gaps can exist between CNT bundles spaced closed to each other, due to a non optimized PECVD oxide deposition process. Decreasing deposition rate likely solves this issue. As shown in fig. 2e in some larger CNT bundles cracks appear with a width of several hundred nm, which are caused by the non-optimized CMP process.

It must also be noted that we encountered difficulties in polishing large bundles with widths of 6 μm or wider. Most of these bundles are removed during CMP, which we attribute to mechanical removal during the CMP step as the substrate adhesion of CNT is generally low [13]. The bundles are only covered on the outside by the PECVD oxide. Embedding the CNT in a layer of atomic layer deposited dielectric, as demonstrated by Chiodarelli et al. [14], to increase mechanical stability could circumvent this problem and the formation of cracks in large bundles.

Although the density of our bundles is relative high, it is still orders of magnitude lower than ideal tight packing in which case density can be as high as 10^{13} − 10^{14} tubes/cm². It has been demonstrated that CNT density can be increased by dipping the tubes into isopropanol [15]. This densification is caused by the capillary forces of the liquid combined with strong Van der Waals interaction between the tubes upon liquid
evaporation.

We employed this technique by simply dipping the full wafers upside-down into an isopropanol bath, followed by drying of the wafers in air. As can be from fig. 3 the width of the resulting bundles are 72 % and 74 % of the initial width for the 2 µm and 5 µm bundle, respectively. This is representative for all bundle sizes over the entire wafer. The resulting area after densification is thus almost 50 % of the initial bundle area, drastically reducing the footprint of the top CNT bundle contact. The bottom contact remains the same, due to the strong enough surface adhesion of the CNT. The tip of the CNT bundle is less densified, but conveniently removed during the CMP process.

We created four-point probe measurement structures using this bottom-up process to measure the resistance of the CNT bundles. Using the top and bottom electrode contacts a current could be forced through the bundle, which could be current-less measured using two different top and bottom contacts. Using this structure only the resistance of the CNT bundle, and the contact resistances to the top and bottom electrode are measured. A sketch of the measurement structure can be found in the inset of fig. 4.

Fig. 4 displays typical I-V characteristics obtained from several bundles with a width of 1 µm and a length in between 3.8 and 4 µm. As can be seen there exist a non-linear component in the measured I-V curves. This is most likely caused by a non-Ohmic contact. We suspect the top contact, as the bottom contact should still be similar to those used for top-down results reported earlier by our group, which didn’t suffer from any non-linearities [12]. These non-linearities are also visible for bundles with a width of 2 and 4 µm, which have a larger contact areas. Improving the CMP conditions, or removing part of the silicon oxide to expose the CNT tips could improve the top contact. Annealing might also solve the problem, although we found that annealing the wafers in a nitrogen atmosphere at 400 °C actually degraded the resistance.

From the five best performing structures we determined the average resistivity and standard deviation using the approximate dimensions of the CNT bundle. The same was done for the densified bundles, assuming a final width of 75 % of that of the initial width (1.5 and 3 µm for, respectively, the initially 2 and 4 µm bundles). The resulting resistivities are plotted in fig. 5 together with results obtained by top-down integration performed before in our group and results taken from literature about CNT vias for 2D integrated circuits.

As can be seen the results are among the better values reported in literature, although still many orders of magnitude higher than the bulk resistivity of for instance Cu. For small bundle sizes the resistivity increases sharply for the as-grown CNT bundles. We suspect that the top contact is the cause of this deviation for these bottom-up results. This is because the measurement results of the densified 2 µm bundle are much better, which also display hardly any non-linearities in the I-V characteristics indicating better contact. The CMP processed used for the densified and non-densified bundles differ, for the latter it was done with a pH 7 slurry, while the first uses the standard slurry. Making the slurry pH neutral resulted in much longer polish times, likely wearing down the tips of the tube resulting in a higher contact resistance.

For the larger 4 µm bundles the resistivity spread is much larger, which could be caused by the before mentioned cracks observed in some of the larger structures. Overall, although a different CMP approach was used, the values between densified and non-densified bundles are not for apart. The obtained values using bottom-up integration are close to those reported before using the same CNT growth recipe, but a top-down approach [12]. For the larger and densified bundles the resulting resistivities are even lower. This confirms that the bottom-up approach does not degrade CNT quality. The higher resistivities measured can be attributed to a higher top-contact resistance, which can be improved by optimizing the CMP parameters.

IV. Conclusion

Carbon nanotubes can be an attractive candidate for vias in 3D monolithic integration due to their good electrical and thermal properties. We demonstrate, for the first time, that it is possible to use a pure bottom-up approach using carbon
nanotubes to create vias. With this approach it is possible to use bundle densification techniques, which decrease the top area of the via. Four-point probe I-V measurements were performed for both densified and non-densified bundles, displaying a non-linear resistance due to a non-Ohmic top contact. The measured resistivities of 10-20 mΩ-cm are among the better values reported in literature.

ACKNOWLEDGMENT

The authors want to thank T.M. Michielsen, F.J.H. van der Kruis and O.J.A. Buijk at Philips Innovation Services MiPlaza for performing the CMP. This project is kindly funded by the European ENIAC Joint Undertaking as part of the JEMSiP_3D project.

REFERENCES
