Design and analysis of a multiple-output transmitter based on DDS architecture for modern wireless communications

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Abstract. Multiple – output transmitter implementation based on Direct Digital Synthesis (DDS) architecture is presented and investigated. A particular number of identical and independent units compose the proposed device. DDS technology is applied on the first stage of these units and provides amplitude, phase and frequency adjustments on the corresponding output signals. Quadrature mixers are driven by DDS’s outputs and corresponding amplification and filtering circuits are also used to prepare the radiofrequency signals in the outputs of the proposed device. Design issues of analog circuitry and digital control logic are also described. Phase, amplitude and frequency accuracy that DDS technology provides are further discussed. Experimental results indicate that the proposed transmitter architecture can provide independent RF signals for wireless applications.

Keywords: direct digital synthesis, quadrature mixer, phase progress, standard deviation

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1. INTRODUCTION

Direct Digital synthesis (DDS) techniques offer efficient and practical methods providing configurable transmitter architectures suitable for modern wireless applications \cite{3, 4, 5}. Amplitude, frequency and phase accuracy and adjustability are the crucial characteristics of this architecture that provide the performance of the proposed multi –channel transmitter implementation.

This implementation and its performance are presented and investigated. Theoretical considerations on digital beamforming aspects (DBF) are further discussed as provided by the proposed circuitry. Phase accuracy is the basic parameter that is studied and investigated. This design and analysis procedure is based on DDS devices. Each of these parts generates an independent modulated signal at a programmable intermediate frequency. Amplitude and initial phase adjustability are also offered by this architecture. A common master clock signal drives these devices and further synchronization aspects are taken into account for efficient performance of the proposed implementation.

Besides, a personal computer controls each dds circuitry, providing programming and initialization procedures. Up – conversion and amplification circuitry are driven by these programmable signals in order to feed antenna radiation elements on wireless communications systems.

In this study the fundamental characteristics of DDS architecture are presented, firstly at Section 2. In Section 3, theoretical analysis of phase progression and direction of transmission on digital beamforming applications (DBF) are treated and discussed. Design, implementation and performance aspects are included in Section 4; the paper concludes in Section 5.
2. FUNDAMENTALS OF DDS

The multiple-output transmitter circuitry that is proposed in the current paper is based on DDS technology. Principles and practices that are provided by this technology are also revealed by the corresponding definition. According to DDS theory, this circuitry generates a sine wave signal with programmable frequency, amplitude and phase. Its performance of the circuit is based on the stability of the reference clock signal $f_C$ [4, 5, 6]. Further details on this circuitry are depicted in Figure 1.

This schematic diagram shows the inner parts of DDS architecture, including phase accumulator, phase–to–amplitude mapping circuit and digital–to–analog converter (DAC). The output of the last device is fed to an external low pass filter. The corresponding output of filter provides the output signal $f_0$. In order for this system to work properly, some critical parameters need to be defined. These are the frequency tuning word $M$, the system reference clock rate $f_C$, the phase accumulator resolution $N$ (bits) and the output amplitude resolution $B$. The whole performance of the device that is presented in Figure 1 is based on the corresponding units of the block diagram and these crucial parameters. In particular, the phase accumulator acts like a modulus $M$ counter. For each receiving pulse of the system reference clock this unit increments its stored number by the value of $M$. This procedure goes on until the phase accumulator overflows. It is then clear that an increase of $M$ leads to a reduction to the time interval before overflow. On each overflowing event the equivalent sine wave cycle is also completed. The second unit of diagram in Figure 1 presents the phase-to-amplitude converter that is driven by the output parameter $K$ of the phase accumulator. This value corresponds to an address in the core of the phase–to–amplitude converter random access memory (ROM). A new location of this memory is accessed during each clock period. The output frequency $f_0$ depends thus on $M$ and $N$ that are DDS fundamental parameters according to the following mathematical expression. This programmable value is also related to $f_C$ the frequency of the system reference clock signal. Equation 1 represents the corresponding mathematical expression.

$$f_0 = M \cdot \frac{f_C}{2^N}$$

From this equation it seems that the variable $f_0$ is specified by the values of parameters $M$, $f_C$ and $N$. The last variable $N$ determines also the minimum frequency resolution which is equal to $f_C / 2^N$. Besides, the corresponding minimum phase resolution is based on $K$ parameter and equals to $2 \cdot \pi / 2^K$ radians. These considerations on DDS architecture are referred to the importance of $K$ and $N$ parameters for this circuitry performance. The values of them provide accurate adjustments on frequency and phase of the output signal. Complete digital control provides the corresponding sub Hertz tuning resolution and sub-degree phase resolution. This feature can be considered as the corner stone of the DDS architecture and performance.

Another crucial feature of this architecture is sampling speed limitation that affects the output signal bandwidth. In particular, DDS core and its Digital–to–Analog converter features limit the bandwidth of the output signal [4, 5, 6]. This crucial value has to be lower than half the sampling frequency, which equals to system reference clock frequency. Many methods employed to overcome this undesirable feature and most of them suggest multiple PLL’s, frequency mixer and oscillator stages. The last method is implemented in the proposed transmitter structure. It
manages to overcome the corresponding limitation on signal’s bandwidth and also offers quite excellent features for modern wireless applications and investigation’s activities.

3. THEORY AND ANALYSIS ON DBF

A major application on wireless communication systems that is provided by the proposed multiple output transmitter architecture is digital beamforming. This technique combines antenna array configurations and digital processing concepts [1, 2].

Antenna array, multiple output digital transmitter and digital signal processor are the three major components of a generic DBF system. The corresponding antenna elements needed to transmit the output power are placed in an arrangement that defines the radiation pattern of the array. Figure 2 shows an n elements linear array. The distance d between the antenna elements is predefined.

![Uniform linear antenna array with n elements.](image)

Based on the array configuration that depicted in Figure 2 and the specific characteristics (phase shifts, amplitude adjustments) of each of $x_n$ signals feeding the antenna element, one can define the radiation diagram of the system. For the case of simplicity, we assume that the main beam must be steered at an elevation angle $\phi$. In this case, the signals that feed two sequential elements must be phase shifted by $\beta$. This parameter is usually referred as a phase progression. A mathematical expression for $\beta$ is provided by equation 2.

$$\beta = 2\pi f \frac{d \cos \phi}{c}$$

(2)

In this equation, $c$ is the speed of the light and $f$ the carrier frequency of the signal that feed each of antenna elements. This formulation combines the uniform linear antenna array arrangement with a corresponding number of RF signals which is phase shifted by parameter $\beta$, sequentially [1, 2]. In particular, this procedure proposes an efficient estimation method that estimates the steering angle of the main beam in a defined antenna array configuration. The accuracy in approximation procedure of $\phi$ is based on corresponding accuracy of $\beta$ and d parameters [3]. Theory of error propagation defines that the standard deviation of parameter $\phi$ ($\sigma_{\phi}$) is related to the corresponding standard deviation of parameters $\beta$ ($\sigma_{\beta}$) and $d$ ($\sigma_d$). Mathematical expressions that based on equation (2) and lead to mean value and standard deviation of variable $\phi$ ($\sigma_{\phi}$) is provided by the following equations:

$$\phi = \arccos\left(\frac{\beta c}{2\pi df}\right)$$

(3)

$$\sigma_{\phi} = \sqrt{\left(\frac{\partial \phi}{\partial \beta} \cdot \sigma_{\beta}\right)^2 + \left(\frac{\partial \phi}{\partial d} \cdot \sigma_d\right)^2}$$

(4)

The equations above express the mean value $\phi$ and standard deviation $\sigma_{\phi}$ of estimated steering angle of main beam for defined parameters of $\beta$, d, and f. The $\frac{\partial \phi}{\partial \beta}$ and $\frac{\partial \phi}{\partial d}$ are the derivatives of variable $\phi$. 

423
This calculation procedure requires knowledge and definition of the corresponding variables and parameters. In this study, the standard deviation of parameter \( d \) (\( \sigma_d \)) is approximately 0.5 mm. Besides, DDS architecture suggests that the corresponding standard deviation of parameter \( \beta \) is approximated to half the smallest phase step in the programming procedure. The corresponding phase accuracy is defined as 0.022 degrees and is specified by the crucial parameters of DDS that has been presented, above. In our configuration the parameter \( d \) equals to 62.5 mm that is the half of wavelength corresponding to a frequency of 2.4 GHz. These considerations and calculated results for main beam angle \( \phi \) are included in Table 1 for four representative situations.

### TABLE 1. Estimated results of main beam angle. \( d = 0.0625m \), \( \sigma_d = 0.0005m \), \( \sigma_\beta = 0.0002rad \)

<table>
<thead>
<tr>
<th>Phase progression ( \beta ) (rad)</th>
<th>Angle of main beam ( \phi ) (rad)</th>
<th>Standard deviation of ( \phi ), ( \sigma_\phi ) (rad)</th>
<th>Angle of main beam ( \phi ) (degrees)</th>
<th>Standard deviation of ( \phi ), ( \sigma_\phi ) (degrees)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5453</td>
<td>1.3960</td>
<td>0.001</td>
<td>80.02</td>
<td>0.06</td>
</tr>
<tr>
<td>1.0905</td>
<td>1.2160</td>
<td>0.003</td>
<td>69.7</td>
<td>0.2</td>
</tr>
<tr>
<td>1.6357</td>
<td>1.0230</td>
<td>0.005</td>
<td>58.6</td>
<td>0.3</td>
</tr>
<tr>
<td>2.1810</td>
<td>0.8030</td>
<td>0.008</td>
<td>46.0</td>
<td>0.5</td>
</tr>
</tbody>
</table>

This table and the corresponding values of parameters that are calculated leads to very interesting observations and conclusions. Table 1 also includes the values of parameters \( \phi \) and \( \sigma_\phi \) in rads. As we can see, every calculated standard deviation of parameter \( \phi \) is less than half of a degree. Besides, as the value of parameter \( \beta \) increases, the corresponding parameter \( \sigma_\phi \) increases but remains quite small. From these considerations it is convenient that the proposed multiple transmitter structure provides sufficient phase accuracy, which seems to be quite excellent for DBF applications.

### 4. DESIGN AND PERFORMANCE ASPECTS

The architecture of the proposed multiple-output transmitter is based on DDS circuitry and its basic characteristics. This also comprises several identical units that operate synchronously and manage to feed the elements of an antenna array configuration. Figure 3 depicts this basic design concept.

![FIGURE 3. Transmitter architecture with \( n \) units.](image)
Figure 3 shows that this implementation includes a defined number of identical units in which DDS circuitry is the first stage on them and provides the output signal $f_0$. In particular, each DDS core provides two outputs signals with frequency $f_0$, the in-phase and the quadrature components. These output signals drive a quadrature modulator for up-conversion purposes. The necessary frequency ($f_{LO}$) up-converts the signal $f_0$ to the appropriate frequency for transmission $f_{RF}$ [7, 9-12]. There is also a special requirement of a power splitter that distribute the local oscillator signal to each input of the $n$ quadrature modulator used in the proposed transmitter design. The outputs of the quadrature modulators are amplified and filtered, before transmission. Preparation procedure of RF signal combines appropriate amplification circuits and filter devices. The corresponding power of the output signal on each of the identical units in the transmitter is measured to be 14 dBm.

As said before the performance of the proposed architecture is based on the system reference clock precision and the control unit characteristics. Each DDS core is supported by an external clock at 10 MHz which is multiplied by a factor of 18 [7, 8]. This procedure provides a stable reference clock signal in each DDS device equivalent to 180 MHz. This way, the bandwidth of the signal in DDS’s output is limited to 90 MHz. Control unit adjusts the corresponding parameters on DDSs’ performance. In particular, amplitude of DDS’s output signal is adjusted with great accuracy by the 12-bit corresponding register. DDS core has also programmable 48-bit frequency register that offers quite excellent frequency accuracy in order of 0.64uHz. The corresponding phase accuracy is provided by the 14-bit register [4, 5, 6]. These features of the above architecture become more efficient and useful, if design aspects on the proposed implementation ensure that DDS circuits operate, synchronously [8]. This requirement is very crucial for transmitter performance. Figure 4 depicts the corresponding design concepts that are suggested to provide synchronous performance of all units in the multiple-output transmitter implementation.

The proposed architecture that ensures synchronized operation of DDS circuits provides the corresponding requirement of the multiple-output transmitter design. An appropriate circuit interface, a reference clock generator and many digital parts are combined to form this proposed structure. The I/O Update Clock signal drives the corresponding pin of each DDS device, simultaneously. This flag activates these devices in order to generate their output signals. Frequency, amplitude and initial phase of each DDS output signal are specified by the defined values in the corresponding programmable registers.

For every change of $f_0$ signal, an update signal is necessary. The time needed from the update signal up to the change in the output, a time interval ($\Delta t$) is elapsed. This accuracy of the ($\Delta t$) is investigated in each DDS output. Measured results indicate that this time interval is strictly depended on DDS architecture.

The requirement on synchronous operation of DDS devices combined with the corresponding features of DDS’s architecture ensures that the proposed implementation may offer interesting and efficient futures for modern wireless...
applications. System reference clock, digital control unit, programmable frequency, amplitude and phase of the DDS output signal are the crucial characteristics of the proposed structure. Figure 5 depicts a group of four output signals that provides phase progression of 60 degrees and has also a defined amplitude progression. This phase progression provides a steering elevation angle of 70 degrees for the main beam of a linear antenna array with equally spaced antenna elements at distance \( d \) equals to half the corresponding wavelength.

**FIGURE 5.** Output signals at the transmitter ports 1, 2, 3 and 4 showing amplitude and phase differences.

The last feature is presented as an amplitude level sequential decrement from output 1 to output 4. The corresponding theory on Digital beamforming systems indicate that in case of amplitude and phase control, the main beam angle is directed to the predefined direction and also the side – lobes’ levels decreases [1, 2]. For these reason, controlling both phase and amplitude is very crucial for DBF applications.

## 5. CONCLUSION

Multiple –output transmitter architecture has been studied and investigated. DDS technology provides its performance for modern wireless applications and DBF systems, especially. The operation of the proposed system has been further investigated in terms of frequency, amplitude and phase accuracy. Theoretical analysis on digital beamforming systems indicates that the proposed implementation offers quite excellent estimation of main beam angle. The corresponding value of standard deviation is approximated close to half of angle degree. Synchronization aspects of the proposed transmitter architecture are also presented and discussed. In conclusion, this design offers versatile and efficient features that support antenna array feeding performances and modern wireless applications.

## REFERENCES