Versatile energy recovery circuit for driving AC plasma display panel with single sustain circuit board

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Received 12 November 2005; received in revised form 9 March 2006; accepted 17 May 2006
Available online 9 June 2006

Abstract

This paper presents an energy recovery (ER) circuit which can operate either in a series or a parallel resonance mode and can drive an AC plasma display panel (PDP) with a single sustain circuit board. The proposed ER circuit consists of one energy storage capacitor, two energy recovery inductors, and three insulated-gate bipolar transistors. The circuit operations in the series and parallel resonance modes are similar to conventional ones, except for the leading edge of the first sustain pulse and the trailing edge of the last sustain pulse. To reduce power consumption in the parallel resonance mode of operation, these two pulse edges are generated using a series resonance between the panel capacitance and the energy recovery inductor. The proposed circuit had energy recovery efficiencies in both the series and parallel resonance modes that were nearly the same as the efficiency of the conventional series resonance ER circuit. Experimental results on a 42-inch XGA single-scan PDP show that the proposed ER circuit is suitable for use in a PDP drive circuit.

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Keywords: Energy recovery circuit; Series/parallel resonance; Power efficiency; Sustain circuit; Plasma display panel (PDP)

1. Introduction

The power consumption of an AC plasma display panel (AC PDP) occurs mostly in the sustain discharges. The major current supplied to the PDP for sustain discharge is a displacement current because two sustain electrodes, the scan (S) and common (C) electrodes, are separated from the discharge gap by an insulator. Accordingly, the PDP has been modeled with a capacitor $C_p$ to analyze behavior of sustain drive circuits [1,2]. The simplest full-bridge type of sustain drive circuit is shown in Fig. 1 [3]. It consists of four MOSFET switches only, and its operation consists of three switching states: the SUS_UP_S, SUS_DN, and SUS_UP_C states. The SUS_UP_S and SUS_UP_C states generate the sustain pulses for S and C, respectively. When the circuit is driven at a voltage of $V_{sus}$, each sustain pulse charges up the panel with an energy of $C_p V_{sus}^2/2$. The same amount of energy is dissipated in the circuit to charge the panel. At the SUS_DN state, the stored energy is dumped to the ground and the voltages of S and C return to 0 V. Accordingly, the amount of energy dissipated for each pulse is $C_p V_{sus}^2$. If the number of sustain pulses per second is $f$, the power consumption is $C_p V_{sus}^2 f$, which becomes intolerable for a practical AC PDP. Furthermore, high charging and discharging currents cause electromagnetic interference (EMI) and circuit heating problems. To relieve these problems, an energy recovery (ER) circuit has been added to the full-bridge sustain circuit.

To recover the energy stored in the panel, all existing ER circuits use either a series or parallel resonance between the panel capacitance $C_p$ and an energy recovery inductor. Two typical circuit configurations of the ER circuit are shown in Figs. 2 and 3. The series resonance ER circuit shown in Fig. 2 was invented by Weber and adopted by many PDP manufacturers [4,5]. It uses two separate ER circuits for S and C. The energy storage capacitors $C_{ss}$
and $C_{cs}$ are charged initially to a voltage of $V_{sus}/2$. Sustain pulses are generated using seven switching states: the ER_UP_S, SUS_UP_S, ER_DN_S, ER_UP_C, SUS_UP_C, ER_DN_C, and SUS_DN states. The initial state is the SUS_DN state at which the voltages $V_c$ of the C electrode and $V_s$ of the S electrode are at 0 V. The switch $S_2$ remains closed to keep $V_c = 0$ V, while generating a sustain pulse for S. At the ER.UP_S state, the inductor $L_s$ and the panel capacitor $C_p$ form a series resonance circuit and the energy stored in $C_{es}$ are supplied to $C_p$. The voltage $V_s$ of the S electrode reaches $V_{sus}$ at one half of the resonance period. The SUS_UP_S state starting at $t = t_1$ holds $V_s$ at $V_{sus}$. At the ER_DN_S state starting at $t = t_2$, $L_s$ and $C_p$ forms a series resonance circuit and $V_s$ decreases to 0 V at one half of the resonance period. The energy stored in $C_p$ is recovered to the energy storage capacitor $C_{es}$. After all stored energy is recovered, the SUS_DN state starts to hold $V_s$ at 0 V. The subsequent sustain pulse for C is generated using the ER_UP_C, SUS_UP_C, ER_DN_C, and SUS_DN switching states on the energy recovery circuit for C, which operates in the same way as the circuit for S. The circuit shown in Fig. 2 has the advantage of flexible sustain waveform design at the expense of cost because it uses two separate ER circuits.

The parallel resonance ER circuit shown in Fig. 3 was invented by Sakai [6,7]. This circuit uses a parallel LC resonance between $C_p$ and $L_s$. The sustain pulses are generated using the SUS_DN, SUS.UP_S, TRANS_A, SUS_UP_C, and TRANS_B states. At the SUS_DN state, both $V_s$ and $V_c$ are at 0 V. The SUS_UP_S state sets $V_s = V_{sus}$ and $V_c = 0$ V. The first sustain pulse for S is generated using the SUS_UP_S state starting at $t = t_0$. Next, the
TRANS_A state starting at \( t = t_1 \) forms a parallel resonance circuit consisting of \( C_p \) and \( L \), and \( V_s \) decreases to 0 V at one half of the resonance period, while \( V_c \) increases to \( V_{\text{sus}} \). The SUS_UP_C state begins at \( t = t_2 \) after \( V_c \) reaches \( V_{\text{sus}} \) and maintains the voltages \( V_c = V_{\text{sus}} \) and \( V_s = 0 \) V. At \( t = t_3 \), the TRANS_B state starts and \( V_c \) decreases to 0 V, while \( V_s \) increases to \( V_{\text{sus}} \). The sequence of SUS_UP_S, TRANS_A, SUS_UP_C, and TRANS_B is repeated until the last sustain pulse. The last sustain pulse is generated using a sequence of TRANS_A, SUS_UP_C, and SUS_DN states. When compared with the ER circuit shown in Fig. 2, the number of circuit elements required in this circuit is significantly reduced. However, because the energy stored in one electrode is being used to charge up the other, the transitions of voltages for S and C occur simultaneously and it is impossible to adjust the separation between the sustain pulses. Also, a hard switching is unavoidable for the first and last sustain pulses, resulting in an EMI problem and an increase in power dissipation.

The challenging factors in designing the ER circuit have been a reduction of circuit cost and an increase of power efficiency, while increasing the degree of freedom in tuning the sustain waveform. This paper proposes an energy recovery circuit which can recover energy from both the S and C electrodes using a single sustain circuit board. The proposed circuit has high power efficiency and good flexibility in tuning the sustain waveform. The operational principle of the proposed circuit is given in Section 2 and experimental results are given in Section 3. A conclusion is given in Section 4.

### 2. Proposed energy recovery circuit

To overcome the disadvantages of the series and parallel resonance ER circuits, we propose the energy recovery circuit shown in Fig. 4. This circuit consists of a full-bridge circuit composed of S1–S4, one energy storage capacitor \( C_s \), two energy recovery inductors \( L_1 \) and \( L_2 \), three insulated-gate bipolar transistors (IGBTs) S5–S7, and three protection diodes \( D_1–D_3 \). It can operate either in a series or in a parallel resonance mode. The sustain pulses are generated using the following nine switching states: SUS_DN, ER_UP_S, SUS_UP_S, ER_DN_S, ER_UP_C, SUS_UP_C, ER_DN_C, TRANS_A, and TRANS_B switching states. The circuit operation at each switching state is shown in Fig. 5. The SUS_DN state sets \( V_s = V_c = 0 \) V. The SUS_UP_S state sets \( V_s = V_{\text{sus}} \) and \( V_c = 0 \) V, and the SUS_UP_C state sets \( V_s = 0 \) V and \( V_c = V_{\text{sus}} \). The ER_UP_S and ER_DN_S states set \( V_c = 0 \) V and provide the current paths between \( C_s \) and the S electrode. The ER_UP_C and ER_DN_C states set \( V_s = 0 \) V and provide the current paths between \( C_s \) and the C electrode. The TRANS_A and TRANS_B states provide the current paths from the S to C electrode and from the C to S electrode, respectively. Initially, the energy storage capacitor \( C_s \) is charged to a voltage of \( V_{\text{sus}}/2 \).

The sustain waveform for the series resonance mode of circuit operation is shown in Fig. 6(a). It is generated by repeating the following sequence of switching states: SUS_DN, ER_UP_S, SUS_UP_S, ER_DN_S, SUS_DN, ER_UP_C, SUS_UP_C, and ER_DN_C. The initial state is the SUS_DN state at which \( V_s = V_c = 0 \) V. While generating a sustain pulse for S, the switch S2 is closed to keep \( V_s = 0 \) V. At the ER_UP_S state starting at \( t = t_0 \), \( L_1 \) and \( C_p \) form a series resonance circuit and the energy stored in \( C_s \) is supplied to \( C_p \). The voltage \( V_s \) reaches \( V_{\text{sus}} \) at one half of the resonance period. The SUS_UP_S state starts at \( t = t_1 \) and maintains \( V_s = V_{\text{sus}} \). The ER_DN_S state starts at \( t = t_2 \) and recovers the stored energy in the panel capacitor \( C_s \) using \( L_1 \) and \( C_s \). Again, \( L_1 \) and \( C_p \) form a series resonance circuit and \( V_s \) decreases to 0 V at one half of the resonance period. The stored energy in \( C_p \) is recovered to \( C_s \). After all stored energy is recovered, the SUS_DN state starts at \( t = t_3 \) to maintain \( V_s = 0 \) V. Next the switching states for generating a sustain pulse for C begin at \( t = t_4 \). During all switching states for C, the switch S4 is closed to keep \( V_s = 0 \) V. At the ER_UP_C state starting at \( t = t_4 \), \( L_2 \) and \( C_p \) form a series resonance circuit. The energy stored in \( C_s \) is supplied to \( C_p \) and \( V_s \) reaches \( V_{\text{sus}} \) at one half of the resonance period. The SUS_UP_C state starts at \( t = t_5 \) and maintains \( V_s = V_{\text{sus}} \). The ER_DN_C state starts at \( t = t_6 \) and recovers the stored energy in \( C_p \) using \( L_2 \) and \( C_s \). After all stored energy is recovered, the SUS_DN state starts at \( t = t_7 \) to keep \( V_s = 0 \) V, completing one cycle of sustain pulses.
The sustain waveform for the parallel resonance mode of circuit operation is shown in Fig. 6(b). It is generated using the following switching states: SUS_DN, ER_UP_S, SUS_UP_S, TRANS_A, SUS_UP_C, TRANS_B, and ER_DN_C switching states. The initial state for a train of sustain pulses is the SUS_DN state. The first sustain pulse for S is generated using the ER_UP_S state starting at \( t = t_0 \) while keeping \( V_c = 0 \) V. At this state, \( L_1 \) and \( C_p \) form a series resonance circuit, the stored energy in \( C_s \) is supplied to \( C_p \), and \( V_s \) increases to \( V_{sus} \) at one half of the resonance period. The SUS_UP_S state starts at \( t = t_1 \) and maintains \( V_s = V_{sus} \). Next, the TRANS_A state starting at \( t = t_2 \) forms a parallel resonance circuit consisting of \( L_1, L_2, \) and \( C_p \). The voltage \( V_s \) decreases to 0 V at one half of the resonance period, while \( V_c \) increases to \( V_{sus} \). The SUS_UP_C state starts at \( t = t_3 \) after \( V_c \) reaches \( V_{sus} \) and maintains \( V_c = V_{sus} \) and \( V_s = 0 \) V. The TRANS_B state starting at \( t = t_4 \) increases \( V_c \) to \( V_{sus} \) and decreases \( V_c \) to 0 V at one half of the resonance period. The sequence of SUS_UP_S, TRANS_A, SUS_UP_C, and TRANS_B is repeated until the last sustain pulse. The last sustain pulse is generated using the TRANS_A and SUS_UP_C states, and then the energy stored in the panel is recovered using the ER_DN_C state starting at \( t = t_5 \). At the ER_DN_C state, \( C_p \) and \( L_2 \) forms a series resonance circuit and the stored energy in \( C_p \) is recovered to \( C_s \). After all stored energy is recovered, the SUS_DN state starting at \( t = t_6 \) keeps \( V_s = V_c = 0 \) V.

As discussed above, the proposed ER circuit structure can operate both in series resonance and in parallel resonance modes. Unlike the conventional series resonance ER circuit shown in Fig. 2, the proposed circuit combines the S and C sustain circuits into a single circuit and reduces the number of required circuit elements without sacrificing
the advantages of the conventional series resonance ER circuit. The parallel resonance ER circuit shown in Fig. 3 uses a hard switching at the first and last pulses, and the energy stored in the panel by the last sustain pulse is dumped to the ground. In the proposed ER circuit, the energy for the first sustain pulse is supplied from $C_s$ and the energy stored in the panel by the last sustain pulse is recovered to $C_s$. Although the proposed circuit uses more circuit elements than the conventional parallel resonance ER circuit, it increases the efficiency of energy recovery and reduces the EMI problems by eliminating hard switching. Accordingly, it is expected that the proposed circuit can be used to drive a PDP with a single sustain circuit board.

3. Experimental results and discussion

The proposed circuit was implemented using the following components: IRF 740 FETs from International Rectifier Co. Ltd for the switches $S_1$–$S_4$, FSGH80N60 IGBTs from Fairchild Semiconductor Co. Ltd for the switches $S_5$–$S_7$, SF20L60U diodes from Shindengen Electric Co. Ltd for the protection diodes $D_1$–$D_3$, and two air core inductors $L_1$ and $L_2$. The IGBT switch has a built-in fast recovery diode. The capacitance $C_s$ was 47 μF. The inductances $L_1$ and $L_2$ were 0.3 μH. The panel capacitance $C_p$ was 0.1 μF.

The measured sustain waveforms of the proposed circuit operating in the series and parallel resonance modes are shown in Figs. 7(a) and (b), respectively. For this measurement, the panel was replaced with a 0.1 μF capacitor to eliminate the effects of discharge on the waveform. The rising time, top-width, and falling time of each pulse in Fig. 7(a) were 0.54, 2, and 0.54 μs, respectively, and the interval between the S and C pulses was 1.92 μs. In Fig. 7(b), these values were 0.54, 4.22, and 0.78 μs for the first pulse, 0.78, 4.22, and 0.54 μs for the last pulse, and 0.78, 4.22, and 0.78 μs for all other pulses. Figs. 7(a) and (b) show that the circuit operated well in both the series and parallel resonance modes of operation. Also, the waveform shown in Fig. 7(b) for the parallel resonance mode had no hard switching pulses because the circuit was operating at series resonance mode for the leading edge of the first pulse and the trailing edge of the last pulse.

The energy recovery efficiency (ER efficiency) for the proposed ER circuit at $V_{sus} = 200$ V was measured using ten pulse trains per one frame time of PDP, which is 1/60 s. The number $N_{sus}$ of sustain pulses for each pulse train was varied from 10 to 120. For comparison, the ER efficiencies for the conventional circuits shown in Figs. 2 and 3 were also measured at $V_{sus} = 200$ V. The ER efficiency $E_r$ is given by

$$E_r = \left(1 - \frac{P_{\text{diss}}}{P_{\text{sus}}} \right) \times 100(\%),$$

where $P_{\text{diss}}$ and $P_{\text{sus}}$ represent the power consumptions of the sustain driver with and without the ER circuit, respectively. Because $C_p = 0.1$ μF, $V_{sus} = 200$ V, and...
f = 12–144 kHz for the experiment, the power $P_{\text{sus}}$ supplied to the panel was $C_p V_{\text{sus}}^2 f = 48–576 \text{ W}$. The measured power consumptions and ER efficiencies versus $N_{\text{sus}}$ for different circuits are shown in Figs. 8(a) and (b). Fig. 8(a) shows that the power consumption $P_{\text{diss}}$ increases with an increase of $N_{\text{sus}}$ for all circuits. The measured $P_{\text{diss}}$ at $N_{\text{sus}} = 30$ were 12 and 11.6 W for the proposed circuit in the series and parallel modes, respectively, and 12.2 and 15.4 W for the conventional series and parallel resonance ER circuits. At $N_{\text{sus}} = 120$, the measured $P_{\text{diss}}$ increased to 82.3 and 78.8 W for the proposed circuit in the series and parallel modes, and to 82.8 and 82.4 W for the conventional series and parallel resonance ER circuits. At any $N_{\text{sus}}$, the ER efficiency $E_r$ for the proposed circuit in the series resonance mode was nearly the same as the one for the conventional one, as shown in Fig. 8(b). The proposed circuit in the parallel resonance mode had nearly the same $E_r$ as the series resonance mode, while, at $N_{\text{sus}} \leq 50$, the conventional parallel resonance ER circuit had a significantly decreased $E_r$ because the energy of the last pulse at each train of sustain pulses was dumped to the ground.

Besides the ER circuit, reset, scan, address, erase pulse generators are required to drive an AC PDP. A full PDP drive circuit was designed and fabricated to check the compatibility of the proposed ER circuit with other circuits. The PDP for a full circuit test was a 42-inch XGA (1024 × 768 pixels) single-scan AC PDP from LG Electronics Inc. The panel capacitance $C_p$ of this PDP was 0.1 µF. The experiment was performed using a typical drive waveform for an AC PDP, which was invented by Matsushita Electric Industrial Co. Ltd. [8] and adopted by many PDP manufacturers. Photographs of the full drive circuit and the displayed image are shown in Fig. 9. The drive circuit consists of S/C drive, scan, data, and control boards, as shown in Fig. 9(a). The S/C drive board generates the setup, setdown, scan, sustain, erase, and bias pulses for S and C electrodes. A copper bus connects the S/C drive board to the C electrodes. The video pattern for Fig. 9(b) was generated using a VG-825 pattern generator from Astrodesign Inc. The number of sub-field for one field of picture was ten. The number of sustain pulses for one field of picture was varied using the average picture level (APL) method [9]. For the experiment, the number of sustain pulses for one field of picture was 382 for a displayed pattern, 260 for a full-white pattern and 1244 for a full black pattern.

While displaying the picture shown in Fig. 9(b), the drive waveform was measured and the results are shown in Fig. 10. The waveform consists of four basic sequences: resetting, addressing, sustaining, and erasing PDP cells. The voltages of the waveform were $V_{\text{sus}} = V_{\text{sr}} = 200 \text{ V}$, $V_r = 380 \text{ V}$, $V_{\text{sb}} = 0 \text{ V}$, and $V_{\text{sc}} = 100 \text{ V}$. The durations of the set-up and set-down periods were 160 and 150 µs.

Fig. 8. The measured (a) power consumptions and (b) ER efficiencies versus $N_{\text{sus}}$ for the proposed circuit in the series and parallel resonance modes, and for the conventional series and parallel ER circuits.

Fig. 9. (a) Picture of a full drive circuit for a 42-inch XGA single-scan PDP and (b) an image displayed using the S/C board with the proposed ER circuit.
The ramp rates for the set-up and set-down voltage ramps were 1.5 and \(-1.43\) V/\(\mu\)s, respectively, and the one for the erase pulse was 10 V/\(\mu\)s. The voltage for data pulses was 75 V. The pulse widths were 1.2 \(\mu\)s for the scan and data pulses, 20 \(\mu\)s for the erase pulse, 10 \(\mu\)s for the first sustain pulse, and 2.5 \(\mu\)s for the other sustain pulses. The pulse transition times at the leading and trailing edges of the sustain pulses were 0.54 \(\mu\)s for the series resonance mode, and 0.78 \(\mu\)s for the parallel resonance mode. The measured waveforms shown in Fig. 10 and the displayed image shown in Fig. 9(b) demonstrate that the proposed ER circuit can be used to drive the PDP without any compatibility problems with other circuits. The sustain voltage margin was \(-22\) V, regardless of the modes of operation of the proposed circuit. This value is more or less the same as the measured one using the conventional series and parallel resonance ER circuits.

The measured sustain waveforms and optical emissions for the series and parallel resonance modes of the proposed ER circuit are shown in Fig. 11. As shown in Fig. 11, the sustain discharges for both the series and parallel modes were induced \(~0.25\) \(\mu\)s before the sustain pulse peak, indicating that the circuit operated normally in both modes.

The DC current of the sustain power supply was measured while displaying black and full-white patterns. The measured currents for the black and full-white patterns in the series resonance mode were 0.75 and 1.31 A, respectively, and the values in the parallel resonance mode were 0.73 and 1.29 A. Considering that the experiment was performed at \(V_{\text{sus}} = 200\) V, the estimated power consumptions of the S/C drive board in the series and parallel resonance modes were 262 and 258 W for displaying the full-white pattern, respectively, and 150 and 146 W for displaying the black pattern. These are more or less the same as the power consumptions of other existing sustain circuits for 42-inch XGA AC PDP [10].

The EMI levels at the S and C output ports of the experimental sustain drive circuit were measured while displaying a full-white pattern and the results are shown in Fig. 12. For the experiment, the circuit was operating in the parallel resonance mode and the number of sustain pulse pairs for one field of picture was 260. The EMI was measured using the E4408B spectrum analyzer from Agilent Inc. with the RF4-E near field probe from Raaco Inc. The level of measured EMI at the C output port was lower than the one at the S output port because the scan pulses were applied to S. Over the whole frequency range of measurement, the soft switching for the first and last sustain pulses reduced EMI at both S and C output ports. The peak near 25 MHz, where the measurement mark was positioned, originated mainly from hard switching. With soft switching, the reduction of the hard switching EMI was \(-2.8\) and \(-6.2\) dBm at the S and C output ports, respectively. (The hard switching EMI levels at the S and C output ports were \(-45.07\) and \(-46.66\) dBm. They reduced to \(-47.86\) and \(-52.8\) dBm with soft switching.) The reduction of hard switching EMI at the S output port was much less than the one at the C output port because the scan pulses were applied to S. This result demonstrates that the proposed ER circuit was quite effective in reducing the EMI problem of the conventional parallel resonance ER circuit.

4. Conclusion

An energy recovery circuit which can operate either in a series or a parallel resonance mode and can drive an AC
PDP with single sustain circuit board, is proposed. It consists of one energy storage capacitor, two energy recovery inductors, and three insulated-gate bipolar transistors. The circuit operations in the series and parallel resonance modes are similar to the conventional ones, except for the leading edge of the first, and the trailing edge of the last sustain pulses in the parallel mode. These two pulse edges were generated using the series resonance mode in order to avoid EMI problems and reduce power dissipation. The measured energy recovery efficiencies of the proposed circuit in the series and parallel resonance modes were nearly the same as the one for the conventional series resonance ER circuit. To check compatibility of the proposed ER circuit with other PDP drive circuits, a full drive circuit for a 42-inch XGA single-scan PDP was designed and fabricated. The power consumptions of the S/C drive board in the series and parallel resonance modes were 262 and 258 W for displaying a full-white pattern, respectively, and 150 and 146 W for displaying a black pattern. The experimental results indicate that the proposed ER circuit is well suited for use in a PDP drive circuit.

Acknowledgements

This work was supported by LG Electronics Inc. and the Korean Ministry of Education under the BK21 program.

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