RTL Delay Macro-Modeling with $V_t$ and $V_{dd}$ Variability

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Abstract—Recent low-power design utilizes a variety of approaches for $V_{dd}$ and $V_t$ control to reduce dynamic and leakage power. It is important to be able to explore various low-power design options at a high-level early in the design process. Furthermore, process variation is becoming large and greatly affects the power and delay results. In particular, the delay analysis becomes very complicated and time-consuming with existing tools. This paper proposes a new efficient RTL delay macro-model to address these recent problems. The goal is to provide transistor-level accuracy at the RTL level with $V_t$ and $V_{dd}$ variability. It also includes the ability to handle PVT variations. The validation of the model is demonstrated by comparison with a circuit simulator and a timing verification tool. The experiments show this macro-model predicts the delay for variable $V_{dd}$ and $V_t$ with an accuracy of ±5% against HSPICE$^\text{TM}$ and ±10% against PrimeTime$^\text{TM}$ for a number of ITC’99 benchmark circuits.

Keywords—Delay Macromodel, RTL Delay Estimation.

I. INTRODUCTION

Designers are now faced with the problem of decreasing the power consumption of VLSI designs while keeping the performance high for portable devices like laptop computers, cell phones and so on. Controlling $V_{dd}$ and $V_t$ has a large effect on the power consumption and performance. To exacerbate the problem, the $V_t$ variation due to the process variation is becoming large and must be included in the analysis of power and delay. Thus, $V_{dd}$ and $V_t$ should be optimized dynamically, statically and statistically with efficient simulations. However, considering the variation of $V_{dd}$ and $V_t$, the delay analysis becomes very complicated and time-consuming by circuit-level or switch-level simulation. Furthermore, considering that the circuit size is becoming very large, delay models of higher abstraction level becomes very important.

In the past, power macro-models for fixed $V_t$ and $V_{dd}$ have been proposed [6]. However, no delay macro-model with $V_t$ and $V_{dd}$ variability for RTL has been proposed with PVT incorporated, although some delay models have been developed at transistor level [1-3].

This paper proposes a new delay macro-model. It enables accurate simulation based on transistor-level modeling and provides efficient analysis at the register transfer level. Furthermore, it provides $V_t$ and $V_{dd}$ variability. It improves the productivity of low-power system designs drastically, since the recent low-power design utilizes complicated approaches of $V_{dd}$ and $V_t$ control, for example MTCMOS, VTCMOS, and other dual-$V_t$ circuits [4, 5]. In addition, our delay macro-model is applicable to statistical timing model in RTL. It opens a new vista of statistical timing analysis.

In the following, we define the design style and assumptions in Section 2. In Section 3, the delay model for basic logic gates (NAND, NOR and INV) is described and it is used as a starting point for the macro-modeling of RTL blocks. The method for extracting the values of the parameters is also explained in this section. The validation of the model with evaluations using some sample circuits that consist of NAND’s, NOR’s and INV’s is described in Section 4. Then, a macro-model for RTL blocks is proposed in Section 5. In Section 6, the validation of our method is shown using some sequential circuit, ITC’99 benchmark circuits. In addition, comparison of experimental results with a switch level simulator and solution with our model is shown here. Conclusions are discussed in Section 7.

II. DESIGN STYLE DEFINITION AND ASSUMPTION

Since the goal of our work is to develop a delay macro-model that is applicable to low-power design with $V_t$ and $V_{dd}$ management, the assumptions related to the underlying design strategy are important. The assumptions we consider are listed below:

- The layout structure consists of multiple voltage islands. A supply voltage is distributed to each voltage island, which consists of some RTL circuits. The supply voltage is different in each voltage island.
- The target circuits have three operating modes, active, idle, and shut-off. MTCMOS and VTCMOS can be used to generate the different operating modes.
• The power consumption to minimize is the average power.
• The delay is the time when an input signal propagates from DFF to the next DFF along the critical path. It includes the setup time and \( T_{\text{clk-q}} \) delay of DFF. This delay is used to determine the maximum clock frequency at which timing is met.
• The delay of sequential circuits is the sum of the delay of the combinational circuits with DFF along the critical path.
• One threshold voltage is given for the critical path in a RTL circuit. Other logic gates may have other threshold voltages to reduce leakage power.
• Critical path is identified and the number of gates along the critical path is known. Logic gates such as NAND and NOR have series transistors. In order to minimize the critical path delay, it is designed that the pin, in the equivalent input pins, connected to the critical path is always connected to the nearest transistor to the drain terminal.

III. Simplified Delay Model

A. The delay model using two fitting parameters, \( \alpha \) and \( \mu \)

A simplified delay model for basic logic gates such as NAND, NOR, and INV can be expressed as follows:

\[
\Delta t = \frac{C_i \cdot V_{dd}^2}{K \cdot (V_{dd} - V_t)^\alpha} \quad (1)
\]

\[
K = \mu \cdot C_{ox} \cdot \frac{W}{L} \quad (2)
\]

where \( W \) and \( L \) are effective channel width and length, \( V_{dd} \) is the supply voltage, \( V_t \) is the threshold voltage, \( C_i \) is the effective oxide capacitance. Here, \( \alpha \) is proposed as a fitting parameter to fit the experimental results of delay. Normally, \( \alpha \) is used to reproduce the transistor \( I_d-V_{gs} \) characteristics as described in [1]. However, we use this parameter for fitting the delay characteristics and simplifying the delay model. The \( \alpha \) in [1] is around 1.2 but the \( \alpha \) in our work is closer to 2.0 because we try to fit delay variations in RTL blocks, not transistor I-V curves. More generally, the values of \( \alpha \) are obtained from experimental results of delay with HSPICE.

The other parameter, \( \mu \), is the effective mobility and is heavily dependent on \( V_{dd} \). So we assume that \( \mu \) is only function of the supply voltage. These values of \( \mu \) are stored using a lookup-table to capture the experimental results. Alternatively, an equation-based approach can be used represent the data, but we have chosen a lookup table in our work.

Using Equations (1) and (2), the total delay of the critical path in a target circuit is expressed as:

\[
\tau = T_{\text{clk-q}} + \sum \Delta t_{\text{NMOS}} + \sum \Delta t_{\text{PMOS}} + T_{\text{setup}} \quad (3)
\]

where \( \tau \) is the total delay, \( T_{\text{clk-q}} \) is delay from the time that the clock arrives to the point at which output voltage stabilizes, \( T_{\text{setup}} \) is the time that the incoming data must be stable before the clock arrives, \( \Delta t_{\text{NMOS}} \) is the time when the output transitions from \( V_{dd} \) to \( V_{dd}/2 \) and \( \Delta t_{\text{PMOS}} \) is the time when the output transitions from 0 to \( V_{dd}/2 \).

Delay modeling must be considered D-flip-flop for RTL estimation because DFF is put on either side of a combinational circuit. When LSIs frequency is determined, setup time and the DFF delay should be considered. The values of \( T_{\text{clk-q}} \) and \( T_{\text{setup}} \) can be derived with HSPICE simply. The values of \( T_{\text{clk-q}} \) and \( T_{\text{setup}} \) depend on \( V_{dd} \) and \( V_t \) and are stored in Look-up-table in order to take these values at the simulation. The total delay through a critical path is the sum of \( \Delta t_{\text{NMOS}} \) and \( \Delta t_{\text{PMOS}} \) of the signals on the critical path. How accurately the values of \( \alpha \) and \( \mu \) are extracted determines the overall accuracy of the delay model.

B. Determining values of \( \alpha \) and \( \mu \)

The values of \( \alpha \) and \( \mu \) are extracted from the experimental results with HSPICE and these values should be intended for the purposes of delay estimation in RTL blocks. The method used to derive the values of these fitting parameters is explained below. First, the delay of a 10 series NAND, 11 series NAND, and 12 series NAND are measured with HSPICE. Then, \( \Delta t_{\text{PMOS}} \) and \( \Delta t_{\text{NMOS}} \) are calculated based on delay differences between stages, using Equations (4) and (5):

\[
\Delta t_{\text{PMOS}} = \tau_{12} - \tau_{11} \quad (4)
\]

\[
\Delta t_{\text{NMOS}} = \tau_{11} - \tau_{10} \quad (5)
\]

The \( \Delta t \) vs \( V_t \) characteristics can be obtained using this method. Figure 1 shows plots of \( \Delta t \) vs \( V_t \) for NMOS and PMOS devices. Next, two points, \( (V_t, \Delta t_{1}) \) and \( (V_t, \Delta t_{2}) \), are chosen from the \( \Delta t \) vs \( V_t \) plots for a given \( V_{dd} \). The values of \( \alpha \) can be calculated through substituting the points into Equation (6) at each \( V_{dd} \) and an average of \( \alpha \) calculated separately for NMOS and PMOS devices using Equation (7). The \( \alpha \) value of NMOS and PMOS at each \( V_{dd} \) is shown in Figure 2. According to our experiments, we find the averages of \( \alpha \) are \( \alpha_{\text{NMOS}} = 2.12 \) and \( \alpha_{\text{PMOS}} = 1.93 \) for 0.18um CMOS. We assume that \( \alpha \) is constant value for the remaining analysis.

\[
\alpha = \frac{\log(\Delta t_{1}/\Delta t_{2})}{\log((V_{dd} - V_t)/2(V_{dd} - V_t))} \quad (6)
\]

\[
\alpha = \text{Avg.}(\alpha(V_{dd} = 1.8), \alpha(V_{dd} = 1.6), ..., \alpha(V_{dd} = 0.9)) \quad (7)
\]
Next, the method used to derive the $\mu$ is explained. The $\mu$ is greatly dependent on the supply voltage $V_{dd}$ and largely independent of the threshold voltage. The values of this parameter are derived with substitution of $\alpha$ and the $\Delta t$ into Equation (8) and (9) at each $V_{dd}$ and $V_t$. Finally, the average of the $\mu$ is calculated at each $V_{dd}$ using Equation (10). Results are shown in Table I. The effective mobility decreases as the supply voltage increases, and the mobility values of NMOS and PMOS should be calculated separately and stored in a table lookup form, as follows:

$$\mu_{PMOS} = \frac{1}{2} \frac{C_t}{Cox} \frac{L}{W} \frac{V_{dd}}{(V_{dd} - V_t)_{PMOS}} \Delta t_{PMOS}$$  \hspace{1cm} (8)

$$\mu_{NMOS} = \frac{1}{2} \frac{C_t}{Cox} \frac{L}{W} \frac{V_{dd}}{(V_{dd} - V_t)_{NMOS}} \Delta t_{NMOS}$$  \hspace{1cm} (9)

$$\mu = \text{Avg.}(\mu(V_t = 0.452), \mu(V_t = 0.466), \ldots, \mu(V_t = 0.772))$$  \hspace{1cm} (10)

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline
$V_{dd}$ & 1.8 & 1.6 & 1.4 & 1.2 & 1 & 0.9 \\
\hline
$\mu_{nmos}$ & 258 & 294 & 334 & 394 & 513 & 636 \\
$\mu_{pmos}$ & 42 & 48 & 55 & 66 & 88 & 109 \\
\hline
\end{tabular}
\caption{\textit{V} TABLE}
\end{table}

C. PVT Variation Simulation with our macro model

Variations in process, supply voltage and temperature (PVT) are problems that arise in deep submicron technology. Supply voltage variations are already included in the delay model. Process parameter variations pose a major challenge in the design optimization of high performance VLSI circuits, especially for sub-100nm technologies. Process variation causes about 20x variation in chip leakage and 30% variation in chip frequency [7]. Major sources of process variation consist of width and length, oxide thickness, threshold voltage and mobility variation on the chip. The device and interconnect performance have temperature dependence, with higher temperature causing performance degradation. Since the threshold voltage changes by 0.8 mV/C, the variation in temperature introduces approximately 60 mV of threshold voltage variation [8]. This can be incorporated in our model by making $V_t$ a linear function of temperature. Simple equations that include the variation of mobility with temperature can also be incorporated in this model, as follows:

$$\mu(T) = \mu_0 \left(\frac{T}{300^{\circ}K}\right)^{-1.5}$$  \hspace{1cm} (11)

where $\mu_0$ is the nominal temperature mobility. Finally, adjustment can be made to $Cox$, $W$ and $L$ to incorporate device variations. Therefore, PVT variation can be simulated with the parameter value variations of $V_t$, $V_{dd}$, $\mu$ and device dimensions. Our macro-model can be applied to statistical simulations for the variations. Some statistical simulations for variations are proposed and known widely. Delay variation due to supply voltage and threshold voltage variation can be simulated statistically because this model has the $V_t$ and $V_{dd}$ variability. In addition, this model is applicable to the channel length and width variation statistical simulation.
IV. Delay Estimation for Logic

The delay variation due to $V_{dd}$ and $V_t$ can be estimated without simulations using the model described in the previous section. While the use of this model does not have any inherent restrictions, it is important to specify the range over which it is applicable in practical circuits. This helps to provide delay estimates with accuracy of $\pm5\%$ at the logic level and $\pm10\%$ for RTL designs in a particular region defined by $V_{dd}$ and $V_t$. The region is expressed as follows:

$$\text{Delay}(V_t, V_{dd}) \leq 2 \cdot \text{Delay}_{\text{min}}$$  \hspace{1cm} (12)

where $\text{Delay}_{\text{min}}$ is the delay of a target circuit when $V_{sb}=0$ and $V_{dd}=1.8$. We assume that the allowable delay must be less than twice the minimum delay of a target circuit. For example, when the technology is 0.18um, it places $V_{dd}$ in the range of 1.8 to 0.9 and $V_t$ in the range of less than 0.95 at $V_{dd}=1.8$. While the range depends on the target technology, it does not present any practical design limitations.

A sample circuit that consisted of NANDs, NORs, and INVs was simulated using HSPICE and compared against the model. All of the logic gates on the critical path were identified in advance and used in the analysis. The circuit consists of 60 logic gates and the ratio is (INV:NAND:NOR = 3:6:1). The comparison is shown in Figure 4.

$$\text{Delay}_n = \text{Delay}_{\text{model}}(V_{dd}, V_t)$$

where $\text{Delay}_{\text{model}}$ is the value of the delay calculated with the model at the same point ($V_{dd}, V_t$). According to our experiments, the accuracy of this modified model is the range of accuracy of $\pm5\%$.

V. Delay Estimation for RTL Blocks

We now propose a method to estimate the delay of the RTL blocks as $V_{dd}$ and $V_t$ change without the need of detailed simulations. Such simulations with HSPICE take a long time to measure the delay at each $V_{dd}$ and $V_t$. However, our macro-model does not require much computational effort to predict the delay, after model generation and calibration. A NAND chain that has $n$ gates is used to approximate the critical path in an RTL block in our method, as shown in Figure 5. Once the critical path in the target RTL block is identified, it is replaced by the NAND chain for the delay estimation.

The model generation methodology of the target RTL block that we use in this paper is explained as follows. A VHDL description of the target circuit is obtained initially and a critical path delay in the block is identified. The kind of logic gates in the target block and the size of transistors are unknown. The value of the delay, $\text{Delay}_s$, of the target circuit is extracted at a point ($V_{dd}, V_t$) with simulations before the approximation. The number of gates, $n$, should be a known quantity. If unknown, the $n$ can be estimated from the initial calibration point ($V_{dd}, V_t, \text{Delay}_s$) of the RTL circuit with Equation (13) and (14) below. First, the $n$ is assumed to be even number and calculated by substituting the initial value to Equation (13). Next, the $n$ is assumed to be an odd number and calculated twice (extra $\Delta t_{\text{PMOS}}$ or $\Delta t_{\text{NMOS}}$) by substituting the initial value to Equation (14). Finally, the $n$ that produces a delay closest to the initial value is selected.

If the $n$ is even:

$$\text{Delay}_1 = \sum_{i=1}^{n/2} \Delta t_{\text{PMOS}} + \sum_{i=1}^{n/2} \Delta t_{\text{NMOS}}$$  \hspace{1cm} (13)$$

If the $n$ is odd, two possible cases exist:

$$\text{Delay}_1 = \sum_{i=1}^{n/2+1} \Delta t_{\text{PMOS}} + \sum_{i=1}^{n/2+1} \Delta t_{\text{NMOS}}$$  \hspace{1cm} (14)$$

After calibration, the delay for any value of $V_{dd}$ and $V_t$ is obtained from the delay equations.
VI. Results with Sequential Circuits

To evaluate the delay macromodel, the RTL estimation was carried out with ITC’99 benchmark circuits [9]. The results in the previous section were based on 180nm CMOS. In this section, we use a 90nm CMOS technology. The benchmark was synthesized to the gate level using Synopsys Design Compiler™ and analyzed using PrimeTime™. These tools provide the critical path delay information along with the number of logic stages along the critical path.

With technology scaling below 90nm, the use of multiple-\(V_t\) libraries is standard for reducing leakage power. Many libraries today offer three versions of their cells: Low \(V_t\) (LVT), Standard \(V_t\) (SVT) and High \(V_t\) (HVT) [10]. In our work, we use the values \(LVT \approx 0.2V\), \(SVT \approx 0.4V\) and \(HVT \approx 0.5V\). The principle objective of having multiple libraries is to reduce leakage power. HVT cells typically have higher delay but lower leakage power while the converse is true for LVT cells. For SVT cells, the delay and power numbers range in between the HVT and LVT cells.

The dual-\(V_t\) design technique selectively places low threshold transistors (LVT) on the critical paths of a circuit. The rest of the design can use SVT or HVT. In MTCMOS, the cores using either LVT or SVT are power-gated using HVT sleep transistors. Therefore, blocks are either active, idle or in sleep mode. For our analysis, we assume that the critical path of the block uses only one value of \(V_t\), either LVT, SVT or HVT.

Since CAD tools are aware of the standard multi-threshold processes, they provide built-in models for LVT, SVT, and HVT. For our work, the delay calibration was initially carried out with PrimeTime™ at the nominal process corner (TT), supply voltage (1.2V), threshold voltage (SVT), and temperature (\(25^\circ C\)). Then, the model was evaluated at 5 other points for each circuit: (1.2V, LVT), (1.2V, HVT), (1.0V, LVT), (1.0V, SVT) and (1.0V, HVT). These results were compared with the results obtained from PrimeTime™ at the same corners.

The values of \(\alpha\) and \(\mu\) model parameters extracted from HSPICE simulations are as follows:

\[
\begin{align*}
\alpha_{LVT} &= 1.26, \quad \alpha_{SVT} = 1.89 \\
\mu_{LVT}(V_s = 1.2V) &= 275cm^2/V-s \\
\mu_{LVT}(V_s = 1.0V) &= 279cm^2/V-s \\
\mu_{SVT}(V_s = 1.2V) &= 81cm^2/V-s \\
\mu_{SVT}(V_s = 1.0V) &= 86cm^2/V-s
\end{align*}
\]

The plots of the six points from PrimeTime™ and the Model are shown in Fig. 6. Three cases are shown with differing amounts of delay error: b22 (2%), b18 (5%), and b15 (10%). The results indicate that the model is quite accurate.
A larger set of 15 benchmarks were analyzed in the same manner. The characteristics of the circuits are shown in Table II. We provide the worst-case errors for each circuit. At 250°C, the largest error for these circuits is 9.6% and the smallest is 1.7%. The average error is about 6.3%. Note that delays for only \( V_{dd} = 1.2 \)V and \( V_{dd} = 1.0 \)V were used since they were only available from PrimeTimeTM at 25°C. A larger range of \( V_{dd} \) is expected to produce the same results since the HSPICE and Model accuracy was within 5%.

We also performed the analysis at temperatures of -40°C and 105°C. This was implemented by varying \( V_{dd} \) linearly with a temperature coefficient and \( \mu \) according to Equation (11). In the first case, we used \( V_{dd} = 1.1 \)V at \( T= -40 \)°C for calibration, followed by comparisons at \( V_{dd} = 1.1 \)V and \( V_{dd} = 1.26 \)V for LVT, SVT and HVT. In the second case, we used \( V_{dd} = 0.9 \)V at \( T= 105 \)°C for calibration, followed by comparisons at \( V_{dd} = 0.9 \)V and \( V_{dd} = 1.08 \)V. The results show an average error of 10.7% for -40°C and 9.7% for 105°C. These results are well within acceptable limits for RTL analysis.

We also showed on 90nm CMOS that the results for the delay estimation for RTL can be within ±6% of PrimeTimeTM after calibration, assuming a single value of \( V_{dd} \) and \( V_{dd} \) in the critical path. Therefore, this model is well-suited for RTL delay estimation at a high-level. It is also capable of handling temperature variations of \( \alpha \) and \( \mu \). The model has applications in voltage island design and other low-power design applications.

### REFERENCES


### TABLE II. ITC’99 SEQUENTIAL BENCHMARK CIRCUITS

<table>
<thead>
<tr>
<th>Design Name</th>
<th>Ni Gate</th>
<th>Ni O/P</th>
<th>Ni FF</th>
<th>CP logic</th>
<th>Max % Error 25°C</th>
<th>Max % Error -40°C</th>
<th>Max % Error 105°C</th>
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<td>b03</td>
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**Average Error for the 15 designs** | 6.3 | 10.7 | 9.7

### VII. Conclusion and Future Work

In this paper, we have proposed a macro-model for delay estimation of RTL blocks. The delay of RTL blocks can be predicted using the macro-model simply but accurately. The two parameters, \( \alpha \) and \( \mu \), used in the macro-model are extracted from experimental results with HSPICE™ in our method. The macro-model was validated based on the results in a 0.18um CMOS technology and showed accuracy within ±5% of HSPICE™ results after calibration. We also showed on 90nm