Overcoming the Challenges of Designing CMOS Software Defined Radio Receivers Front-Ends Embedding Analog Signal Conditioning

Silvian Spiridon\textsuperscript{1,2}, Claudius Dan\textsuperscript{1}, Mircea Bodea\textsuperscript{1}

\textsuperscript{1}“POLITEHNICA” University of Bucharest, \textsuperscript{2}Now with Broadcom, Bunnik, The Netherlands

Abstract—Today’s mobile terminals are real multiple media platforms compatible to a rather large number of wireless standards. The ideal candidate for such a mobile terminal radio receiver front-end is the Software Defined Radio Receiver (SDRR). The main challenge the designer must overcome is the SDRR circuit level design optimization, while considering the large amount of information comprised in the envisaged wireless standards. By driving the SDRR design through an initial system level analysis, based on a standard independent systematic methodology, the useful information is structured. Thus, a SDRR design recipe is developed based on the circuit / transistor level designer perspective.

I. INTRODUCTION

Today’s radio environment is governed by a large number of wireless communication standards (e.g., GSM, Bluetooth, W-LAN). The basic modern communication system is depicted in Fig. 1: different types of mobile equipment connected into wireless networks.

It becomes obvious there is a strong need of mobile equipment capable of communicating over the envisaged standards.

The first obvious solution is to incorporate for each standard a separate Application Specific Integrated Circuit (ASIC) into the mobile device. Nonetheless this requires a large number of ICs. But, building a reconfigurable ASIC, able to ensure compatibility with the wide array of communication standards in use today, is more efficient from two main reasons, \cite{1}:

1. One “universal” design is required; thus design, packaging and testing costs are minimized, and
2. As the “universal” ASIC is compatible with a wide array of wireless communication standards the various ASICs can be merged; thus the overall area of ASICs comprised in a mobile terminal is minimized.

Moreover, in order to maximize the potential of wireless communications, the latest wireless standards converge towards an “one size fits all” solution. As an example, the W-LAN standard, IEEE 802.11g uses almost all digital modulation schemes (BPSK, QPSK, QAM-16 and QAM-64) on OFDMA carrier support with variable modulation depths, while it still maintains compatibility with the earlier IEEE 802.11b lower data rate standard, \cite{2}. Another example is the WiMAX – IEEE 802.16 standard, \cite{3}.

Hence, also the latest developments in standardization point to a software re-configurable hardware solution for the radio front-end as the best way to trade-off backwards compatibility with future trends.

The paper’s main goal is to tackle the challenges of designing CMOS SDRR front-ends embedding analog signal conditioning and to develop a design receipt from the circuit / transistor level designer perspective.

In order to achieve this aim, a structured approach with clear design targets is required. Section II introduces the structured SDRR front-end design approach emphasizing the key design targets, while Section III presents the SDRR front-end design recipe. Finally, Section IV presents the conclusions.
II. A STRUCTURED APPROACH IN SDRR DESIGN

Designing radio receivers in general, and SDRRs in particular, is a very challenging task. The amount of information the designer needs to disseminate, both at circuit level as well as at system level, is huge. Therefore a structured approach of the design process is the enabling factor in finding and implementing the optimal circuit design.

From the beginning the designer must set clear design targets which should enable him to identifying the key trade-offs shaping the SDRR design. First of all, (1) the most suited architecture for the SDRR front-end, in the deep sub-micron CMOS processes needs to be identified. Second of all, (2) the designer needs to be able to handle efficiently the large amount of information comprised in the wireless standards. Basically he requires a compass that enables him to explore the SDRR domain map. This tool must be based on simple and efficient models suited for manual analysis. Third of all, (3) to develop the SDRR front-end design strategy from both the system level and transistor level perspectives and to use this strategy to design the front-end’s building blocks.

III. A SDRR FRONT-END DESIGN RECEIPT

A. The Optimal Architecture

First, the analysis should tackle the identification of the most suited architecture for the SDRR front-end. The most efficient choice for the SDRR front-end, from the system level implementation, was coined by Mitola in reference [4]. Basically the front-end is an Analog-to-Digital Converter (ADC). But, still to this date, due to practical implementation constrains in a CMOS process, a SDRR embeds a signal conditioning block in between the antenna and the ADC. This block will provide additional selectivity, amplification and frequency translation to the wanted signal, thus relaxing the ADC performance requirements. By extending the homodyne architecture through the inclusion of (a) an offset cancelation loop and (b) an LO frequency divider, its monolithic integration is facilitated.

Moreover, the homodyne architecture was enhanced to the concept in Fig. 2, [1], in order to fit better a multi-standard receiver implementation.

The RF signal is firstly amplified by a Low Noise Amplifier (LNA) and then downconverted directly to baseband in the mixer (MIX). The anti-alias Low Pass Filter (LPF) knocks down the unwanted blockers and interferers to allow the Variable Gain Amplifier (VGA) to amplify the wanted signal and optimally load the ADC. The system is operated by the baseband signal processor.

In [5], based on the analysis and evaluation of figures of merit of existing radio receiver architectures the homodyne topology, also known as direct conversion or zero-IF architecture, is proposed as the best candidate for an “universal” receiver. In [6], the key issues of direct conversion receivers, like offset, 1/f noise and self-mixing, are presented and solutions are proposed to make the homodyne architecture ready for monolithic integration. By extending the homodyne architecture through the inclusion of (a) an offset cancelation loop and (b) an LO frequency divider, its monolithic integration is facilitated.
TABLE I
THE KEY SDRR PARAMETERS THAT ENABLE A STANDARD INDEPENDENT APPROACH

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Notes</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity @ 3dB noise figure</td>
<td>Receiver sensitivity, $S_{RX}$</td>
<td>$-109$</td>
</tr>
<tr>
<td>Frequency plan</td>
<td></td>
<td>$-95...-78$</td>
</tr>
<tr>
<td>RF channel bandwidth</td>
<td>$0.8 / 0.9 / 1.8 / 1.9$ GHz</td>
<td>$2.4 / 5$ GHz</td>
</tr>
<tr>
<td>Effective RF signal bandwidth $BW_{RF}$</td>
<td></td>
<td>$0.2$ MHz</td>
</tr>
<tr>
<td>$SNR_{0}$</td>
<td>The minimum SNR at the receiver output required for the</td>
<td>$9$</td>
</tr>
<tr>
<td></td>
<td>signal demodulation within the specified Bit Error Rate</td>
<td>$4...21$</td>
</tr>
</tbody>
</table>

The design of any wireless receiver is determined by the interdependency between its noise, linearity and gain performance. With a smart design the input impedance influence can be equated out.

Fig. 3 sketches the liaisons between the individual trades-offs shaping the SDRR front-end design. The most important consequences of solving the trade-offs are: (1) the optimal filter partitioning, as the solution for the trade-off between the SDRR area and power consumption, [11], and (2) the smart gain partitioning, as a solution for the trade-off between the SDRR noise and linearity performance, [12].

First, the most important issue due to blockers and interferers is the risk of the receiver output clipping. This is due to (a) the large receiver dynamic range, and thus, gain imposed by the low sensitivity levels and (b) the large difference in power levels between the blockers and the RF useful signal. Hence, the receiver selectivity is critical and a thorough analysis of the channel selection strategies is required.

In [11], the SDRR generic blockers diagram is defined and introduced, as a very efficient tool in evaluating, in a standard independent approach, the filter partitioning for channel selection in multi-standard radio receivers. The diagram consists of all blockers and interferers present at receiver’s antenna input, under which influence the receiver must be able, still, to successfully demodulate the wanted signal. By using this tool, the designer is enabled to find the optimal channel selection strategy (e.g., a LPF order larger than 4 brings no further benefit for the targeted standards channel selection, [11]). Further on, thanks to an in-depth analysis of the envisaged standard requirements, the receiver linearity performance (i.e., its $IIP3, IIP_{3RX}$) is evaluated, [10].

Second, (2) the wireless environment offers extreme conditions for the radio signal reception. Depending on the received signal characteristics (i.e., the wanted signal level and the presence of blockers and interferers), the SDRR ability to properly demodulate the signal is tributary to either its noise or linearity performance.

For standard independent approach, the signal reception is grouped in three generic scenarios: (i) the wanted signal is very week and the receiver noise performance is critical, (ii) the input signal is weak, but is surrounded by blockers and interferers, as specified by the blockers diagram; in this case, while a good noise performance is required, the linearity constraint become also important and (iii) the wanted signal is strong, and, thus, the receiver noise performance is critical.

In order to mitigate all the receive scenarios, the authors introduce in [12] the smart gain partitioning strategy tailored towards multi-standard radio receivers.

Basically, the smart gain partitioning foresees (a) the receiver gain is programmable depending on the input signal level and is split in between its HF and LF part (i.e., between the LNA and the VGA) and (b) the receiver noise and linearity performance (i.e., $NF_{RX}$ and $IIP3_{RX}$) adjust with its HF part gain, $A_{HF}$. Hence, by evaluating the received burst characteristics through the Receiver Signal Strength Indicator (RSSI), the receiver gain and its noise and linearity performance are dynamically adjusted. In this way, the SNR at the receiver output, $SNR_{out}$, is kept larger than $SNR_{0}$, the minimum required for a proper signal demodulation.

Basically, all the key SDRR electrical specifications are determined based on hand calculation. Of course, CAD simulations can further assist the designer in validating and refining the numbers.

C. The Design Strategy

The receiver RF front-end (i.e., the LNA and mixer) should be built using differential or pseudo-differential transistor pairs, [7]. The trade-off between the noise and linearity performance is set by the amount of source degeneration: when low noise is required, the RF front-end gain is set to the maximum and subsequently no degeneration is to be implemented, at least in the LNA; on the other hand, when high linearity is required, it can be achieved by degenerating the source of the differential pair devices.

The main goals in choosing the baseband blocks architecture are: (a) high linearity and (b) immunity to particular technology characteristics and easiness of the design porting.
To control the baseband chain linearity, given the rather low baseband signal bandwidth (i.e., maximum 20 MHz for W-LAN), low power feedback amplifiers are used as the building brick of all the low frequency part circuits. The amplifier implementation is based on a high GBW fully differential op amp and on a linear feedback network of poly Si resistors and/or metal-insulator-metal capacitors, [13]. The two stage opamp concept is implementing a class AB output stage (a) to leverage the noise-linearity constraints with the low power consumption requirement of mobile applications and (b) to decouple the intrinsic opamp parameters (e. g., GBW) from the output load, [14].

By using feedback the modular architecture gains immunity to particular technology characteristics, like leakage, and inherently also to process scaling, as feed-back use represents the only way the designer can control and, subsequently, meet the specifications, alleviating the technology implementation.

IV. CONCLUSIONS AND FUTURE TRENDS

This paper tackled the challenges in designing CMOS multi-standard radio receivers embedding analog signal conditioning. A SDRR front-end design receipt was developed from the circuit / transistor level designer perspective. The structured approach aids the designer (i) in handling the huge amount of information in the wireless standards and, subsequently, (ii) in finding the optimum choices for the SDRR front-end circuit level implementation.

By firstly identifying the most suited architecture, given the deep sub-micron CMOS processes, the designer can pursue the calculation of the SDRR electrical specifications through a comprehensive standard independent analysis based on hand calculations. Finally, the SDRR front-end circuit level implementation is based on a modular design targeting future design scaling.

Still, looking in the future, the trend is to move as much as possible the processing of the RF/analog signal into the digital domain. Literature papers, [14, 15] have shown the feasibility of analog circuits content reduction in radio transmitters and synthesizers, in favor of more digital circuits.

Also, techniques in calibrating transceiver impairments by using the relative inexpensive digital gates are starting to appear. Already for calibrating transmitter impairments, such breakthrough techniques have been recently published in [17].

For radio receivers such leap forward methods have just been reported for the low frequency part. In [18] a novel architecture for the BB chain of a multi-standard wireless receiver has been presented: almost the whole receiver can be described in an RTL language and can be implemented using a standard digital design approach, except a small macroblock located after the downconverter mixer. By extrapolating this trend and by considering the high rate at which the ADCs power efficiency is improved, [19], on short or medium term ADC based SDRRs will become reality.

ACKNOWLEDGMENT

The authors would like to express their acknowledgment to Dr. F. Op’t Eynde for the fruitful discussions on the topic.

REFERENCES