Abstract—In this paper, a novel Chinese abacus multiplier is presented. The architecture of a 4-bit multiplier is demonstrated. The simulation results of our work are compared with the 4-bit Braun array multiplier. The 0.35\(\mu\)m and 0.18\(\mu\)m TSMC CMOS technologies are used in the simulation. The delay time of the abacus multiplier is at least 63\% less than that of Braun array multiplier for 0.18\(\mu\)m technology. The power consumption of the abacus multiplier is about 51\% less than that of Braun array multiplier for 0.18\(\mu\)m technology.

Index Terms—Braun array multiplier, Chinese abacus multiplier, fast multiplier, high speed.

I. INTRODUCTION

Multiplication is one of the most critical operations in many computational systems. Array-based multipliers [1], [2] and tree-based multipliers [3], [4] are well known and are often used in VLSI implementation of fast multipliers. This paper presents a novel multiplier by using Chinese abacus method to achieve high speed and low power.

The Chinese abacus is a very popular efficient technique used for centuries in China and other Orient countries to perform arithmetic functions. Gang et al. [5]–[7] proposed the first novel adder employing the method of Chinese abacus, and we then proposed another novel radix-4 Chinese abacus adder [8].

A basic column element of the Chinese abacus is depicted in Figure 1. Figure 1 demonstrated the decimal number of seven represented by Chinese abacus. Each column element has one higher bead with a weight of five and four lower beads with a weight of one. The key feature of the Chinese abacus is the use of one bead with weight five. This allows the operator to minimize the transmission of rests.

Figure 1. Chinese abacus coding with base 10 of the decimal number 7.

A novel Chinese abacus multiplier was proposed in this paper. Figure 2 depicts the constitution of Chinese abacus multiplier. Each row element has three segments, up beads with each weight of sixteen, middle beads with each weight of four and bottom beads with each weight of one. Figure 2 depicts the decimal number 39 represented in the proposed Chinese abacus.

Figure 2. The configuration of proposed novel Chinese abacus multiplier.

An operation example of multiplication is demonstrated in Figure 3. \(A = (a_3 a_2 a_1 a_0)_2 = (1010)_2\), \(B = (b_3 b_2 b_1 b_0)_2 = (0111)_2\), the product of \(A\) and \(B\) can be expressed as \(1\times4^3 + 0\times4^2 + 1\times4^1 + 2\times4^0 = 70\).

Figure 3. An operation example of multiplication

The architecture of proposed multiplier is shown in Figure 4. The function of this 4x4 abacus multiplier is divided into three parts as depicted in Figure 4.

The first part is BPA (binary product to abacus) module. The second part is PA (parallel addition) module. The third part is TB (Thermometric to Binary) transformation module. The three modules are discussed in the following sections.

II. THE ARCHITECTURE OF THE PROPOSED MULTIPLIER

A. The first part is BPA (binary product to abacus) module:

This module converts two 4x2 binary number \((a_3 a_2 a_1 a_0)(b_1 b_0)\) and \((a_3 a_2 a_1 a_0)(b_3 b_2)\) into an abacus representation \((H_2 H_1 H_0)(M_2 M_1 M_0)(L_2 L_1 L_0)\)abacus. \((H_3 H_2 H_1)\) represents three up beads with each weight of sixteen \((4^2)\). \((M_2 M_1 M_0)\) represents three meddle beads with each weight of four \((4^1)\), and \((L_2 L_1 L_0)\) represents three lower beads with each weight of one \((4^0)\). The block diagram of the BPA is shown in Figure 5.
Figure 4. Block diagram of the 4x4 abacus multiplier

An example is demonstrated in Figure 3. (a3a2a1a0)2 = (1010)2 = 10 and (b1b0)2 = (11)2 = 3, (1010)2 * (11)2 = (001|111|011)abacus = (0+0+1)*16 + (1+1+1)*4 + (0+1+1)*1 = 30.

PG module transfers previous stage to up beads. The behavior of PG module is modeled in the equations (12) – (14):

\begin{align*}
O_0 &= 0 \\
O_1 &= X_1 + X_0C_{in} \\
O_2 &= X_0 + C_{in}
\end{align*}

B. The second part is PA (parallel addition) module:

This block can count two column elements with same weight and then transform it to thermometric representation K0-K5, where 0 ≤ K_i ≤ K_j ≤ 1 for i > j.

This module acts similarly as multiplexer. The number \(X_2X_1X_0\) is as the input signal of this multiplexer as shown in Figure 4. The number \(Y_2Y_1Y_0\) is as selector to modify the configuration of the number \(X_2X_1X_0\) and results the thermometric sum \(K_5K_4K_3K_2K_1K_0\). There are only four

\begin{align*}
H_1 &= (l_1*10) + (S_1*S_0) \\
H_0 &= (l_1)(S_1*S_0) + (l_1)(S_1*S_0) \\
L_2 &= (l_1*10)(S_1*S_0) + (l_1*10)(S_1*S_0) \\
L_1 &= (l_1)(S_1*S_0) + (l_1)(S_1*S_0) + (l_1*10)(S_1*S_0) \\
L_0 &= (l_1*10)(S_1*S_0) + (l_1)(S_1*S_0) + (l_1*10)(S_1*S_0)
\end{align*}
The behavior of PA module is modeled in the equations (15) – (22):

\[ f_1 = \overline{X_2} \cdot X_1 \]  
\[ f_2 = \overline{X_1} \cdot X_0 \]  
\[ K_0 = (Y_0) \overline{X_0} + (1)f_2 + (1)f_1 + (1)X_2 \]  
\[ K_1 = (Y_1) X_0 + (Y_0) f_2 + (1)f_1 + (1)X_2 \]  
\[ K_2 = (Y_2) \overline{X_0} + (Y_1) f_2 + (Y_0) f_1 + (1)X_2 \]  
\[ K_3 = (0) \overline{X_0} + (Y_2) f_2 + (Y_1) f_1 + (Y_0) X_2 \]  
\[ K_4 = (0) \overline{X_0} + (0) f_2 + (0) f_1 + (Y_2) X_2 \]  
\[ K_5 = (0) \overline{X_0} + (0) f_2 + (0) f_1 + (Y_2) X_2 \]  

The detail circuits of PA module are derived from the equations (15) – (22). The PA module can count all beads simultaneously.

C. The third part is TB (Thermometric to Binary) transformation module:

This module transforms thermometric representation to binary numbers. Although it may convert higher part or lower part number \( K_5 - K_0 \) as shown in Figure 4, the circuit of this module is identical. The outputs \( S_1, S_0 \) and \( C_{out} \) are determined by the following equations:

\[ S_0 = \overline{K_5} \cdot C_n + \overline{K_4} \cdot C_n + \overline{K_3} \cdot C_n + \overline{K_2} \cdot K_2 + \overline{K_1} \cdot C_n + \overline{K_0} \cdot C_n + \overline{K_1} \cdot \overline{K_0} \cdot C_n \]  
\[ S_1 = K_3 \cdot C_n + \overline{K_3} \cdot C_n + \overline{K_4} \cdot \overline{K_2} \cdot K_2 + \overline{K_1} \cdot C_n + \overline{K_0} \cdot C_n \]  
\[ C_{out} = K_3 + K_2 \cdot C_n \]  

The use of the Chinese abacus approach results a competitive technique with respect to conventional methodologies.

III. SIMULATIONS AND COMPARISONS

In the previous sections we designed a 4x4 multiplier by using the Chinese abacus methodology. The circuits of prototype have been simulated with HSPICE by using the transistor models of a 0.35\( \mu \)m, and 0.18\( \mu \)m TSMC CMOS technologies. For the sake of simplicity, all the lengths and widths of the transistors are set to the smallest values allowed by each technology, CMOS inverters are used as loads in each output in simulations. An inverter is used as input buffer to generate a real world signal waveform. The simulation results are compared with the 4x4 Braun array multiplier listed in Table I. The delay is the longest time of signal from input to output simulated by all input patterns. The simulation results used 0.35\( \mu \)m and 0.18\( \mu \)m TSMC CMOS technologies delay time is 2.99ns and 1.50ns. The delay of the 4x4 abacus multiplier is 63% less than Braun array multiplier for 0.18\( \mu \)m technology.

The power consumption of these multipliers is also listed in Table I. The average results of power consumption are various 256 input patterns. The simulation is performed at a frequency of 50MHz. In 0.18\( \mu \)m technology, the power consumption of abacus is 51% less than that of Braun array multiplier.

From these results, we can expect that abacus multiplier will remain competitive with the Braun array multiplier.

<table>
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<tr>
<th>Technology</th>
<th>This work</th>
<th>Reduction %</th>
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IV. CONCLUSION

This paper proposes a novel Chinese abacus multiplier. All the results are simulated by 0.18\( \mu \)m, 0.35\( \mu \)m TSMC CMOS technologies. The improvements are described as follows.

The delay time of abacus multiplier is at least 63% less than that of the Braun array multiplier in 0.18\( \mu \)m technologies.

Power consumption of the abacus multiplier is about 51% less than that of the Braun array multiplier in 0.18\( \mu \)m CMOS technology. It significantly reduced power consumption. The use of Chinese abacus approach results a competitive technique with respect to conventional fast multiplier.
Figure 7. The chip layout of 4x4 abacus multiplier in 0.35μm TSMC CMOS technology.

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