Tensile CESL-induced strain dependence on impact ionization efficiency in nMOSFETs

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1. Introduction

The study of strained Si has attracted considerable attention for improving metal–oxide–semiconductor field-effect transistors (MOSFETs) performance owing to the higher carrier mobility [1–6]. The improvement in carrier mobility originates from the modification of band structures leading to the reduction of the conductivity effective mass and the suppression of the carrier-phonon scattering rates [2,3]. In terms of CMOS process integration issue and cost consideration, process-induced strain, also called uniaxial strain, has become an indispensable method to boost advanced CMOS performance [4,5]. Among all the feasible process-induced strain methods (strained spacer, shallow trench isolation, embedded SiGe, etc.), capping a silicon nitride (SiN) film as a contact etch stop layer (CESL) is one of the promising ways to introduce the uni-axial strain into a transistor channel and is also compatible with a standard CMOS process flow [6]. However, a significant reliability topic in strained-Si MOSFETs is that the substrate current (I s) generation via impact ionization process, i.e., impact ionization efficiency (IIE), is widely believed to be enhanced by the uniaxial strain due to the carrier mobility improvement and/or the narrowing effect of the bandgap energy. Although the strain-induced IIE enhancement has already been reported [7–11], knowledge of the physical origin of the IIE enhancement is still poor.

The aim of this paper is to concentrate on the experimental analysis of the IIE enhancement in strained-Si MOSFETs with tensile CESL. From the universal relationship between the IIE and the electric field in the pinch-off region, the physical understanding of the tensile CESL-enhanced IIE in strained-Si MOSFETs can be substantially improved.

2. Experimental

The strained-Si nMOSFETs used in this study had a 30 nm-thick SiO2 and a 350 nm-thick polycrystalline silicon as the gate oxide. The gate oxide was used as a CESL stressor to apply tensile stress into the channel region. For comparison, the control-Si nMOSFETs deliberately removed the deposition step of the SiN cap layer and used a 100 nm-thick TEOS SiO2 instead, as shown in Fig. 1a. Furthermore, the MOSFETs used a gate width-to-length ratio of 25 μm/0.4 μm. The experimental samples were fabricated using an HP 4156C semiconductor parameter analyzer.

3. Results and discussion

Fig. 2 shows the linear region transfer characteristics of nMOSFETs without and with the tensile CESL. The field-effect mobility \( \mu_{FE} \) can be easily determined from the transconductance and given by \( \frac{g_m V_d}{C_{ox} V_{dW}} \), where \( g_m \) is the transconductance at \( V_d = 0.1 \) V. Compared to control Si, the enhanced \( \mu_{FE} \) ratio of approximately...
20% for strained-Si nMOSFETs is indicated in the insert of Fig. 2. In addition, Fig. 3 shows the drain saturation current \((I_{DS})\) enhancement for strained-Si nMOSFETs with the tensile CESL compared to the control-Si counterpart. As expected for strained-Si nMOSFETs, the \(I_{DS}\) enhancement can be attributed to the tensile channel strain caused by the presence of the CESL stressor. At the same gate overdrive \((V_G - V_T = 1.5\, \text{V})\), the comparison of \(I_{DS}\) for nMOSFETs between without and with the tensile CESL is plotted together in Fig. 3, clearly indicating a marked increase in \(I_{DS}\) at \(V_D > 3.5\, \text{V}\) for strained-Si nMOSFETs. Through the source terminal floating technique [10], the excess diode (drain-to-substrate) leakage current even at \(V_D > 3.5\, \text{V}\) has markedly smaller effect on the \(I_{DS}\) caused by impact ionization process, as shown in Fig. 4. Furthermore, for such

![Fig. 1. Schematic illustration of nMOSFETs: (a) without a tensile CESL and (b) with a tensile CESL.](image1)

![Fig. 2. Linear region transfer characteristics of nMOSFETs without and with the tensile CESL. The insert shows the enhanced mobility ratio of approximately 20% in strained-Si nMOSFETs compared to control-Si nMOSFETs.](image2)

![Fig. 3. Drain and substrate currents as a function of drain voltage for nMOSFETs with the tensile CESL at a fixed gate overdrive \((V_G - V_T = 1.5\, \text{V})\). The results of nMOSFETs without the tensile CESL are also shown for comparison.](image3)

![Fig. 4. Comparison of substrate current in control-Si nMOSFETs with source terminal grounded and floating at \(V_G - V_T = 1.5\, \text{V}\).](image4)

a 30 nm-thick gate oxide, the influence of the gate current on the \(I_{DS}\) can be also neglected. Therefore, the impact ionization multiplication coefficient \(M - 1\) as a function of \(V_G\) is determined to the ratio of the \(I_{DS}\) enhancement \(I_{DS}/I_{DS0}\) in control-Si near the drain region, it is necessary to translate \(M - 1(V_G) \approx I_{DS}/I_{DS0}\). Because of the \(I_{DS}\) enhancement associated with the maximum electric field \(E_m\) near the channel, it is necessary to translate \(M - 1(V_G) \approx M - 1(E_m)\). According to the lucky electron model [13], \(M - 1(E_m)\) is described as

\[
M - 1 \approx \frac{I_{DS}}{I_{DS0}} \exp \left( \frac{-\phi_i}{q\lambda E_m} \right),
\]

where \(\phi_i\) is the threshold energy for impact ionization and \(\lambda\) is the mean free path. Moreover, \(E_m\) can be expressed as

\[
E_m = \frac{V_D - V_{sat}}{I},
\]

where \(V_{sat}\) is the voltage at the pinch-off point and \(I\) is the effective pinch-off length. \(E_m\) in Eq. (2) can be indirectly assessed through \(V_{sat}\) versus \(V_{sat}\). \(V_{sat}\) is obtained from the linear extrapolation of the output resistance versus \(V_D\) plot in the channel-length modulation region (not shown here) [14]. As predicted by Eqs. (1) and (2), the slope of the \(\ln[I_{DS}/I_{DS0}(V_D - V_{sat})]\) versus \(1/(V_D - V_{sat})\) plot is represented by \(-\phi_i/q\lambda\). To differentiate between the contribution of these components \((I, \lambda, \text{and } \phi_i)\) to the IIE, the comparison of the slope change in nMOSFETs between without and with the tensile CESL is made, as shown in Fig. 5. Firstly, the \(I\) component is known to be proportional
to the source/drain junction depth ($x_j$) and the gate oxide thickness ($t_{ox}$), i.e., $l = x_j^3 t_{ox}^{1/3}$ [15], and mainly dependent on CMOS process. Here, the $l$ contributing to the IIE can be reasonably assumed to be negligible because the nMOSFETs were fabricated using the same front-end CMOS process. Secondly, in Fig. 5, the slope change of approximately 2.7% shows a tensile CESL-enhanced IIE, implying that the contribution of the $\lambda$ component to the IIE can be neglected. This is because under a high electric field, $\lambda$ appears to be insensitive to the CESL-induced tensile strain. Then, a constant high gate voltage of 20 V with 2 h at the room temperature, i.e., Fowler–Nordheim (FN) stress condition, is adopted to electrically stress the gate oxide, with source, drain, and substrate tied to ground. After undergoing the FN stressing, the subthreshold swing of strained-Si nMOSFETs shows a marked increase in the SiO$_2$/Si interface trap density, as seen in Fig. 6, and also supplies another condition with greater scattering, i.e., the change of the $\lambda$. In Fig. 7, the comparison of the slope change in strained-Si nMOSFET between without and with FN stressing appears to be quite consistent, further indicating that the contribution of the $\lambda$ component to the IIE could be ruled out. Furthermore, if the tensile CESL-enhanced IIE is attributed to the narrowing effect of the bandgap energy, the 2.7% slope change can correspond to the bandgap shift $\Delta E_g$ of approximately 30 meV. Through a well-known relationship of $\Delta E_g = -3.66 \times 10^{-11} \sigma$ [16], the channel stress, $\sigma$, caused by the tensile CESL can

![Fig. 5](image1.png)

**Fig. 5.** $I_d/I_D (V_d - V_{dsat})$ dependence of $1/(V_d - V_{dsat})$ in strained-Si nMOSFETs with the tensile CESL. The result of nMOSFETs without the tensile CESL is also shown for comparison.

![Fig. 7](image2.png)

**Fig. 7.** $I_d/I_D (V_d - V_{dsat})$ dependence of $1/(V_d - V_{dsat})$ in strained-Si nMOSFETs before and after FN stressing. The FN stress condition is at $V_G = 20$ V for 2 h.

![Fig. 8](image3.png)

**Fig. 8.** (a) Four-point-bending fixture and (b) schematic illustration of tensile stress for wafer bending.

![Fig. 9](image4.png)

**Fig. 9.** $I_d/I_D (V_d - V_{dsat})$ dependence of $1/(V_d - V_{dsat})$ in strained-Si nMOSFETs with the tensile CESL and an externally tensile stress. The results of nMOSFETs without the tensile CESL and externally tensile stresses are also shown for comparison.
be found to be approximately 820 MPa. In addition, the CESL-induced threshold-voltage shift ($\Delta V_T$) was characterized at $V_D = 0.1$ V and determined to be approximately 10 mV. The $\Delta V_T$ ($\approx 10$ mV) further linked to the $\Delta E_g$ can be expressed as $\Delta V_T \approx (m - 1)\Delta E_g$, where $m$ is the body-effect coefficient. The extracted $m$ value of 1.33 appears to exactly fall within a typical range of 1.3–1.4 [16]. Finally, a four-point-bending method is also used to apply the externally tensile stresses on strained-Si and control-Si nMOSFETs, as shown in Fig. 8. Compared to control Si, the marked slope change in strained-Si nMOSFETs with the tensile CESL and externally tensile stresses is shown in Fig. 9. Then, Fig. 10 shows that the wafer-bending experiments appear to be quite consistent with the theoretical calculation using $\Delta E_g = -3.66 \times 10^{-11} \sigma$ [16]. It clearly indicates that the tensile CESL-enhanced IIE can be mainly attributed to the narrowing effect of the bandgap energy. However, the comparison of the hot-electron degradation characteristics in nMOSFETs without and with the tensile CESL is also made, as shown in Fig. 11. Although the reliability degradation in strained-Si nMOSFETs appears to be more severe than that in control-Si nMOSFETs, the part certainly needs further research due to the opposite report showing the improved hot-electron reliability in strained-Si nMOSFETs [17].

4. Conclusion

Tensile CESL-induced strain dependence of the IIE in strained-Si nMOSFETs has been presented for the first time. From the universal relationship between the IIE and the electric field in the pinch-off region, a 2.7% difference in the IIE of nMOSFETs between without and with the tensile CESL is found. This result can not due to the modulation of the mean free path, $\lambda$, but to the narrowing effect of the bandgap energy caused by the tensile CESL-induced strain, i.e., the reduced threshold energy for impact ionization. In addition, the wafer-bending experiments can further give strong evidence on this point. It means that the IIE measurement can serve as a reliable monitor of CMOS process-induced strain into the channel.

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References