A Digital-Calibration Technique for Redundant Radix-4 Pipelined Analog-to-Digital Converters

Masanori Furuta, Member, Shoji Kawahito, Senior Member, IEEE, and Daisuke Miyazaki, Member, IEEE

Abstract—This paper describes a digital-calibration technique, which corrects gain errors due to capacitor mismatch and offset errors due to charge injection in redundant radix-4 pipelined analog-to-digital converters (ADCs). The error coefficients are directly measured using an integral nonlinearity (INL) plot. The proposed method simplifies the error-measurement process and removes on-chip measurement circuits in the ADC. Computer simulations show that the maximum INL of 15 LSB in an uncalibrated 15-bit ADC is reduced to less than 0.3 LSB using the digital calibration.

Index Terms—Capacitor mismatch, digital calibration, error measurement, pipelined analog-to-digital converter (ADC).

I. INTRODUCTION

HIGH-RESOLUTION analog-to-digital converters (ADCs) with high conversion rate are essential components in wideband wireless communication and modern video applications [1]–[3]. In these ADCs, nonlinearity, power dissipation, and chip area are important design issues. Pipelined architectures are becoming dominant for high-speed, high-resolution, and low-power ADCs. Pipelined ADCs with switched-capacitor implementations, which consist of a cascade of several low-resolution sub-ADCs, are particularly popular. Although several design styles exist for the pipelined ADC, the use of relatively high resolution per stage algorithm for sub-ADCs has made it possible in reducing the total power dissipation and chip area [4].

A main source of nonlinearity error in pipelined ADCs is capacitor mismatch in a multiplying digital-to-analog converter, particularly if relatively small capacitors are used in meeting the requirement of high-speed operation and low-power consumption. A number of techniques to overcome this limitation have been reported. An analog self-calibration [5], [6] is a technique that directly controls the sampling capacitance of each interstage gain amplifier by attaching trimming capacitors. However, this technique requires extra analog hardware, and it may degrade the analog performances. On the other hand, a digital-calibration technique [7], [8] does not much affect the performance of the ADC significantly, because the error correction of capacitor mismatch is performed in digital domain. Although this method needs extra digital hardware to process the error correction, an advanced CMOS technology relaxes the problem of the power dissipation and the circuit area of such digital circuits. However, this method still requires additional analog circuits for error measurement in the ADC core, and the accuracy of calibration depends on that of the built-in measurement circuits. The authors proposed a fully digital-calibration technique of capacitor mismatch for a redundant radix-2 pipelined ADC [9], [10], without on-chip error-measurement circuits. The technique is applied to a 10-bit ADC.

In this paper, a digital-calibration technique for high-resolution redundant radix-4 pipelined ADCs is proposed. Recently, pipeline ADCs with the radix-4 redundant digit set of \{-3, −2, −1, 0, 1, 2, 3\} have been reported [4], [16]. In these pipelined ADCs, each pipeline stage performs analog-to-digital subconversion (ADSC) with a redundant digit set of \{-3, −2, −1, 0, 1, 2, 3\} and multiplying digital-to-analog conversion with the gain of 4. The redundancy in the digit set of each pipelined stage leads to a relaxation of the comparator precision, and it is an indispensable technique for pipelined ADCs. The redundant radix-4 pipelined ADC is more efficient in power than that of the redundant radix-2 pipeline ADC [4]. A pipelined ADC with a minimum redundant digit set of \{-2, −1, 0, 1, 2\} is another possible architecture of power efficient ADC, although the tolerance to the comparator precision is smaller than that with \{-3, −2, −1, 0, 1, 2, 3\}. The use of redundant digit sets is originally discussed in computer arithmetic [16]. The digital calibration for the redundant radix-4 pipelined ADC is more complicated than that for the redundant radix-2 ADC. In the proposed calibration method, capacitor-mismatch errors of pipeline stages are measured using an integral nonlinearity (INL) plot for a ramp signal. There is no need for additional analog circuits for error measurement on the ADC chip. The capacitor-mismatch errors are calculated by an analytical relationship between the total error power due to the INL and the mismatch error. The error calculation requires a few steps of calculations. In each step, errors in each stage of the pipelined ADC are calculated independently using analytical formulas, and then errors are corrected using the calculated errors. The same procedure is repeated until the corrected INL error meets the specifications. Simulation results show that a few calculation steps are sufficient for the INL of less than 0.3 LSB in a 15-bit ADC.

In the following, the principle of error correction, the error calculation method, and the computer simulation results are described.

Manuscript received March 27, 2006; revised January 17, 2007. This work was supported by the Semiconductor Technology Academic Research Center (STARC).

The authors are with the Research Institute of Electronics, Shizuoka University, Hamamatsu 432-8511, Japan (e-mail: mfuruta@idl.rie.shizuoka.ac.jp).

Digital Object Identifier 10.1109/TIM.2007.904569
II. PRINCIPLE OF ERROR CORRECTION

Fig. 1 shows a system setup for the digital calibration. The ADC model is a redundant radix-4 pipelined ADC with on-chip digital error correction circuits. The error-measurement circuits consist of an error coefficient calculator and a ramp signal generator (SG).

The pipelined ADC consists of an input sample-and-hold (S/H) stage followed by a cascade of radix-4 pipelined ADC stages. Each pipelined stage consists of an ADSC and a multiplying digital-to-analog-converter (MDAC). The MDAC generates the residue for the following stage using a digital-to-analog subconverter and an S/H amplifier with gain of 4. To simplify the following analysis, we assume that the per-stage resolution of all the stages is the same.

A. Redundant Digit Sets

An interstage residue plot of a conventional radix-4 pipelined ADC is shown in Fig. 2(a). In pipelined ADCs, main sources of the nonlinearity error are gain errors due to capacitor mismatch, offset errors due to charge injection, and comparator offset errors [11]. If these errors do not exist, the output voltage $V_{\text{out}}(i)$ for the $i$th stage is given by

$$V_{\text{out}}(i) = 4V_{\text{in}}(i) - D_i V_{\text{ref}}$$  \hspace{1cm} (1)

where $V_{\text{in}}(i)$ is input voltage of the $i$th stage, $V_{\text{ref}}$ is reference voltage, and

$$D_i = \begin{cases} 3, & \text{if } V_{\text{in}}(i) \geq (1/2)V_{\text{ref}} \\ 1, & \text{if } (1/2)V_{\text{ref}} > V_{\text{in}}(i) > 0 \\ -1, & \text{if } 0 \geq V_{\text{in}}(i) > -(1/2)V_{\text{ref}} \\ -3, & \text{if } -(1/2)V_{\text{ref}} \geq V_{\text{in}}(i) \end{cases}$$

Fig. 2 shows a redundant radix-4 pipelined ADC residue plot. In this redundant radix-4 pipelined ADC, the $i$th stage digital

Fig. 2. Residue plot of radix-4 algorithm pipelined ADC. (a) Ideal. (b) With comparator offset.

Fig. 2(b) indicates an interstage residue plot for the case that the comparator offset exists. As shown in Fig. 2(b), the comparator offset results in a vertical shift in the transfer characteristic, and the output may exceed $V_{\text{ref}}$. Thus, the error results in a missing decision level.

Fig. 3 shows a redundant radix-4 pipelined ADC residue plot.
A comparator error is extraordinarily large. The tolerances of the algorithms with redundancy, missing decision levels are connected to the reference voltage sources, as shown in Fig. 5. In the next amplification and subtraction phase, the digital-calibration technique for redundant radix-4 pipelined ADCs is more advantageous than that in the pipelined ADC with \{-3, -2, -1, 0, 1, 2, 3\} is simply given by \(N_r \approx (2N + 1)\). For the N-stage ADC with \{-2, -1, 0, 1, 2\}, \(N_r \approx 2N + 0.4\). From the viewpoints of the comparator offset tolerance and the resolution, the radix-4 pipelined ADC with \{-3, -2, -1, 0, 1, 2, 3\} is more advantageous than that with \{-2, -1, 0, 1, 2\}. In the following, the digital-calibration method for the digital code set of \{-3, -2, -1, 0, 1, 2, 3\} is described. With a little modification, the presented method can also be used for the digital code set of \{-2, -1, 0, 1, 2\}.

In these algorithms with redundancy, missing decision levels due to the comparator error can be prevented unless the comparator error is extraordinarily large. The tolerances of the comparator error are \(\pm (1/16)V_{\text{ref}}\) and \(\pm (1/8)V_{\text{ref}}\) for the digital code sets of \{-2, -1, 0, 1, 2\} and \{-3, -2, -1, 0, 1, 2, 3\}, respectively. The digital dynamic range of N-stage redundant radix-4 pipelined ADCs with \{-2, -1, 0, 1, 2\} and \{-3, -2, -1, 0, 1, 2, 3\} are \(2/3(2^{2N+1} - 1/2)\) and \(2^{2N+1} - 1\), respectively. The relationship between the number of pipeline stages (\(N\)) and the number of resolution bits (\(N_r\)) in the pipelined ADC with \{-3, -2, -1, 0, 1, 2, 3\} is simply given by \(N_r \approx (2N + 1)\). For the N-stage ADC with \{-2, -1, 0, 1, 2\}, \(N_r \approx 2N + 0.4\). From the viewpoints of the comparator offset tolerance and the resolution, the radix-4 pipelined ADC with \{-3, -2, -1, 0, 1, 2, 3\} is more advantageous than that with \{-2, -1, 0, 1, 2\}. In the following, the digital-calibration method for the digital code set of \{-3, -2, -1, 0, 1, 2, 3\} is described. With a little modification, the presented method can also be used for the digital code set of \{-2, -1, 0, 1, 2\}.

### B. Gain and Offset Error Modeling

The basic operation of the MDAC is explained in Figs. 5 and 6. Although a fully differential switched-capacitor circuit is commonly used for pipelined ADCs, a single-ended circuit is dealt here to simplify the error analysis. Without any modification, the presented method can be used for the fully differential architecture. In the sampling phase, the input is sampled at the bottom plates of all capacitors \(C_1\), \(C_2\), and \(C_3\), as shown in Fig. 5. In the next amplification and subtraction phase, \(C_1\) is connected to the op-amp feedback path, and the other two capacitors are connected to the reference voltage sources, as shown in Fig. 6. The reference voltage to be connected is \(V_{\text{ref}}\), 0, or \(-V_{\text{ref}}\) depending on the digital output of the previous
The relationship stage. Table I shows the connection of the two capacitors during the amplification and subtraction phase. The relationship between input and output voltages with capacitor mismatch is given by

\[
V_{out} = \frac{C_1 + C_2 + C_3}{C_1} V_{in} - \left(\frac{D^{(1)}_1 + D^{(2)}_1}{C_1} + \frac{D^{(3)}_1}{C_1}\right) V_{ref} \\
= \frac{C_1 + C_2 + C_3}{C_1} V_{in} - \left(\frac{D^{(1)}_2}{C_1} + \frac{D^{(2)}_2}{C_1} + \frac{D^{(3)}_2}{C_1}\right) V_{ref} \tag{4}
\]

where

\[
D^{(1)}_i = \begin{cases} 
1, & \text{if } (3/8) V_{ref} \geq V_{in} > (1/8) V_{ref} \\
0, & \text{otherwise} \\
-1, & \text{if } -(1/8) V_{ref} > V_{in} \geq -(3/8) V_{ref}
\end{cases}
\]

\[
D^{(2)}_i = \begin{cases} 
1, & \text{if } (5/8) V_{ref} \geq V_{in} > (3/8) V_{ref} \\
0, & \text{otherwise} \\
-1, & \text{if } -(3/8) V_{ref} > V_{in} \geq -(5/8) V_{ref}
\end{cases}
\]

\[
D^{(3)}_i = \begin{cases} 
1, & \text{if } V_{in} > (5/8) V_{ref} \\
0, & \text{otherwise} \\
-1, & \text{if } -(5/8) V_{ref} > V_{in}
\end{cases}
\]

In the ideal case of \(2C_1 = 2C_2 = C_3\), the output voltage is

\[
V_{out} = 4V_{in} - (D^{(1)} + 2D^{(2)} + 3D^{(3)}) V_{ref}. \tag{5}
\]

Therefore, the digital code in (1), \(D_i\) is given by \(D_i = D^{(1)}_i + 2D^{(2)}_i + 3D^{(3)}_i\) for \(i\)th stage. The ideal output voltage \(V_{out}\) of this MDAC is referred to as the residue, the plot of which is shown in Fig. 4.

Errors due to the capacitor mismatch are defined as \(a_1 = C_2/C_1 - 1\) and \(a_2 = C_3/C_1 - 2\). Hence, (4) is expressed as

\[
V_{out} = (4 + a_1 + a_2)V_{in} + \left\{D^{(1)}_i(a_1 + 1) + D^{(2)}_i(a_2 + 2) + D^{(3)}_i(a_1 + a_2 + 3)\right\} V_{ref}. \tag{6}
\]

The gain error of the interstage switched-capacitor amplifier causes the output to be either larger or smaller than the conversion range of the following stage depending on whether the gain is larger or smaller, respectively, than the ideal gain. This results in positive differential nonlinearity (DNL) for the positive gain error and negative DNL for the negative gain error. Fig. 7(a) and (b) shows the effect of the gain error on the pipelined residue plot and the overall A/D conversion characteristic. The charge injection error also causes the overall offset error, such as shown in Fig. 7(c).

Fig. 8 shows an error analysis model of an \(N\)-bit pipelined ADC with offset and gain errors in the S/H stage and the MDAC. For simplicity, \(V_{out}, V_{in},\) and \(V_{ref}\) of the \(i\)th stage are denoted by \(x_{i+1}, x_i,\) and \(r,\) respectively.

The capacitor-mismatch errors \(a_1, a_2\) and the digital code \(D^{(1)}_i, D^{(2)}_i,\) and \(D^{(3)}_i\) of the \(i\)th stage are denoted by \(a_{1,i}, a_{2,i},\) \(D^{(1)}_i, D^{(2)}_i,\) and \(D^{(3)}_i\), respectively. If the gain error due to the capacitor mismatch and the offset error due to the charge injection \(b_i\) exist in the \(i\)th interstage amplifier, the \(i\)th stage output voltage is given by

\[
x_{i+1} = (4 + a_{1,i} + a_{2,i})(x_i + b_i) - \left\{D^{(1)}_i(a_{1,i} + 1) + D^{(2)}_i(a_{2,i} + 2) + D^{(3)}_i(a_{1,i} + a_{2,i} + 3)\right\} r. \tag{7}
\]

The digital code \(D_i\) is expressed as \(D_i = D^{(1)}_i + 2D^{(2)}_i + 3D^{(3)}_i\). The analog error due to the gain and the offset errors is given by

\[
e_i = (a_{1,i} + a_{2,i})x_i - \left\{D^{(1)}_i(a_{1,i} + 1) + D^{(2)}_i(a_{2,i} + 2) + D^{(3)}_i(a_{1,i} + a_{2,i})\right\} r + (4 + a_{1,i} + a_{2,i})b_i. \tag{8}
\]

The capacitor-mismatch errors are usually less than 1%. Therefore, assuming \(a_{1,i}, a_{2,i} \ll 4,\) the error can be simplified to

\[
e_i \cong (a_{1,i} + a_{2,i})x_i - \left\{D^{(1)}_i(a_{1,i} + 1) + D^{(2)}_i(a_{2,i} + 2) + D^{(3)}_i(a_{1,i} + a_{2,i})\right\} r + 4b_i. \tag{9}
\]

In the S/H stage, the output \(x_1\) having the gain error \(a_0\) and offset error \(b_0\) is expressed as

\[
x_1 = (1 + a_0)x_0 + b_0 \tag{10}
\]

with \(x_0\) as the input and the error is given by

\[
e_0 = a_0x_0 + b_0. \tag{11}
\]

In the digital correction, the errors as analog voltage are replaced by digital values of errors. In an \(N\)-stage ADC, the
digitized output value $X_0$ corresponding to the S/H input voltage $x_0$ is expressed as

$$X_0 = D_1 4^{-1} + D_2 4^{-2} + \cdots + D_{N+1} 4^{-N-1}$$  \hspace{1cm} (12)$$

where $D_i \in \{-3, -2, -1, 0, 1, 2, 3\} (i = 1, 2, \ldots, N+1)$.

The digitized error $E_0$ in the S/H stage is approximately given by

$$E_0 \approx A_0 X_0 + B_0$$  \hspace{1cm} (13)$$
where \( A_0 \) and \( B_0 \) are digitized values of gain error \( a_0 \) and offset error \( b_0 \), respectively. Although \( X_0 \) itself contains error, if the total error is small enough, the error in \( X_0 \) is negligible when it is used for the error correction. This is because \( E_0 \) can be approximated by \( A_0 X_0 + B_0 \), if \( A_0(X_0 - X_0) \ll 4^{-N} \), where \( X_0 \) is an ideal digital output without errors. The digitized error in the \( i \)th stage \( E_i (i \geq 1) \) is approximately given by

\[
E_i \approx (A_{1,i} + A_{2,i})X_i - \left\{ D_i^{(1)} A_{1,i} + D_i^{(2)} A_{2,i} + D_i^{(3)} (A_{1,i} + A_{2,i}) \right\} + 4B_i
\]

where \( A_{1,i}, A_{2,i}, \) and \( B_i \) are digitized estimates of \( a_{1,i}, a_{2,i}, \) and \( b_i \), respectively. Since \( X_i \) cannot be measured directly, \( X_i \) is approximated with the ADC output as

\[
X_i = D_i A^{-1} + D_{i+1} A^{-2} + \cdots + D_{N+1} A^{-N-i-1}
\]

for the digital error correction. Those approximations are valid for the digital calibration if the errors are small enough [12]. When the S/H stage and the first through the \( M \)th pipelined stages are calibrated, the overall digitized error is given by

\[
E = E_0 + E_1 A^{-1} + E_2 A^{-2} + \cdots + E_M A^{-M}
\]

\[
= A_0 X_0 + B_0 + \sum_{i=1}^{M} B_i A^{-i+1} + \sum_{i=1}^{M} \left\{ (A_{1,i} + A_{2,i})X_i - \left(D_i^{(1)} A_{1,i} + D_i^{(2)} A_{2,i} + D_i^{(3)} (A_{1,i} + A_{2,i}) \right) \right\} A^{-i}.
\]

The digital calibration is performed by subtracting \( E \) from \( X_0 \) in digital domain. The maximum nonlinearity error is reduced to 0.25 LSB by adding one more stage in the pipelined ADC if the digital correction is accurate enough.

### III. ERROR MEASUREMENT

The overall offset error \( E_{\text{os}} = B_0 + B_1 + B_2 A^{-1} + \cdots + B_M A^{-M+1} \) can be measured by giving zero to the ADC input. The S/H gain error \( A_0 \) is simply measured by giving \( \pm V_{\text{ref}} \) and taking the difference of the actual digital code from the ideal code. In case that the ADC has a parallel pipeline architecture, the corrections of gain and offset errors are essential. However, in single channel ADCs, these errors do not affect the ADC linearity [14].

In order to measure the gain errors due to capacitor mismatch, an INL plot of an ADC is used. The INL plot is obtained by giving a ramp signal to the ADC input using a high-resolution DAC, together with a digital ramp SG, as shown in Fig. 1. The digital-domain errors in each stage \( A_{1,k} \) and \( A_{2,k} (k = 1, \ldots, M) \) are determined using the cost function calculated with the mean square of the INL plot given by

\[
\eta = \frac{1}{2^{2N+1}-1} \sum_{i=1}^{2^{2N+1}-1} \text{INL}_i^2
\]

where \( \text{INL}_i \) is the INL of the \( i \)th digital code.

The error measurement is based on a fact that the relationship between \( \eta \) and each mismatch error has a quadratic function. To understand this relationship, the estimation of the \( k \)th stage capacitor-mismatch errors \( A_{1,k} \) and \( A_{2,k} \) is considered for the case that errors in the other stages coexist. The cost as a function of \( A_{1,k} \) and \( A_{2,k} \) is expressed as

\[
\eta(A_{1,k}, A_{2,k}) = \frac{1}{2} \int (E_k + E_{\text{other}})^2 dX_1
\]

\[
= \frac{1}{2} \int E_k^2 dX_1 + \frac{1}{2} \int E_k E_{\text{other}} dX_1
\]

\[
+ \frac{1}{2} \int E_{\text{other}}^2 dX_1
\]

where \( E_k \) is the capacitor-mismatch error due to \( A_{1,k} \) and \( A_{2,k} \), and \( E_{\text{other}} \) is the sum of other errors than \( A_{1,k} \) and \( A_{2,k} \). Using

\[
X_k = 4^{k-1} X_1 - \sum_{j=1}^{k-1} 4^{(k-1)-j} \left( D_j^{(1)} + 2D_j^{(2)} + 3D_j^{(3)} D_j^{(1)} \right)
\]

\[
\eta(A_{1,k}, A_{2,k}) \text{ is expressed as}
\]

\[
\eta(A_{1,k}, A_{2,k}) = A_{1,k}^2 \beta_{1,k} + A_{2,k}^2 \beta_{2,k} + 2A_{1,k} A_{2,k} \beta_{3,k}
\]

\[
+ A_{1,k} \beta_{4,k} + A_{2,k} \beta_{5,k} + \alpha_k.
\]

See Appendix A for the definition of \( \beta_{1,k}, \beta_{2,k}, \beta_{3,k}, \beta_{4,k}, \beta_{5,k}, \) and \( \alpha_k \). Equation (19) means that the cost function \( \eta(A_{1,k}, A_{2,k}) \) has a quadratic function of \( A_{1,k} \) and \( A_{2,k} \). Let us consider an ADC which has capacitor mismatches \( A_{1,k} \) and \( A_{2,k} \) at the \( k \)th stage. If the error correction is performed using error coefficients of \( A_{1,k}^s(c) \) and \( A_{2,k}^s(c) \), the cost function defined by \( \eta^c \) after the error correction as a function of \( A_{1,k}^s(c) \) and \( A_{2,k}^s(c) \) is given by [9]

\[
\eta^c(A_{1,k}^c, A_{2,k}^c) = \left( \hat{A}_{1,k} - A_{1,k}^c \right)^2 \beta_{1,k}
\]

\[
+ \left( \hat{A}_{2,k} - A_{2,k}^c \right)^2 \beta_{2,k}
\]

\[
+ 2 \left( A_{1,k} - A_{1,k}^c \right) \left( \hat{A}_{2,k} - A_{2,k}^c \right) \beta_{3,k}
\]

\[
+ \left( A_{1,k} - A_{1,k}^c \right)^2 \beta_{4,k}
\]

\[
+ \left( \hat{A}_{2,k} - A_{2,k}^c \right)^2 \beta_{5,k} + \alpha_k.
\]
This theoretical relationship suggests us a possibility to determine $\hat{A}_{1,k}$ and $\hat{A}_{2,k}$ from the measured data. In this case, the gain errors $A_{1,k}$ and $A_{2,k}$ can be calculated by searching the minimum of $\eta$. However, because of the correlation term [the second term of the right side of (18)], the calculated $A_{1,k}^{(c)}$ and $A_{2,k}^{(c)}$ as a result of searching minimum of (20) are not exactly equal to $\hat{A}_{1,k}$ and $\hat{A}_{2,k}$, respectively, unless $E_{\text{other}} = 0$. Therefore, iteration of error calculation is necessary. In each iteration, the theoretical relationship of (20) is used for the calculation.

There are eight unknown parameters of $A_{1,k}, \hat{A}_{1,k}, \beta_{1,k}, \beta_{2,k}, \beta_{3,k}, \beta_{4,k}, \beta_{5,k}$, and $\alpha_k$ in (20). If the calculation is successfully performed, $E_{\text{other}}$ finally approaches to zero. Therefore, in each iteration, we can once assume $E_{\text{other}} = 0$ to simplify the theoretical calculation. Hence, the (20) can be approximated as

$$\eta^{(c)}(A_{1,k}, A_{2,k}) \approx (\hat{A}_{1,k} - A_{1,k})^2 \beta_{1,k} + (\hat{A}_{2,k} - A_{2,k})^2 \beta_{2,k} + 2(\hat{A}_{1,k} - A_{1,k})(\hat{A}_{2,k} - A_{2,k}) \beta_{3,k}. \quad (21)$$

The validity of this assumption is confirmed in the simulations. Hence, parameters to be determined are reduced to $A_{1,k}, \hat{A}_{2,k}, \beta_{1,k}, \beta_{2,k}$, and $\beta_{3,k}$. If we have more than five simultaneous equations, $A_{1,k}, \hat{A}_{2,k}$ can be determined analytically, but using the measured $\eta^{(c)}$. The basic idea of determining $A_{1,k}, \hat{A}_{2,k}$ is similar to the method explained in [9] for the radix-2 case. To do this, error coefficients of $A_{1,k}^{(c)}$ and $A_{2,k}^{(c)}$ are once set to $(0,0), \eta^{(c)}(\Delta,0), \eta^{(c)}(-\Delta,0), \eta^{(c)}(\Delta,\Delta), \eta^{(c)}(-\Delta,\Delta), \eta^{(c)}(\Delta,-\Delta), \eta^{(c)}(-\Delta,-\Delta)$, and $\eta^{(c)}(\Delta,\Delta)$ with on-chip RAM, and the value $\eta^{(c)}(A_{1,k}^{(c)}, A_{2,k}^{(c)})$ is measured using the converter itself. Although value of $\Delta$ can be chosen arbitrarily, the reasonable choice is the maximum INL before the calibration. To calculate the unknown parameter $\beta_{1,k}$ at first, $\eta^{(c)}(\Delta,0), \eta^{(c)}(-\Delta,0)$, and $\eta^{(c)}(0,0)$ are calculated using (21) as

$$\eta^{(c)}(\Delta,0) = (\hat{A}_{1,k} - \Delta)^2 \beta_{1,k} + \hat{A}_{2,k}^2 \beta_{2,k} + 2(\hat{A}_{1,k} - \Delta)\hat{A}_{2,k} \beta_{3,k} \quad (22)$$

$$\eta^{(c)}(-\Delta,0) = (\hat{A}_{1,k} + \Delta)^2 \beta_{1,k} + \hat{A}_{2,k}^2 \beta_{2,k} + 2(\hat{A}_{1,k} + \Delta)\hat{A}_{2,k} \beta_{3,k} \quad (23)$$

$$\eta^{(c)}(0,0) = \hat{A}_{1,k}^2 \beta_{1,k} + \hat{A}_{2,k}^2 \beta_{2,k} + 2\hat{A}_{1,k}\hat{A}_{2,k} \beta_{3,k} \quad (24)$$

Using $d_1$ and $d_2$ defined as

$$d_1 = \eta^{(c)}(\Delta,0) - \eta^{(c)}(0,0)$$
$$d_2 = \eta^{(c)}(-\Delta,0) - \eta^{(c)}(0,0)$$

$\beta_{1,k}$ can be determined as

$$\beta_{1,k} = \frac{d_1 + d_2}{2\Delta^2}. \quad (25)$$

Similarly, using $d_3, d_4, d_5$, and $d_6$ defined as

$$d_3 = \eta^{(c)}(0,\Delta) - \eta^{(c)}(0,0)$$
$$d_4 = \eta^{(c)}(0,-\Delta) - \eta^{(c)}(0,0)$$
$$d_5 = \eta^{(c)}(\Delta,\Delta) - \eta^{(c)}(\Delta,-\Delta)$$
$$d_6 = \eta^{(c)}(-\Delta,-\Delta) - \eta^{(c)}(-\Delta,\Delta)$$

the parameters $\beta_{2,k}$ and $\beta_{3,k}$ are calculated as

$$\beta_{2,k} = \frac{d_3 + d_4}{2\Delta^2}$$
$$\beta_{3,k} = \frac{d_5 + d_6}{8\Delta^2}. \quad (26)$$

d_7 and d_8 are defined as

$$d_7 = \eta^{(c)}(0,-\Delta) - \eta^{(c)}(0,\Delta)$$
$$d_8 = \eta^{(c)}(-\Delta,0) - \eta^{(c)}(\Delta,0).$$

Using (21), $d_7$ and $d_8$ are expressed as

$$d_7 = 4\hat{A}_{2,k}\Delta\beta_{2,k} + 4\hat{A}_{1,k}\Delta\beta_{3,k}$$
$$d_8 = 4\hat{A}_{1,k}\Delta\beta_{1,k} + 4\hat{A}_{2,k}\Delta\beta_{3,k}$$

and from these equations, $\hat{A}_{1,k}$ and $\hat{A}_{2,k}$ are determined as

$$\hat{A}_{1,k} = \frac{\beta_{2,k}d_8 - \beta_{3,k}d_7}{4\Delta(\beta_{1,k}\beta_{2,k} - \beta_{3,k}^2)} \quad (27)$$

and

$$\hat{A}_{2,k} = \frac{\beta_{1,k}d_7 - \beta_{3,k}d_8}{4\Delta(\beta_{1,k}\beta_{2,k} - \beta_{3,k}^2)}. \quad (28)$$

Using the calculated errors of the first through $M$th stages, the error correction is performed, and the cost function is calculated again. The same procedure is repeated using the renewed cost function until the maximum INL meets the given specifications.

IV. COMPUTER SIMULATIONS

The validity of the proposed calibration method is confirmed by simulations. Although the error-measurement method is based on deterministic process, random numbers are used to evaluate the performance of the proposed error-measurement method. Random capacitor-mismatch errors are given to all the MDAC stages of redundant radix-4 pipelined ADCs using a
random number generator with Gaussian distribution. These capacitor-mismatch errors are treated as unknown, and these are calculated by the method explained in the previous section. In the tested 11-, 13-, and 15-bit ADCs, the number of stages of error correction are 3, 4, and 5, respectively.

Fig. 9 shows the DNL and the INL plots of the 15-bit redundant radix-4 pipelined ADC in three calibration steps. The number of pipeline stages is eight. Table II shows the list of assumed capacitor-mismatch errors. These values are generated with random numbers. The number of stages of error correction is five. The residual errors in each step and the resulting maximum INLs are shown in Table III. The maximum INL error is given by

$$\text{INL}_{\text{max}} = \max_{i=1}^{2^{N+1}-1} \{\text{INL}_i\}$$ (29)

where $\text{INL}_i$ is the INL of the $i$th digital code. In the initial step without calibration, all the error coefficients are zero, and the residual errors are the same as the internal errors themselves. In the second step, the maximum INL is reduced to 0.8 LSB. In the third step, the maximum INL is reduced from 15 LSB to less than 0.3 LSB without the initial calibration.

Recently, high-resolution A/D converters with digital resolution enhancement techniques are becoming popular [18], [19]. A digitally enhanced 15-bit A/D converter [18] has the maximum INL of 1.5 LSB. Although the results of this paper are obtained by simulations, and these cannot be directly compared to other works in which the data are measured by real chips, the maximum INL of 0.3 LSB achieved with the proposed digital-calibration method is good enough when compared to the state-of-the-art digital-calibration techniques.

The result of Table III is of a particular case of capacitor-mismatch errors. To confirm the effectiveness of the proposed error correction method for many different patterns of
FURUTA et al.: DIGITAL-CALIBRATION TECHNIQUE FOR REDUNDANT RADIX-4 PIPELINED ADCs

Fig. 10. Calculation step versus mean value of maximum INL (redundant radix-4 algorithm ADC).

Fig. 11. Calculation step versus mean value of maximum INL (value of standard deviation for random number generator is $3\sigma = 1\%$, $2\%$, and $4\%$).

For three different standard deviations of capacitor-mismatch errors, the total of 1000 different sets of capacitor-mismatch errors, which are randomly generated, are tried. The capacitor-mismatch errors are randomly added to the ADC models in each calibration; the average and the variance of the maximum INL are calculated by

$$\overline{\text{INL}}_{\text{max}} = \frac{1}{N_t} \sum_{j=1}^{N_t} \text{INL}_{\text{max}}(j)$$

(30)

$$\sigma^2_{\text{INL}_{\text{max}}} = \frac{1}{N_t - 1} \sum_{j=1}^{N_t} \left(\text{INL}_{\text{max}}(j) - \overline{\text{INL}}_{\text{max}}\right)^2$$

(31)

where $N_t$ is the number of trials. Fig. 10 shows the results of the averaged maximum INL as a function of the number of calibration steps for 11-, 13-, and 15-bit ADCs. The standard deviation of the capacitor mismatch in this case is $1/3\%$, or $3\sigma = 1\%$. In the 11-bit ADC, the error can be calculated without repetition. Even in the 15-bit case, two times of repetitions are sufficient. Figs. 11 and 12 are calculation results of mean value and standard deviation of maximum INL as a function of the number of calibration steps in the 15-bit pipeline ADC for three different standard deviations of capacitor-mismatch errors. Both the mean value and the standard deviation of the maximum INL are reduced by the calibration. However, for $3\sigma = 2\%$ and $4\%$, the maximum INL after calibration is limited to 0.6 and 0.76 LSB in average, respectively. This is because the digital error calibration is based on an approximated error correction given by (14). Therefore, for large capacitor-mismatch errors, the error due to the approximation is not negligible, and the resulting effect of error calibration becomes insufficient. However, the calibration method is still effective because high-resolution ADCs use relatively large capacitance in reducing thermal noise, and the capacitance mismatch can be less than $1\%$ as $3\sigma$ [17].

V. CONCLUSION

In this paper, a digital-calibration technique for redundant radix-4 pipelined ADCs is described. The proposed technique based on INL plot does not need to incorporate the calibration circuits into the ADC core, and hence, the high calibration accuracy is guaranteed. Although a few steps are necessary for high-resolution ADCs, the error calculation using analytical formulas of the INL error power is useful in simplifying the error measurements. The validity is confirmed by simulations. This method is useful for factory calibration.

APPENDIX

The mismatch errors in $k$th stage $E_k$ and the sum of other errors $E_{\text{other}}$ are expressed as

$$E_k = (A_{1,k} + A_{2,k})$$

$$\times \left\{ 4^{k-1}X_1 - \sum_{j=1}^{k-1} 4^{(k-1)-j} (D_j^{(1)} + 2D_j^{(2)} + 3D_j^{(3)}) \right\}$$

$$- \left\{ D_k^{(1)} A_{1,k} + D_k^{(2)} A_{2,k} + D_k^{(3)} (A_{1,k} + A_{2,k}) \right\}$$

$$E_{\text{other}} = \sum_{i=0}^{k-1} E_i + \sum_{i=k+1}^{M} E_i.$$
The first term in (18) is calculated as
\[
\frac{1}{2} \int_{-1}^{1} E_1^2 dX_1 = A_{1,k}^2 \beta_{1,k} + A_{2,k}^2 \beta_{2,k} + 2A_{1,k}A_{2,k} \beta_{3,k}
\]
where
\[
\beta_{1,k} = \frac{1}{2} \int_{-1}^{1} \left\{ 4^{k-1} X_1 - \sum_{j=1}^{k-1} 4^{(k-1)-j} \left( D_j^{(1)} + 2D_j^{(2)} + 3D_j^{(3)} \right) \right\}^2 dX_1
\]
\[
\beta_{2,k} = \frac{1}{2} \int_{-1}^{1} \left\{ 4^{k-1} X_1 - \sum_{j=1}^{k-1} 4^{(k-1)-j} \left( D_j^{(1)} + 2D_j^{(2)} + 3D_j^{(3)} \right) \right\}^2 dX_1
\]
\[
\beta_{3,k} = \frac{1}{2} \int_{-1}^{1} \left\{ 4^{k-1} X_1 - \sum_{j=1}^{k-1} 4^{(k-1)-j} \left( D_j^{(1)} + 2D_j^{(2)} + 3D_j^{(3)} \right) \right\}^2 dX_1.
\]

The second term in (18) is calculated as
\[
\frac{1}{2} \int_{-1}^{1} (E + E_{\text{other}})^2 dX_1 = A_{1,k} \beta_{4,k} + A_{2,k} \beta_{5,k}
\]
where
\[
\beta_{4,k} = \int_{-1}^{1} \left\{ 4^{k-1} X_1 - \sum_{j=1}^{k-1} 4^{(k-1)-j} \left( D_j^{(1)} + 2D_j^{(2)} + 3D_j^{(3)} \right) \right\} E_{\text{other}} dX_1
\]
and
\[
\beta_{5,k} = \int_{-1}^{1} \left\{ 4^{k-1} X_1 - \sum_{j=1}^{k-1} 4^{(k-1)-j} \left( D_j^{(1)} + 2D_j^{(2)} + 3D_j^{(3)} \right) \right\} E_{\text{other}} dX_1.
\]

The last term in (18) is defined as
\[
\alpha_k = \frac{1}{2} \int_{-1}^{1} E_{\text{other}}^2 dX_1.
\]
Shoji Kawahito (M’86–SM’00) was born in Tokushima, Japan, in 1961. He received the B.E. and M.E. degrees in electrical and electronic engineering from Toyoohashi University of Technology, Toyohashi, Japan, in 1983 and 1985, respectively, and the D.E. degree from Tohoku University, Sendai, Japan, in 1988.

In 1988, he was with Tohoku University as a Research Associate. From 1989 to 1999, he was with Toyohashi University of Technology. From 1996 to 1997, he was a Visiting Professor with Eidgenössische Technische Hochschule Zürich, Zurich. Since 1999, he has been a Professor with the Research Institute of Electronics, Shizuoka University, Hamamatsu, Japan. His research interests are in mixed analog/digital circuit design for imaging and sensing devices and systems.

Dr. Kawahito received the Outstanding Paper Award at the 1987 IEEE International Symposium on Multiple-Valued Logic, the Special Feature Award in Large-Scale Integration Design Contest at the 1998 Asia and South Pacific Design Automation Conference, Beatrice Winner Award at the 2005 IEEE International Solid-State Circuits Conference. He is a member of the Institute of Electronics, Information and Communication Engineers of Japan, the Institute of Image Information and Television Engineers of Japan, and the International Society for Optical Engineering.

Daisuke Miyazaki (S’97–M’02) was born in Tokushima, Japan, in 1974. He received the B.E. and M.E. degrees in information and computer sciences from Toyohashi University of Technology, Toyohashi, Japan, in 1997 and 1999, respectively, and the Ph.D. degree from Shizuoka University, Hamamatsu, Japan, in 2002.

From 2002 to 2005, he was a Research Associate with the Research Institute of Electronics, Shizuoka University. He was with the Semiconductor Business Group, Sony Corporation, Atsugi, Japan, in 2005. His design work includes high-resolution ADCs and its implementation of mixed-signal system-on-a-chips.