PLL Jitter Analysis with Various Power Delivery Networks on a Board

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Abstract

Increasing frequency and reducing time margin have made designs of power delivery networks (PDNs) on board to be an integral part of chip designs. Power delivery network designs are usually achieved by mounting the decoupling capacitors on power plates so that the designed power impedance is relatively lower on the interested frequency ranges. But, some parts out of frequency-dependant impedance profile of power delivery networks that make the major effect on noise performances of digital, RF, and analog chips does not be very clear according to chip’s family. In this paper, we demonstrate the analysis of power delivery networks for the multiple voltage domains on an analog PLL jitter performance.

We look for self impedances of chip mounted on board according to decoupling capacitor's size, their positions, and DC-DC chip. We analyze the PLL’s jitter characteristics depending on self-impedance profiles for core and IO circuit. Through this work, it is clear that the PDNs design concept which is considering inherent operation characteristics should be adapted for the efficient and costive system.

Introduction

The commercial trend in the electrical market requires the chips to be integrated of different IPs like analog, RF, digital for higher performance and more complicated functions. Another requirement in the market is that it must be committed for battery-operation, i.e., to low power. Two requirements can be achieved by 1) allocating optimum operation voltage levels and operation frequency of each IPs [1-5] and 2) designing proper power domains. Generally, these approaches are spreading in chips fabricated with deep-submicron technology. Consequently increasing power domains under high performances and small design area constraints make the design of chip and board difficult, especially on low cost mobile terminals.

Major issues of these systems’ design complexities are power integrity and proper consumptions of passive elements and PCB layers. The on-board power integrity, i.e., the capability of delivering the needed powers with the requested noise-free voltage levels, becomes the paramount importance in the design of all high complex and high performance board system and must be studied at the early design stage [6]. But, in the view of cost-efficient design, the overdesign by overestimation of a generated power noise level and noise effect on the chip performance should be prevented.

In this paper, we demonstrate the on-board PDN design for high performance analog PLL including several design components such as decoupling capacitors, their values and positions, and the VRM. Through this work, we show that the cost-effective PDN design can be achieved when the board designer knows the detailed chip characteristics, with simulations and measurements.

Simulations and Measurements

The effect of a board PDN on PLL jitter performance is tested by separating the power domains for analog part, digital part, and IO circuitry, i.e., of 1) PLL core circuits including the closed-loop path and the VCO, 2) some digital control logic, and 3) high speed IO circuitry.

Fig. 1 shows the test board for jitter performance simulation. The power supplier is connected near the position B on the board and decoupling capacitor is mounted on position A or B with different capacitances. The board is designed with a PWR/GND plane of two middle layers in total 4-layer stacks. Fig. 2 shows the block layout of the fabricated PLL chip. The other digital blocks are also included in this chip but not displayed here. The jitter performance is evaluated as shown in Fig. 3. The simulated peak-to-peak jitters are measured with stimulating sinusoidal noises with amplitude of +/-5%VDD only on analog PLL power domain. The simulated output frequency is 1GHz. In Fig. 3, the jitter performance is very sensitive within the range between 1M~20M because of the closed-loop bandwidth and the VCO phase noise. Fig. 4 shows the self impedance of analog PWR/GND on the chip according to decoupling capacitors’ values and positions illustrated in Fig. 1. Although the case of no decoupling capacitor mounted on a board is worst in overall frequency range, the case of 0.5uF is mounted at position A has worse impedance characteristic within a critical range in the dotted circle. The resulted outputs are shown in Fig. 5. The rank of the jitters depends on the impedance characteristic of a critical frequency range, and their values in the dotted circle are independent on decoupling capacitors. In conclusion, the proper PDN design doesn’t mean the lower impedance overall frequency range but it’s more effective in case of a PDN design which makes the impedance of highest sensitive frequency domains more lower. Even if decoupling capacitor is not properly used, the performance is more degraded; more than the case of no decoupling capacitor.

Fig. 6 shows the fabricated test board for PLL jitter performance evaluation, and Fig 7 shows its brief modeling schemes. In this test feature, we evaluate the IO noise effect on PLL jitter performance and make different PDN architectures for IO circuitry. Fig. 7(a) is a brief model with the PLL and DC-DC module and Fig. 7(b) is a brief model with the PLL.
Fig. 7(c) is a modeling configuration of the test module including de-coupling capacitors. The module is constructed with two signal layers and 4-GND/PWR layers as one GND plate and 3 PWR planes of PLL analog, PLL digital, and PLL IO circuits. The PDNs are modeled with tiled cells based on PEEC model.

First, we test how much the VRM as an IO power supplier can reduce the noises and jitters. Fig. 8 shows the self impedance curves of analog, digital, and IO circuits when DC-DC turns on and off. The simulated results are the same plots. It means that the possibility of the state of DCDC can’t affect the noise figures. As a result, Fig. 11 shows no differences according to DCDC on and off. Second, the difference with or without decoupling capacitor of “47uF” on PLL IO PDN is illustrated in Fig. 9. The self impedance of IO circuitry shows the different values about not only high frequency ranges but also low frequency ranges. It is already expected because the high capacitance can’t affect the impedance of high frequency ranges. But, the effect of self impedances at the low frequency ranges on high speed IO noise or jitter performance was not clearly mentioned.

Fig. 10 shows the measured maximum power noises of IO power domains on the on board. The major difference of two measurement configurations is whether the “47uF” capacitor is mounted or not on the board. The “no 47uF” case (model in Fig 7(b)) shows more severe noise values than those of “47uF” (model in Fig. 7(a)). From Fig. 9, it is not clear that the noise increase according to operation frequency is generated only by high speed IO clock transitions because it is possible that the self impedance near critical operation frequency domain is a major factor to make a long term period noise. Fig. 11 shows the measured jitters for above mentioned in three cases. Compared with Fig. 10 and Fig. 11, the PLL jitter performance does not seem to depend directly on the noise levels on PLL IO PDNs.

From above simulation and test results, two important facts can be dragged, 1) we should concentrate the self impedance of PDNs within critical frequency domains in which chip is more sensitively affected and 2) for PDN design for high speed IO circuitry, the self impedance of low frequency also a considerable design factor to improve the jitter performance.

From this evaluation, the cost-effective and efficient PDN design can be possible if board designer knows the detailed chip operation at a design early stage of PDN.

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Conclusions
In this paper, we evaluate the design issues between self impedances of PDNs and jitter performances. The chip power domains are constructed with three different voltages for PLL core circuits like VCO and charge pump, PLL digital circuits, and high speed IO circuits. More detailed analysis is performed with simulation on PLL analog circuit part and for collaborated effects of IO noises on a jitter performance, because separated power supplier with the VRM and external power supplier for IO circuits is devised and their jitter performances are compared through simulation and measurement.

From above simulation and test results, two important facts can be dragged, 1) we should concentrate the self impedance of PDNs within critical frequency domains in which chip is more sensitively affected and 2) for PDN design for high speed IO circuitry, the self impedance of low frequency also a considerable design factor to improve the jitter performance.

References
Fig. 1. Test board for jitter simulation.

Fig. 2. PLL layout

Fig. 3. Peak-to-Peak jitters of the designed PLL vs. noise frequencies. The noise amplitude is given as sinusoidal signals with +/-5% amplitude of VDD, and the jitter is measured at output clock frequency of 1GHz.

Fig. 4. Self impedance of chip by decoupling capacitor on the board of Fig. 1.

Fig. 5. Simulated jitter performances according to mounting decoupling capacitors as without board decoupling capacitor, with board decoupling capacitor(500nF) at position A, with board decoupling capacitor(5uF) at position A, and with board decoupling capacitor(500nF) at position B.

Fig. 6. Fabricated test board for PLL jitter performance.
Fig. 8. Test board simulation of Fig. 6. When the DCDC chip tuned off.

Fig. 9. Test board simulation in case of that the VRM components of 47uF capacitor and 4.7nH inductor are demounted.

Fig. 10. Maximum power noises according to PLL clock frequency when DC-DC turns on or off.

Fig. 11. The peak-to-peak jitters according to PLL clock frequency.