Hybrid CMOS-MQCA Logic Architecture using Multi-Layer Spintronic Devices

Jayita Das, Syed M. Alam, Srinath Rajaram, Sanjukta Bhanja

Abstract—We present a novel hybrid CMOS-MQCA architecture using multi-layer Spintronic devices as computing elements. A feasibility study is presented with 22nm CMOS where new approaches for spin transfer torque induced clocking and read-out scheme for variability-tolerance are introduced. A first-of-its-kind Spintronic device model enables circuit simulation using existing CAD infrastructure. Approximately 70\% reduction in energy consumption is observed when compared against conventional field-induced clocking scheme.

Index Terms—Magnetic Quantum Cellular Automata, MQCA, CMOS, Multi layer, Spintronic, novel, MTJ, Spin Valves, Switching current, Clocking current, Low Power, Verilog-A, magnetostatic, TMR, GMR, Magnetoresistance, Differential Output, Read out, Spin transfer torque induced, Nonvolatile, Non destructive, variability, Standard Cell, Controlled Cell, Ferro coupling, Antiferro coupling, Generic Regular Hybrid.

I. INTRODUCTION

The scaling of CMOS down to sub-micron regime has raised considerable concerns about the leakage power and variance tolerance of a circuit. With the increase of interconnect resistance as a result of scaling, signal delay through them also increases. Magnetic Quantum Cellular Automata (MQCA) is a potential candidate for addressing some of the aforementioned shortcomings in deep sub-micron design. By using the inherent properties of magnetic materials, MQCA has demonstrated reliable logic circuit performance at room temperature.

Recent developments in Spin Transfer Torque (STT) induced switching in Magnetic Tunnel Junctions (MTJs), a multi-layer Spintronic device, make them promising candidates as constituent elements in MQCA architecture. Their unique property to be switched with the application of a suitable current can be utilized for feeding the inputs to the architecture. High tunnel magnetoresistance (TMR), indicating the resistance difference between logic 0 and 1 states, observed in certain classes of MTJs increases the sense margin of their read circuitry. To our knowledge, we are the first to utilize the dipolar coupling between the free layers of neighboring MTJs to perform logic computation (see Fig. 1 over and above read-write necessity. We have performed a multi-layer micromagnetic simulation of a majority AND operation (see Fig. 2) using LLG simulation suite [1]. MTJs were separated by 20nm. Note that the coupling was already known to the memory community but was treated as a hindrance to the memory density. These reliable properties justify the use of MTJs as elements for non-volatile logic computation in hybrid CMOS-MQCA structures with zero static power.

In this paper, we have explored a novel MQCA architecture using a multi-layer Spintronic device that offers us better controllability on the cells of the architecture. We have introduced logic computation through dipolar interaction between the free layers of neighboring Spintronic devices in conjunction with STT induced clocking. In addition to designing the fundamental operations, such as input, output, and clocking, we have developed the necessary Spintronic device model to enable circuit level simulation of any logic function using existing CAD infrastructure. Rest of the paper is organized as following: Section II reviews the prior work in conventional MQCA based logic architecture and computational techniques. Our proposed Generic Regular Hybrid CMOS-MQCA architecture, implementing complete state-full logic with co-existent memory and computation ability within cells, is described in Section III. Input scheme to the hybrid CMOS-MQCA architecture using STT induced write operations is presented in Section IV. A novel differential sensing scheme for the MQCA outputs with high tolerance to variability is proposed in Section V. The read circuit, performing a low power non-destructive sensing, is designed and simulated in 22nm predictive CMOS technology [2]. Section VI discusses the STT induced clocking technique introduced in our architecture to aid state propagation between neighboring cells. A Verilog-A model of the Spintronic device cell is designed and discussed in Section VII. This is the first reported model to our knowledge to emulate the interaction among the neighboring Spintronic cells using a Finite State Machine (FSM), and at the same time, enabling write, read, and clocking of an individual cell fully utilizing the underlying physics. Finally, Section VIII
substantiates our claims of design modularity, energy, and area optimization through supporting simulated and computed data. The novelty of our work lies in

1) proposing a hybrid CMOS-MQCA architecture that enhances modularity and introduces cell selectivity in clocking.
2) integrating 22nm CMOS with multi-layer Spintronic devices to realize the hybrid architecture using optimum number of metal layers.
3) proposing a spin-induced clocking where a cell is clocked by a short positive voltage pulse needed to drive the cell to precision state. The computing occurs post-precision.
4) using Spin Transfer Torque induced input writing and leveraging from MQCA architecture to obtain variability-tolerant differential outputs for nondestructive sensing
5) a Verilog-A model, for physics-based characteristics of the Spintronic cell, integrated with an FSM to model the dipole neighbor interaction.

II. REVIEW OF MQCA

Traditionally, MQCA comprises of a matrix of single layer permalloy disks or nanomagnets; each exhibiting single-domain behavior. An anisotropy in the shape of these magnetic cells gives them an energetically favorable direction of magnetization along their easy axis or largest dimension. The hard axes of the cells are along their shorter dimensions and contribute to the energy maxima in their energy landscape [3]. The two distinct magnetic orientations of the cells are suitably used in representing logic 0 and 1 in circuit operation. The magnetization of the cell can be switched between these two energy minimum states through suitably applied external fields. Furthermore, dipolar interaction between multiple neighboring cells also influences the final state. Once the cell switches to one of the energetically favorable magnetization direction, it retains its state until the next clock signal is applied to it.

Various experimental demonstrations of logical components like majority [4], NAND/NOR [5], AND/OR [6] have been presented for MQCA logic. Performing the fundamental operations in MQCA array, such as clocking the cells for state propagation, supplying inputs, and sampling computed outputs, for any complex logic implementation is a challenge due to power consumption and difficulty of integration of the underlying circuits. Clocking the magnets for perfect ordering is in general performed by field-induced clocking [7], [8], [9], [10] except in the experimental demonstration in [6] that uses a rotating magnetic field. Magnitude of current required in these clocking schemes, to generate a high enough magnetic field, is high, in the order of milli-Ampere. Most of prior work have reported static inputs and outputs observed through magnetic force microscopy. Recently, MQCA systems were driven by on-chip input field current [11] where 680 mA were reported for an easy axis to easy axis switching (not using clock). The experimental read-out [12] was shown by trapping domain wall of a neighboring wire. In [13] researchers have experimentally demonstrated the feasibility of integrating MTJ with MQCA for resistance measurements. Alternate low power and better controlled input, output, and clocking schemes with back-end CMOS circuitry are the motivations of our work.

There is a critical need to integrate input, output and clocking schemes with CMOS in order to realize a feasible future 2020 and beyond CMOS successor. In [14], authors have reported a non-volatile implementation of a hybrid CMOS-MTJ full-adder using 34 transistors and 4 MTJs to perform the operation. The design requires storing one of the inputs to the adder in the MTJ while the other input is fed externally into the CMOS circuitry. However, this work suffers from many of the pitfalls of CMOS scaling due to physical electrical interconnects and offers much less flexibility in design. Contrary to prior work, our study is the first effort to use multi-layer Spintronic devices as individual computing elements so that we can leverage from the Spin Transfer Torque (STT)
induced current switching and the integration with low power CMOS, at the same time using the interaction between devices to compute and propagate information. Most importantly, this work is the first step to offer localized control of individual elements of MQCA architecture.

III. REGULAR HYBRID CMOS-MQCA ARCHITECTURE

Fig. 3 shows a novel hybrid CMOS-MQCA architecture implementing a half-adder logic function without the loss of generality. In this array the multi-layer Spintronic devices are arranged in a regular 2D grid. The horizontal and vertical pitch of the grid is constrained by the neighbor interaction from top, right, bottom and left. The 2D grid consists of an ensemble of majority logic blocks for AND/OR implementation, ferro-/anti-ferro interconnects and differential output generator blocks. The fixed cell in the majority logic is either set to logic 0 or 1 depending on AND/OR operation between the inputs to the majority logic. The presence or absence of a cell at a particular lattice site in the hybrid CMOS-MQCA architecture is determined by the underlying logical function. The cells in the 2D grid are broadly categorized into

- **Input cells** - Cells with a nmos access transistor underneath them and marked in green (A, B and their complements) in Fig. 3. These cells accept inputs to the hybrid CMOS-MQCA architecture. They are never clocked.

- **Standard cells** - Cells without access transistor and are connected directly across the bit and source lines through vias. These cells are marked in yellow in Fig. 3. All the standard cells in a row are clocked together.

- **Controlled cells** - Cells with access transistors for selective clocking based on word line voltage. The controlled cells can be sub-categorized into Ordinary Controlled cells and Output cells marked in blue and red, respectively, in Fig. 3. The Output cells are subset of the controlled cells with additional connections to the readout circuit.

The anti-ferromagnetic interconnects used for horizontal information propagation are realized through horizontal placement of Standard cells (horizontal wire in Fig. 3) with a pitch of 70nm. The ferro-magnetic interconnects are implemented through vertical placement of cells (vertical wire in Fig. 3) with a pitch of 120nm. The maximum number of cells in any interconnect is limited to 4 owing to existing clocking limitation [10]. Using the Differential Output Generator of the logic grid and its variability reduction feature, pairs of output cells and their complements are read simultaneously by the sensing circuitry discussed later in Section V. The sequence of rows or columns that needs to be selected for clocking is decided by row and column decoders, at the periphery of the circuitry, according to the logic to be performed. In Fig. 3, the architecture realizes the sum output S of a Half-Adder operation.

The 2D grid of hybrid CMOS-MQCA array is suitable for fabrication with CMOS devices underneath the Spintronic devices. Fig. 4 shows a cross-section view along the easy axis of three neighboring cells. The cross-section view represents three vertically located cells in the majority logic elements in Fig. 3. The free layers at the top are connected to individual bit lines located in metal layer 2. The pinned layer of the Input and Controlled cells are connected via metal layer 1 to the source of the access transistor beneath each. The Standard cells, on the other hand, have their pinned layer connected to a source line in metal layer 1. The poly gates of all the access transistors in a column are connected by a continuous poly line and can be strapped through a word line situated in metal layer 3 at the periphery of the array. In our study, the MQCA array is built of multi-layer Spintronic devices (MTJs) of 100nm×50nm footprint with 20nm horizontal and vertical spacing between neighbors. We first investigated which CMOS technology node is suitable for the hybrid CMOS-MQCA array. Spintronic device pitch requirement is restrictive to achieve neighbor interactions. Existence of only one nmos access transistor in a 2×2 cell area, as evidenced in Fig. 3, relaxes CMOS transistor pitch requirement (to achieve high W/L ratio for enhanced current drive and low ON resistance of the access transistors). The metal layer 1 pitch is maintained at 70nm while the metal layer 2 and metal layer 3 pitches are 120nm and 140nm each (see Fig. 3). The values are well within the specifications for 22nm CMOS technology node [15], thus substantiating our claim for the practical feasibility of the hybrid architecture at 22nm or below.

IV. STT-INDUCED INPUT SCHEME

The input to the generic array architecture is fed by writing an Input Cell comprising of an access transistor connected to the Spintronic device as shown in Fig. 5. Furthermore, all the Input cells are in the same column sharing a vertical word line. This enables providing all the inputs to the hybrid CMOS-MQCA architecture in parallel at the start of the computation, thereby augmenting computation speed. All the inputs to the architecture are written in either one of the two initial and consecutive Global pulses, of positive and negative polarity, applied across the appropriate bit and source lines. The shared word line is raised high during both the occasions to select their access transistors. All the inputs that need to be written to AP state are written during the first pulse. The second pulse writes their complements. Eqn. [16] determines the threshold value of switching current, \( I_s \), for the cell while Eqn. [17] calculates the duration \( \tau \) of the current pulse,
required to effectively switch the cell.

\[
I_c = \frac{2e}{h\eta} \alpha \mu_0 V M_s (H_c + 0.5 M_s)
\]

\[
\tau = \frac{1}{\alpha \mu_0 \gamma M_s} \ln \left( \frac{\pi}{2\theta_0} \right)
\]

where \(\alpha\) is damping constant, \(\mu_0\) is the permeability of free space, \(M_s\) is saturation magnetization of switching layer (free layer), \(V\) is the volume of the layer, \(\eta = p/(1+p^2)\) for parallel-to-anti-parallel (P-to-AP) switching and \(\eta = p/(1-p^2)\) for AP-to-P switching and \(p\) is the spin polarization, \(H_c\) is strength of in-plane magnetic anisotropy and the term \(0.5 M_s\) is due to demagnetizing effect. \(\gamma\) is the gyromagnetic ratio while \(\theta_0\) is the initial angle of magnetization between the free and the pinned layer. A current of magnitude \(I_{c,AP}\) or greater is passed from the bit line to source line (referred as positive current) to write the cell to anti-parallel (logic 1) state. A current of magnitude \(I_{c,P}\) or greater is passed from the source line to bit line (referred as negative current) to write the cell to parallel (logic 1) state. This is similar to writing conventional Spintronic devices [18].

V. TMR-BASED READOUT SCHEME

The reasonably high value of TMR in MgO based MTJs and their intrinsic dependence on bias voltage, gives a wide difference in the resistance of the cell between the parallel and anti-parallel states near zero-bias voltage [19]. This resistance difference is effectively utilized in reading the output of the MQCA architecture. Furthermore, we have proposed a novel Non-Destructive Low Power Differential ReadOut scheme leveraging the characteristics of the hybrid CMOS-MQCA architecture (in MQCA, we have bit and bit spatially adjacent) for a high tolerance to variability. The ReadOut circuit is illustrated in Fig. 6. A symmetry is aimed among the transistors in the two arms of the circuit. The reading of the cell is carried out in two consecutive phases Pre-charge phase followed by Sensing phase as shown in the simulated waveforms Fig. 7 (\(M_{1a,1b,2a,2b}\) and \(M_{3a,3b}\) are access transistors of the output cells \(S_a, S_b\) and their complements \(\bar{S}_a, \bar{S}_b\), respectively. The access transistors remain on (\(\phi_1 = 1\)) during the entire read operation.

During the Pre-charge phase, the \(\phi_2\) signal is pulled low thereby turning off transistors \(M_3\) and \(M_4\). The active low signal \(\phi_3\) is pulled down to assist in fast pre-charge of the nodes \(X\) and \(Y\) to a potential \(V_{dd}\). Signal \(E_q\) is raised high to equalize nodes \(X\) and \(Y\) through transistor \(M_5\). During the sensing phase, \(\phi_2\) is raised to a low voltage, say \(V_{read}\), for applying a low voltage bias on the MTJs. With \(E_q = 0\) and \(\phi_3 = 1\), voltage differences start to grow at nodes \(X\) and \(Y\) due to differential current from the complementary output states. The Comparator senses the potential across the nodes \(X\) and \(Y\) and accordingly the output \(O/P\) is made high or low.

*The key characteristics of our Readout schemes are:*

- **Differential Output Reading:** This technique utilizes the inherent property of MQCA architecture to readily produce the complement of a bit through anti-ferromagnetic coupling.

- **Low Power Non-destructive read:** In order to read the contents of the Output Cells a very small current, in the range of 4-5 \(\mu\)A, is supplied to the cells. This ensures reading the cells at very low voltage bias, thus facilitating the effective utilization of high TMR for the sensing operation. A low read current through the cells rules out any possibility of their switching during Read.

- **Variability Tolerance:** In the nanometer regime, any variations that creep in the cell dimensions can have a profound impact on the cell parameters. We have proposed a Variability Tolerant Read Architecture by reading pairs of cells (\(S_a, S_b\)) and their complements (\(\bar{S}_a, \bar{S}_b\)) simultaneously as shown in Fig. 6 Sensing standard deviation is reduced by a factor of 1.4 compared to a simple differential approach. The area and temporal
cost associated with this improvement is minimal.

VI. STT-INDUCED CLOCKING

Contrary to field-induced clocking using overhead Copper (Cu) wires [7], we have proposed a novel way of clocking the cells in the array that provides us with better control and selectivity over the cells, thereby optimizing power and area. In a Spin Transfer Torque induced switching device, when a positive current flows through the device, the damping force acts in opposition to the spin transfer torque in the free layer [18], which is routinely used in oscillators. An appropriate choice of current can equalize the forces and take the device into Precession. Soon after the current is released, the device switches to the energetically favorable direction under the influence of any magnetic field external to the device. We have utilized this concept and implemented the STT-induced clocking mechanism for our cells in the hybrid CMOS-MQCA architecture.

The cells in the body of the logic are clocked using a discretely progressing positive Precession pulse, applied in sequence across the selected source and bit lines (see Fig. 8). This pulse is preceded by the two Global Write Pulses applied indiscriminately to all the cells in the body of the logic. The two Global pulses (positive followed by negative), ensures that all the cells in the body of logic are switched to the Parallel or Logic ‘0’ state at the start of computation. This time instant is labeled as \( T_1 \) in Fig. 8. Next, the logic computation and propagation takes place with the help of the series of Precession pulses applied to rows of cells in the sequence of logic computation (see Fig. 8). The cells in the next clock zone are set to precession when the clock for the current zone is released so that the cell’s state is only influenced by neighbors in the previous clock zone.

The scheme introduces selectivity into the architecture through two sets of cells - Standard cells and Controlled cells. In a horizontal wire once the clocking pulse is released, the anti-ferromagnetic coupling among the cells retains the clocked state until a change in the state of the wire’s input propagates down the wire by pushing the next cells off their precession state [10].

Cells in a vertical wire are clocked by applying separate voltage pulses across the source and bit lines of the rows constituting the wire. The clocking pulse for a vertical wire is released sequentially in the direction of information propagation. For a vertical wire the ferro-magnetic coupling opposes the precession state if the clocking pulse for all the cells are released simultaneously [10], therefore, mandating a sequential release of clock for a vertical wire. The information propagation in vertical wire takes place similar to horizontal wire. A Controlled Cell is clocked by selecting its access transistors while corresponding bit and source lines are pulsed. It helps in selectively clocking cells in a row only when required, thus saving power.

VII. SPINTRONIC DEVICE MODEL FOR HYBRID CMOS-MQCA SIMULATION

A Verilog-A model of the Spintronic cell that emulates the STT-induced switching and clocking behaviors as proposed in the paper is developed. In addition to physics-based equations for MTJ fundamental characteristics, such as critical switching current, voltage dependant state resistance and TMR, [16] [20] [19], our Verilog-A model is the first of its kind to emulate the dipolar coupling between the free layers of neighboring cells through a Finite State Machine (FSM). Fig. 9 depicts a cell’s interaction with its neighbors.

The salient features of the model are outlined below:

- A cell switches its state only under the influence of its immediate neighbors to its top, left, bottom and right.
- The cell’s interaction with its neighbors is modeled through four dual-bit bi-directional magnetic ports A, B, C, and D as in Fig. 9.
– One of the four ports serves as the output of the cell depending on the direction of information propagation. The output port declares the state of the cell: Parallel\((00)\), Anti-parallel\((11)\) and Clocked / Precession\((10/01)\).

– The other three magnetic ports serve as the inputs for the cell, and plays the deciding role in the cell’s state right after the cell is clocked.

• When the state of a cell, under the influence of its neighbors, is undeterministic, the ferromagnetic coupling from top and bottom neighbors decides the cell’s state.

• A cell when in clocked state is considered to have no influence on its neighbors.

The influencing neighbors and the cell’s behavior under their influence is modeled through two types of cells -

• **Horizontal Cell** that emulates information propagation in horizontal direction using bitwise operation by

\[
D = B \cdot C + \overline{A} \cdot (B \oplus C)
\]

When made to simulate a horizontal wire, the top and bottom inputs to the cells are fixed to anti-parallel and parallel state or otherwise, so that each cell is influenced by only the neighbor to its left/right depending on the direction of information propagation to the right/left.

• **Vertical Cell** similarly computes its state under the influence of its neighbors using bitwise operation by

\[
D = B \cdot C + \overline{A} \cdot (B \oplus C)
\]

The entire MQCA architecture can be realized using proper interconnects of the two types of cells. The details of the Verilog-A model and FSM algorithms are omitted from the paper due to space limitation. The model is thoroughly tested and verified using different voltage pulses and different combinations of inputs in Cadence design environment. The model will be freely available to the scientific community to assist in the simulation of hybrid CMOS-MQCA logic.

**VIII. PERFORMANCE ANALYSIS**

The cell characteristics in the proposed hybrid CMOS-MQCA architecture are summarized in Table I along with switching, clocking or precession, and read current values and durations. The values are theoretically computed using Eqn. 1 and Eqn. 2 or simulated when appropriated (for e.g. read). With a resistance of 2K offered by the cell in the parallel state and a TMR of 100 for a MgO based MTJ cell, the anti-parallel state offers a resistance of 4K. A half-adder is designed within the specifications of the hybrid architecture. A full-adder is designed using the half-adder as modules. The full adder templates are then instantiated to develop a 8-bit ripple carry adder and a 8x8 array multiplier, thus supporting the modularity in design.

Table II presents the delay, energy and area in the above-mentioned circuits. The total energy consumed is computed using our proposed STT-induced clocking as well as field-induced clocking techniques for comparison. A 4mA current \((t_{clk} = 10\, ns)\) [7] is assumed for field-induced switching. Table ?? validates our claim of STT-induced clocking as an energy efficient clocking technique over traditionally used field-induced clocking for logic computation along with high selectivity of cells in the body of the logic. A 70 – 75% reduction in energy consumption is observed using STT-induced clocking.

Furthermore, as seen from Eq. 1, the switching current decreases in proportion as the Spintronic devices (MTJs) are scaled down. So does the energy consumption of the circuit. But the reverse effect occurs for field-induced clocking with scaling [21] that is used in the most of the prior work discussed in Section II.

**IX. CONCLUSION**

This work highlights the selectivity of cells offered and the power improvement through STT-induced clocking in a novel hybrid CMOS-MQCA architecture using multi-layer Spintronic devices (MTJs). The feasibility of the architecture with 22nm or below CMOS technology is studied. The fast, low power and non-destructive Readout circuit demonstrates robustness against variability by leveraging inherent properties of the hybrid CMOS-MQCA architecture. The modularity of design block helps in the realization of larger circuits. With the scaling of underlying CMOS, the overlying Spintronic cell dimensions will reduce leading to lower switching current and overall reduction in computation energy in future. A Verilog-A model of the Spintronic device has been developed and is available for others to explore novel hybrid CMOS-MQCA circuits.

**REFERENCES**


### Table I

<table>
<thead>
<tr>
<th>Cell Dimension</th>
<th>100x50x2 mm²</th>
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<tr>
<td>Horizontal pitch</td>
<td>70nm</td>
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<tr>
<td>Vertical pitch</td>
<td>120nm</td>
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### Table II

<table>
<thead>
<tr>
<th>Logic function</th>
<th>Delay ((ns_{clk} + w_{ap}))</th>
<th>Energy ((STT-induced Clocking))</th>
<th>Energy ((Field-induced Clocking))</th>
<th>Area ([\mu m²])</th>
</tr>
</thead>
<tbody>
<tr>
<td>Half-Adder</td>
<td>4+2</td>
<td>78.5nJ</td>
<td>237pJ</td>
<td>0.41</td>
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<tr>
<td>Full-Adder</td>
<td>8+2</td>
<td>278pJ</td>
<td>1015pJ</td>
<td>1.9</td>
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<tr>
<td>32-bit Ripple Carry Adder</td>
<td>256+2</td>
<td>8.9nJ</td>
<td>32.5nJ</td>
<td>60.8</td>
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<tr>
<td>8x8 array multiplier</td>
<td>60+2</td>
<td>15.2nJ</td>
<td>57nJ</td>
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