A 5 GHz fully integrated ESD-protected low-noise amplifier in 90 nm RF CMOS


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Abstract

A 5.5 GHz fully integrated low-power ESD-protected low-noise amplifier (LNA), designed and verified in a 90 nm RF CMOS technology, is presented for the first time. This 9.7 mW LNA features a 13.3 dB power gain with a noise figure of 2.9 dB, while maintaining an input return loss of −14 dB.

Keywords: 90 nm, RF CMOS, LNA, and ESD

Introduction

Several emerging applications for portable electronic devices are being introduced primarily due to the availability of high data rate wireless local area networks. While classic CMOS technology nodes were previously not seriously considered for RF applications, the deep sub-micron technologies could offer an alternative solution and designer freedom. For instance, in the 90 nm CMOS technology node, transit frequencies well over 100 GHz has been achieved [1], and the commercial manufacturing options are increasingly becoming available. However, with downsizing also the maximum allowed voltage over transistors decreases, placing severe restrictions on analog design options. Recently, the realization of a 100 GHz Voltage-Controlled Oscillator (VCO) in 90 nm CMOS [2] has put CMOS in the mm-wave design. The design of a 5 GHz LNA and VCO [3][4] validated this technology node for low-voltage low-power, high performance RF front-ends. Further, with the decrease of gate oxide thickness, CMOS circuits get more sensitive to stress from electrostatic discharge (ESD), e.g. by contact with human body. In this sense, circuits that are connected to the outside world via their inputs are usually most exposed to ESD stress.

In RF systems, the LNA is usually connected to the outside world through the antenna. In addition, it is one of the most critical building blocks in any RF front-end. Therefore, the design and validation of the nominal performance and ESD robustness in state-of-the-art CMOS technologies is highly relevant.

In this paper, the design and verification of a 5 GHz CMOS LNA with ESD protection in a 90 nm RF CMOS technology is presented for the first time. This LNA is protected against ESD up to 1.4 A Transmission Line Pulse (TLP) current [11], corresponding to 2 kV HBM stress. Further, it has a power consumption of 9.7 mW, a power gain of 13.3 dB, and a noise figure of 2.9 dB, while maintaining an input return loss of −14 dB. The input 1 dB compression point is -11.5 dBm, the third-order input referred intercept point (IIP3) is −2.7 dBm, both at 5.5 GHz.
stage, power is saved and degradation of linearity is prevented.

The power-constrained noise optimization technique by Shaeffer et al. [7], including the impact of the non-quasi-static input resistance [8], has been used to get an initial estimation of the aspect ratio and overdrive voltage of M1.

The input and output nodes of the LNA are protected against ESD by the use of inductors (L_{ESD}) between these nodes and the ground. These inductors shunt away the hazardous ESD current from the core LNA circuit. Grounded gate NMOS transistors, typically used as ESD protection devices, are used as power clamps (M_{ESD}). In this way, all possible pin combinations are protected against ESD as required from ESD reliability point of view. More details on the ESD protection behavior can be found in [9].

At resonance, the ESD inductor compensates leftover parasitic capacitances (RF pad, decoupling capacitor Cc…). Similar approaches have been published before in 0.25 µm CMOS, however using only simulations and without any silicon verification [10]. Moreover, in that work off-chip components and the on-chip ESD inductor were integrated in the matching network. In this work, the ESD on-chip inductor has been added after the design of the core LNA circuit, minimizing the impact on the LNA performance. In other words, this LNA also operates well when L_{ESD} is omitted, as will be illustrated further with the LNA’s noise figure measurement results. Finally, capacitances C_{DEC} are used for power supply decoupling.

**Layout**

Fig. 2 shows the micrograph of the LNA. The circuit area is 940 x1000 µm². Both the input NMOS M1 and cascode NMOS M2 have an aspect ratio of 110 µm/90 nm. The multi-fingered transistors have their gates contacted on both sides in order to reduce the noise contribution from the gate resistance. All inductors are implemented on-chip with a grounded patterned poly-shield. The top 2 copper metal patterns were shunted with vias for the inductors in order to create a thick top metal level of approximately 1.3 µm. The inductors used are: 0.4 nH for L_s, 4.3 nH for L_G, and 1.1 nH as load inductor, the measured quality factors (Q) at 5 GHz are 8.8, 7, and 7.8. The ESD inductors at input and output nodes have an inductance value of 3 nH, with a Q of 6.5 at 5 GHz. The chosen value is a compromise between noise figure degradation, input matching and ESD robustness of the LNA.

**Experimental results**

The LNA has been measured on wafer. The gain with the LNA drawing 8.1 mA from a 1.2 V supply voltage is 13.3 dB at 5.5 GHz, and 13.4 dB at the peak (5.43 GHz), as shown in Fig. 3. The 3-dB bandwidth is 1350 MHz (4.68-6.03 GHz); the 1-dB bandwidth is 691 MHz (5.035-5.726 GHz). The reverse isolation for the LNA is approximately –30 dB within the bandwidth. Further, an input reflection of –14.2 dB (= S_{11}) is measured at 5.5 GHz (Fig. 4). A small upward shift in frequency is observed in the S_{11} curve, with a minimum return loss of –38 dB at 5.99 GHz. This is due to an inaccurate model of the source degeneration inductor, as proven by re-simulations with updated models. However, still a good input matching is obtained over the entire operation 3-dB bandwidth of the LNA: a reflection coefficient from –6.15 at 4.68 GHz to –33 dB at 6.03 GHz.

An output reflection coefficient of –19 dB is measured at 5.5 GHz, and a minimum return loss of –21.7 dB at 5.46 GHz, as shown in Fig. 4. An output reflection below –4 dB is obtained over the entire 3-dB bandwidth of the LNA.

![Fig. 2 LNA micrograph](image)
The noise figure of the ESD protected LNA at 5.5 GHz, in nominal operation, is 2.95 dB, as shown in Fig. 5. The minimum noise figure of 2.9 dB occurs at 5.2 GHz. An identical LNA, but without the ESD-inductors, was also measured at the same power consumption. The noise figure decreased with about 0.25 dB, because of absence of the ESD inductor at the input.

In order to investigate the nonlinear behavior of the LNA, the 1-dB compression point is measured by sweeping the RF power of the applied signal. At 5.5 GHz the compression point occurs at –11.5 dBm input power as shown in Fig. 6. The compression point over the entire operating range is shown in Fig. 7. The measurements to extract the third–order input referred intercept point (IIP3) are shown in Fig. 8. An IIP3 of –2.7 dBm has been obtained. These results demonstrate that a high dynamic range and a good linearity have been obtained in this design.

The Transmission Line Pulse (TLP) [11] technique has been used to characterize the ESD robustness of the LNA. TLP pulses up to 1.4 A were applied at the input, positive with respect to ground, and no RF degradation was observed after ESD stress. This level corresponds to about 2 kV Human Body Model (HBM) ESD protection. The power clamps can withstand up to 1.6 A TLP, corresponding to 2.5kV HBM.

State-of-the-Art

To compare the performance of our LNA to other designs, different figures of merit (FOM) that are common in literature, are used. The performance summary of the LNA, and a comparison with other fully integrated CMOS LNAs operating in the 5 GHz band, are shown in Table 1. The FOMs do not include the ESD performance. However, to the authors’ knowledge, this work is the first published fully integrated 5.5 GHz LNA with ESD protection.

A first figure of merit (FOM₁) for low-power RF amplifiers is the ratio of the gain in dB to the DC power consumption. The LNA described in this paper has a value of 1.38 for this FOM. This high value is achieved due to use of 90 nm CMOS technology. Further, this FOM can be extended to include the noise figure of the LNA as follows

\[
FOM_1[\text{mW}^{-1}] = \frac{\text{Gain}[\text{dB}]}{(\text{NF} - 1)[\text{abs}] \cdot P_{\text{DC}}[\text{mW}]}
\]  

Brederlow, et al, [12] proposed a FOM that also includes IIP3, and operating frequency fC as follows

\[
FOM_2[-] = \frac{\text{Gain}[\text{abs}] \cdot \text{IIP3}[\text{mW}] \cdot f_C[\text{GHz}]}{(\text{NF} - 1)[\text{abs}] \cdot P_{\text{DC}}[\text{mW}]}
\]
A 5.5 GHz fully integrated, low-power LNA with ESD protection was designed and verified experimentally in a 90nm RF CMOS technology. This state-of-the-art LNA features a power consumption of 9.7 mW, a 13.3 dB power gain with a noise figure of 2.9 dB, while maintaining an input return loss of –14 dB. The 3-dB bandwidth is 1.35 GHz (641 MHz 1-dB bandwidth). The input 1 dB compression point is –2.7 dBm. To the authors’ knowledge, this work is the first published fully integrated 5.5 GHz LNA with ESD protection.

Specifications
- Gate length: 0.09 μm
- Gate oxide thickness: 1.2 nm
- Supply voltage: 1.2 V
- Power consumption: 9.7 mW
- Gain: 13.45 dB
- Noise figure: 2.90 dB
- 3-dB bandwidth: 1.35 GHz
- Input 1 dB compression point: –2.7 dBm
- Intercept point (IIP3): –11.5 dBm
- Return loss: –16.2 dB
- Input return loss: –14 dB
- Output return loss: –14.2 dB
- 5th order intermodulation: –30 dBm
- ESD protection: 3-kV HBM
- Operation at 5.5 GHz

The authors would like to thank EU IMPACT IST-2000-30016 project and the Flemish IWT for their support, the IMEC PLINE for processing of the wafers, Andries Scholten from Philips Eindhoven for MOS Model 11 parameter extraction, Luc Pauwels for measurement assistance, and Johan Mees for all the design environment support.

### Table 1 Summary of measured LNA performance and state-of-the-art fully integrated 5 GHz LNAs

<table>
<thead>
<tr>
<th>Name</th>
<th>Gate length</th>
<th>Supply voltage</th>
<th>Power consumption</th>
<th>Gain</th>
<th>3-dB BW</th>
<th>S11 (dB)</th>
<th>S22 (dB)</th>
<th>S12 (dB)</th>
<th>FOM1</th>
<th>FOM2</th>
<th>FOM3</th>
<th>ESD-Protection</th>
</tr>
</thead>
<tbody>
<tr>
<td>This Work</td>
<td>0.09</td>
<td>1.2</td>
<td>9.7 mW</td>
<td>13.45</td>
<td>-15</td>
<td>-14</td>
<td>-30</td>
<td>-11.5</td>
<td>1.38</td>
<td>0.51</td>
<td>1.51</td>
<td>2</td>
</tr>
<tr>
<td>W. Jeamsaksiri [3]</td>
<td>0.09</td>
<td>1.2</td>
<td>9.7 mW</td>
<td>13.45</td>
<td>-15</td>
<td>-14</td>
<td>-30</td>
<td>-11.5</td>
<td>1.38</td>
<td>0.51</td>
<td>1.51</td>
<td>2</td>
</tr>
<tr>
<td>D. Linten [4]</td>
<td>0.09</td>
<td>1.2</td>
<td>9.7 mW</td>
<td>13.45</td>
<td>-15</td>
<td>-14</td>
<td>-30</td>
<td>-11.5</td>
<td>1.38</td>
<td>0.51</td>
<td>1.51</td>
<td>2</td>
</tr>
<tr>
<td>T. K. K. Tsang [16]</td>
<td>0.25</td>
<td>1.2</td>
<td>10 mW</td>
<td>13.45</td>
<td>-15</td>
<td>-14</td>
<td>-30</td>
<td>-11.5</td>
<td>1.38</td>
<td>0.51</td>
<td>1.51</td>
<td>2</td>
</tr>
<tr>
<td>H.W. Chu [13]</td>
<td>0.25</td>
<td>1.2</td>
<td>10 mW</td>
<td>13.45</td>
<td>-15</td>
<td>-14</td>
<td>-30</td>
<td>-11.5</td>
<td>1.38</td>
<td>0.51</td>
<td>1.51</td>
<td>2</td>
</tr>
</tbody>
</table>

### Conclusions

- A 5.5 GHz fully integrated, low-power LNA with ESD protection has been designed and verified experimentally in a 90nm RF CMOS technology. This state-of-the-art LNA features a power consumption of 9.7 mW, a 13.3 dB power gain with a noise figure of 2.9 dB, while maintaining an input return loss of –14 dB. The 3-dB bandwidth is 1.35 GHz (641 MHz 1-dB bandwidth).
- The input 1 dB compression point is –2.7 dBm. To the authors’ knowledge, this work is the first published fully integrated 5.5 GHz LNA with ESD protection.
- Performance parameters such as gain, noise figure, power consumption, and input return loss have been achieved simultaneously with on-chip input and output matching networks and ESD protection.

### Acknowledgements

- The authors would like to thank EU IMPACT IST-2000-30016 project and the Flemish IWT for their support, the IMEC PLINE for processing of the wafers, Andries Scholten from Philips Eindhoven for MOS Model 11 parameter extraction, Luc Pauwels for measurement assistance, and Johan Mees for all the design environment support.

### References