Power Management and Delivery for High-Performance Microprocessors

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ABSTRACT
This paper provides an introduction to advanced power management and delivery techniques that have been employed in leading microprocessor designs. The techniques need multiple voltage rails supplied by independent voltage regulators. We provide justification for near-load regulators and explain the practical challenges associated with the regulator integration.

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B.7.0 [Hardware]: Integrated Circuits General

General Terms
Performance, Design

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Voltage regulators, power management, microprocessors, power delivery.

1. INTRODUCTION
Aggressive technology scaling has enabled very high transistor integration capacity. Complex functions are integrated into hardware with multiple heterogeneous cores and caches. Managing total power consumption has emerged as the most challenging task in today’s highly complex microprocessor systems. Independent per-core dynamic voltage/frequency scaling (DVFS) is proven to be an effective way to minimize power consumption. It needs multiple voltage rails supplied by independent voltage regulators on the platform.

We provide an introduction to power management techniques that have been employed in leading designs in Section 2. It is followed by justification for near-load voltage regulators (VR) as a possible solution. Section 3 attempts to explain the practical design considerations and challenges associated with regulator integration in microprocessor systems.

1.1 Power Trends
Aggressive technology scaling has enabled integration of billions of transistors on a single die to enable high-performance multi-core servers, heterogeneous multi-core client processors and small form factor handheld devices. The ever-increasing transistor density has led to decreasing wire widths, increased current density, higher supply currents, larger transients, and large die sizes while lowering both the supply \( V_{MIN} \) and \( V_{MAX} \) of operation. Off-die dimensions, such as die-package interface, are not shrinking at the same rate. This has led to high power densities, high power consumption, strict supply impedance targets and expensive metal stacks.

Figure 1: Power Delivery Requirements and Effects
Figure 1(a) includes the slew rate trends on a high-performance server processor. It is exceeding 100A/nS and causing three distinct voltage droops on microprocessor die, as shown in Figure 1(b). The largest of those, known as the first droop is due to on-die capacitance and on-package inductance in the power delivery network.

2. MICROPROCESSOR POWER MANAGEMENT
DVFS is a well-known power reduction technique employed in current multi-core products offered by major microprocessor vendors.

Figure 2 shows multiple supply domains on two recent 32nm Intel® microprocessors. The latest Itanium™ processor requires 10+ independent voltage rails [1] while the second generation Core™ processor includes 3 independent rails, two of which were scaled dynamically [2]. Off-chip voltage regulator modules (VRM) supply these voltage rails from motherboard to socket to package to the die with various forms of bulky and expensive decoupling capacitors and power routing planes in the system.

Figure 2: Power Domains on 32nm Microprocessors
2.1 Recent Techniques

The obvious solution to the platform level power delivery problem is to have an efficient VR on the motherboard with switching FETs, inductors for conversion, capacitors to control droops, and a low resistance path to socket with minimal communication with load die. Top metal layers on the die are dedicated to power distribution and hence made very thick compared to the rest. Dedicated power and ground tracks are added on every metal layer with opportunistic on-die device decap placement.

To mitigate non-ideal power delivery requirements, a concept of load line was established for VRMs. It follows a linear V-I supply characteristic to satisfy triple operating voltage constraints for $I_{\text{MAX}}$, $I_{\text{MIN}}$ and thermal design power ($I_{\text{TD}}$) conditions. VRMs also employ active voltage positioning (AVP) to maintain the supply at the low voltage point of the 3rd droop to expose the system only to “excess” 1st droop beyond the 3rd droop.

First generation Core™ processors included adaptive clocking, integrated per-core gate powers to minimize standby leakage and a Power Control Unit (PCU) to optimize power across various states of operation. The PCU was a proprietary 32-bit microcontroller. Temperature, current and power sensors on the die feed the information to PCU which in turn decided on the power gating algorithm. PCU also communicated to external regulator control and accepted OS inputs [3].

3. NEAR-LOAD VOLTAGE REGULATORS

For efficient DVFS, the microprocessors require multiple independent variable voltages to the die that can be changed by mV increments. e. g. Equation (1) explains a sample 6.25mV $V_{\text{STEP}}$ for a 7-bit voltage identification (VID) code that is sent from a processor to a motherboard VRM.

\[
\frac{V_{\text{MAX}} - V_{\text{MIN}}}{V_{\text{VDD}}} = (1.3V - 0.5V) \times 2^2 = 6.25mV
\]

In addition to VID requests, the VRM is also supposed to compensate the voltage droops. In case of the 1st and 2nd droops the VRM is too far to respond effectively. Hence voltage regulators should be placed as close to the die as possible.

3.1 Conversion Benefits

If a second stage VR is inserted between a motherboard VRM and a microprocessor die, the VRM can provide low supply current at high output voltage, thereby reducing the VRM to 2nd stage VR impedance significantly. Figure 3 shows the benefits for different voltage conversion ratios for an assumed conversion efficiency of 85% [4]. VRM current, off-chip decoupling requirement and resistive losses decrease significantly with the voltage ratio.

If the VR is integrated on the package or in a microprocessor die, it improves the load response. Small parasitic capacitances in the VR to load power delivery network enable switching frequencies of 100MHz+ [7]. Due to miniaturization of the overall solution, including power FETs and passive components, complex multiphase designs are easily implemented for droop mitigation.

3.2 Regulator Topologies

The VRM on the motherboard converts a battery output or AC-DC brick output to die voltages. The voltage conversion is one aspect of the design and regulating the die voltage to 6.25mV resolution is another aspect. Three most common topologies for near-load VRs are linear [5], switched capacitor [6] and inductor-based buck regulators [7]. The description of the individual topologies is out of scope for this paper and the reader is referred to [3] for detailed explanation. Linear regulation achieves fine resolution by manipulating device $R_{\text{on}}$ while buck regulators do this by adjusting the duty cycle of power FET inputs. Switched capacitors are easy to integrate for high to low voltage conversion, but switch capacitor based regulators lack the fine resolution ability. It can be achieved at the expense of loss of efficiency or complex topologies.

4. INTEGRATION CHALLENGES

Near-load VRs seem to be the panacea for all of the power management and power delivery problems, but they require practical design considerations, and pose engineering and financial challenges for integration in high volume products. We describe some of the issues in this section.

System-Level Requirements: Integrated VRs must conform to all the VID, adaptation, and droop response requirements. They have to interact with power control signals, satisfy DVFS and thermal throttling requests.

Testability: The silicon-integrated VRs should be testable across the entire voltage range. They may require power noise injectors.

Across-Load Efficiency: VRs are designed to provide high efficiencies at higher current loads. They suffer from light load inefficiency. Load-adaptive phase or driver shedding is required for reasonable light load efficiency.

Power FETs: If the incoming voltage is higher than 2$^{\text{nd}}$ $V_{\text{MAX}}$, high-voltage tolerant FETs may be necessary.

Incoming Power Delivery: The on-die routing from the bumps to integrated VRs is as important as the VR output power routing. It is challenging to route high currents in high device density areas.

Passives: IF high-Q inductors or capacitors are integrated, they should be area efficient. If inductors are processed with on die magnetics [8], additional processing is involved.

Thermal considerations: Integrated VRs will typically occupy 10% of the load die area. The current delivery system at the output of VR should not cause thermal hotspots.

Total cost of integration: Near-load VRs will require changes in devices, passives, package, and also in HW-SW interface. The incurred cost by all of these changes should reduce
system-level energy consumption to reduce the total system level cost.

5. CONCLUSIONS
Advanced power management techniques are employed in high power microprocessor systems and low energy handheld products. Near-load voltage regulators are the key enablers for future products, however, they pose some design challenges. Voltage regulator integration is the wave of the future, but it has to be done in the right way.

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7. REFERENCES


