Chip-to-chip interconnections based on the wireless capacitive coupling for 3D integration

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Abstract

Chip-to-chip interconnection, based on wireless communication by capacitive coupling was investigated. This innovative approach will considerably reduce the pitch of the pin and strongly help in the implementation of a dense network of interconnects, while improving inter-chip bandwidth and power dissipation. The 3D integration technology based on aligned wafer-to-wafer direct bonding technique was implemented for IC capacitive interconnection realization. The capacitive structures are created by facing two wafers with symmetrical IC chips bearing at last level a two-dimensional array of metal arms covered by a dielectric layer. Communication take place by capacitive coupling using capacitors created at location in the aligned micro-array. The capacitance dielectric thickness was monitored during the wafer bonding. Specific wafer process flow and especially precise circuit alignment were applied; in order to create between the bonded chips the capacitive interconnect arrays. After bonding, one wafer was thinned down, and I/O via were opened though the piled up remaining silicon and the two bonded stacks of CMOS structures. That elaborated structure was then ready for wire bonding. Electrical characterization tests are performed and the first functional testing gives very good performances in high-speed communication between the stacked chips.

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1. Introduction

To meet the ever-increasing demands of ULSI circuits with high performance in terms of chip size, power consumption, integration of heterogeneous technologies in one single die and lower cost, new 3D IC technologies are emerging.

3D concept has been a subject of interest for many years and was reported by Akasaka in 1986 [1] considering that the ultimate IC structure consists in the stacking of active IC layers and insulating materials. The latest progress in wafer bonding and heterogeneous material integration in ICs technology enabled this demonstration [2].

In this paper, we present for the first time the electrical results and a technological approach for 3D integration at the wafer level, applied to a demonstrator achievement, able to connect two separately processed CMOS wafers via capacitive interconnections [3]. One of the possibilities to realize the capacitive interconnections is the direct wafer bonding via capacitor dielectric layer. This is obtained at the last metal passivation layer, after its adaptation to the molecular direct wafer bonding needs [4,5]. The implementation of the technological steps for 3D integrated interconnection will be compatible with advanced IC technology and able to support the requirements previously stated.
2. Experimental

2.1. Capacitive interconnects circuit development

Capacitive connections do not provide DC signal propagation; for that reason, specific receiver and transmitter are required, and their synchronization strategy is a key issue for the interface design: these circuits could be synchronized by specific signals or remain fully asynchronous [6]. In this work, the former approach is implemented: communication can be optimized, thanks to synchronism information, by performing a level-to-edge conversion inside transmitter, and also by biasing receiver in the highest gain state (as explained in next section). This approach represents a valid strategy in order to increase interconnection sensitivity and to deal with the trade-off (due to channel attenuation $\text{CCC} / (\text{CCC} + \text{CRX}, \text{Fig. 1})$) between receiver performance and interconnection size. For these reasons, the interface includes a clock propagation buffer in order to provide synchronization between receivers and transmitters. This device is fully asynchronous and its design is not crucial about size and power because just one of these circuits is required to control many of the synchronous ones.

To sum up, we present a vertical interconnection interface, where many capacitive interconnections are used for parallel general-purpose signal propagation, with the basic functionality granted by a reduced number of synchronization elements. For these targets, a symmetric core has been designed, with data receivers on one side and transmitters on the opposite one. The capacitive electrodes have been designed in different sizes ($25 \times 25 \mu m^2$, $15 \times 15 \mu m^2$ and $8 \times 8 \mu m^2$) for the capacitive coupling evaluation and the capacitive interconnections are arranged in $3 \times 3$ clusters in order to evaluate inter-electrode crosstalk. The communication circuits are small enough to be laid out under the smallest electrode.

For I/O connections purposes, three sided digital incremented pad-frame has been included for the 3D structures, in order to open the via thought the stacked interfaces and reach the pad extensions of two stacked chips.

2.2. 3D integration process development

Standard CMOS wafers, processed in 0.13 $\mu m$ technology and provided by STMicroelectronics, were used for the capacitive interconnection elaboration by a 3D integration approach. The layout of the considered chips was at the last metal level, adapted to the symmetrical considerations in face-to-face wafer aligned bonding. Unfortunately, the global die floor plane had an insufficient symmetry configuration for a wafer-to-wafer alignment in eight inches wafers technology. For this reason the eight inches CMOS wafers were cut at four inches standard dimensions to recover mirror symmetry. Thus, the prepared wafers followed the assembly process at four inch wafer level integration as illustrated in Fig. 2a. This process flow allowed us to obtain the demonstrator architecture, see Fig. 2b. To reach these interface requirements for wafer bonding, an additional low temperature PECVD SiO$_2$ film was deposited on the passivation layer and then planarized by chemical-mechanical polishing (CMP). At the same time, the dielectric thickness was monitored, for a precise capacitance stack architecture achievement. For this, the processed faces of each pair of CMOS wafers were aligned, with a top to bottom precision using SUSS – BA6 set-up, then associated by direct bonding.

The bonding quality and alignment accuracy controls were checked by infrared (IR) microscopy, as shown on the picture in Fig. 3a and b.

The bonded wafers sandwich, was then thinned down and polished from one side. In Fig. 4a and b, is shown the optical and infrared camera view of the bonded and thinned down wafer sandwich.

The thinning down of the upper Silicon wafer was stopped at up to 30 $\mu m$, above the CMOS patterns. For needs of demonstrator characterisation, this side of wafer has been used for I/O connections. The dry plasma etching through the Silicon and stacked CMOS dielectrics was the most adapted solution in order to reach a good via quality and I/O pads metal integrity. The schematically represented cross section of bonded CMOS wafers after the via etching down to the input and output metal pads level is represented in Fig. 5a, and Fig. 5b gives the global wafer view of etched structure after the photoresist stripping.

3. Results and discussion

The wafer-to-wafer integration process applied to the standard processed CMOS wafer for vertical integration was successfully achieved using direct bonding. Bonding interface quality (see Fig. 6) was evaluated by bonding
energy measurements using Maszara’s method [7], before the upper wafer surface thinning. The bonding energy was estimated between 600 and 800 mJ/m², the estimated values are comparable with the results obtained for thermal oxide bonding energy stabilized at the same temperature [4].
Successfully opened via for the I/O pads connections and excellent interface adhesion during the stacked wafers dicing, allowed to package the chips on the adapted to test ceramics — Fig. 7a and b. Non conventional conditions for the wires bonding due to the small via dimensions and top wafer Silicon surface was implemented by ST Microelectronics packaging team.

The feasibility of the presented architecture was demonstrated by electrical test of stacked chips with a 1.2 V power supply.

In Fig. 8a and b is shown the interface electrical test, which has been provided in order to have low speed
input–output and high-speed 3D data transmission. The functionality of the three different types of clusters has been demonstrated at 25 MHz and shows a very good performance for the three different dimensions of 3D integrated communication capacitances.

4. Conclusion

Vertical integration was achieved for the capacitive coupling structure implementation between two CMOS standard processed wafers. After appropriate surface conditioning, the wafers were precisely aligned, with ±1 µm accuracy and directly bonded via the adjusted dielectric layer for the capacitance implementation. One backside of the bonded sandwich wafer was thinned down. The stacked by this technology structure is able to be diced and packaged or to receive the next wafer for a direct bonding and supplementary stage level integration in 3D structure.

For the capacitive interconnection demonstrator testing, we have carried out the I/O via opening through the thinned Silicon and stacked CMOS structure of the both wafers. The I/O access to the test structure of the communication capacitor was achieved by wires bonding on the ceramic. The first capacitive interconnections performances of the 3D integrated chips have very promising characteristics and can be considered as a first step for Terabit chip integration.

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References


Further Reading