A CHAOTIC TIME-DELAY SAMPLED-DATA SYSTEM AND ITS IMPLEMENTATION

MÜSTAK E. YALÇİN, RAMAZAN YENİÇERİ and SERDAR ÖZOĞUZ
Department of Electronics and Communication Engineering
İstanbul Technical University,
İstanbul, Maslak, TR-34469, Turkey.
{mustak.yalcin, yenicerir, ozoguz}@itu.edu.tr

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Chaotic time-delay systems are attractive candidates to generate chaotic dynamics because of their relatively simple system model. Circuit realization of the time-delay part is the main drawback of these systems. In order to overcome this drawback, a chaotic time-delay system which features a binary feedback function is presented. The use of binary feedback function results in a considerably simplified implementation of the time-delay unit based on using Flip-flop chain. Modeling the system thus obtained yields a chaotic sampled-data system. The existence of chaotic dynamics in the introduced sampled-data systems is numerically verified by calculating system Lyapunov exponents and applying a detailed bifurcation analysis. Chaotic attractor of the introduced sampled-data system is verified by the circuit realization of the system. In order to minimize the number of flip-flops in the chain while keeping the system in chaos, spectrum of Lyapunov exponent versus clock frequency of the flip-flops and a bifurcation parameter is computed. The circuit realization of the introduced sampled-data system includes relatively simple structure compared to other chaotic time-delay systems and overcome the complexity of the circuit implementation of the time-delay block.

Keywords: Sampled-data system, Circuit implementation, Time-delay system, Delay Differential Equations.

1. Introduction

There has been an increasing interest in Delay Differential Equation (DDE) to generate chaotic dynamics since Mackey-Glass equation [Mackey & Glass., 1977] describing physiological control systems was introduced. The first circuit realization to integrate Mackey-Glass equation was presented by Namajunas et al. [Namajunas et al., 1995] in 1995. Despite its simplicity, first-order nonlinear differential-delay equation of Mackey-Glass system can exhibits various dynamic behavior on a single state variable. Inspired by Mackey-Glass system, a new first-order nonlinear differential-delay equation with piecewise nonlinearity has been introduced by Uwe an der Heiden and M.C. Mackey [an der Heiden & Mackey, 1982] and its circuit realization was given by Losson et al. [Losson et al., 1993]. Another new DDE with piecewise linear characteristic, motivated by Cellular Neural Network with delay was introduced by Lu and He [Lu & He, 1996] and its chaotic behavior was experimentally verified [Lu et al., 1998]. A circuit realization of Mackey-Glass equation including piecewise linear delayed feedback experimentally verified that the model exhibits chaos [Tamasevicius et al., 2006]. This model has been generalized by introducing additional breakpoints.
in the piecewise linear function to obtain multi-scroll chaotic attractor by Wang and Yang [Wang & Yang, 2006]. Instead of using piecewise linear function, a cubic nonlinearity [Uçar, 2002] and a Chaotic DDEs with signum [Yalçın & Ozoguz, 2007] and hysteresis functions [Kılınç et al., 2010] together with their generalization were introduced to generate multi-scroll chaotic attractors.

Chaotic autonomous and non-autonomous systems require at least third-order and second-order continuous-time systems, respectively. However, a first-order continuous-time system with time-delay feedback can generate chaos. Although chaotic time-delay systems may be of smaller degree than the other types of systems, from the implementation point of view, the complexity of the time-delay block is the main drawback of these systems. Time-delay unit is commonly implemented using a cascade of filters, such as T-type LCL filters [Namajunas et al., 1995; Yalçın & Ozoguz, 2007] or Bessel-type filters [Lindberg et al., 2010] such that required delay is set to the group delay of the network. In [Namajunas et al., 1995] 30 LCL sub-circuits which is a total of 60 inductances and 30 capacitances has been used to implement the delay line. Mykolaitisa et al. [Mykolaitisa et al., 2003] have used a coaxial transmission line which is a specialized cable to implement the time-delay unit. Bucket brigade devices which is also known as analog delay line has been used by Losson et al. [Losson et al., 1993]. The analog delay line samples and delays the signal by storing it in the array of capacitor circuits. Furthermore, output of the delay circuit is fed through a Bessel-type filter. Delay part of the system can alternatively be implemented on a digital circuit [Pham et al., 2012]. To this end, analog signal in the input of the delay block is converted to a digital signal by an analog-to-digital converter (ADC), then this signal is delayed on a digital circuit. The delayed signal in the digital circuit is converted to an analog form and used in the system. From the circuit implementation point of view, implementation methods of the time-delay block of chaotic time-delay systems do not make chaotic time-delay systems an alternative for possible applications.

Time-delay block is considered as a memory device which stores the input and transfers it to the output after a delay time. When the digital circuit is considered, flip-flops (usually D-type) are used as memory device. Flip-flop is a digital circuit that has two stable states and its output takes the state of the input at the moment of a positive edge at the clock signal. The state of the input is sampled by the clock signal and held between two sequential clock edges. Thus, the state is delayed on a flip-flop chain. The chain length is proportional to the desired delay. It should be noted that, flip-flop chain is suitable for the circuit-integration.

This paper seeks to explore the possibility of using flip-flops in the implementation of chaotic time-delay systems. For this purpose, we have presented a chaotic time-delay system with a binary feedback function which is the function of delayed state variable. The nonlinear feedback function is a binary output function therefore a chain of flip-flops might be used to delay the output of the nonlinear feedback function. The use of a flip-flop (D-type) chain to delay the binary output of the nonlinear feedback part of the introduced system yields a new system which is a sampled-data feedback system [Astrom & Wittenmark, 1984]. Although sampled-data system is well-known in digital control systems and some related techniques have been recently used for synchronization of chaotic systems [Lu & Hill, 2008; Chen et al., 2012; Barajas-Ramirez et al., 2003], to our knowledge, a chaotic sampled-data system has not been introduced yet in the literature.

The paper is organized as follows. In Section II, the proposed time-delay chaotic system with a binary feedback function is introduced and the dynamical behavior of the system is analysed. In Section III, we present a chaotic time-delay sampled-data system which is obtained after the delay block of the proposed time-delay chaotic system is implemented using a flip-flop chain. The effect of chain’s clock period to the system dynamics is studied in Section IV. Then the circuit implementation is discussed and the obtained experimental results are reported in Section V. Finally, Section VI concludes the work.

2. Time-Delay System with Binary Feedback

We consider the following delay differential equation

\[ \dot{x}(t) = -x(t) + \alpha f(x(t - \tau)) \]  

(1)
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Figure 1. The nonlinear function $f(x)$ and its approximate function $g(x)$ with $\gamma = 20$ given in Eq. (3).

Figure 2. Chaotic attractor of the system (1).

where $\alpha \in R$ is the bifurcation parameter and the nonlinearity $f(\cdot)$ (Figure 1) is given by

$$f(x) = \begin{cases} -1 & |x| \leq 1 \\ 1 & |x| > 1 \end{cases}. \quad (2)$$

This equation with small difference has been used to model the processes in various areas of biology and chaotic dynamics of the system has been already presented by Uwe an der Heiden and M.C. Mackey [an der Heiden & Mackey, 1982]. Figure 2 shows the chaotic attractor of the presented system (1) in $x(t) - x(t-\tau)$ plane for $\alpha = 2$ and $\tau = 8$.

The nonlinearity of the system is a discontinuous function and it can be approximated by $\tanh(\cdot)$ functions such as

$$g(x) = \tanh(\gamma(-x-1)) + \tanh(\gamma(x-1)) + 1. \quad (3)$$

Figure 1 shows the $f(\cdot)$ function and its approximation $g(\cdot)$. The introduced system (1) with this smooth approximate function (3) evolves in the same type of chaotic attractor.

Here, $S = \{x(t) : x(t) = x(t-\tau)\}$ is defined as a Poincaré section for computing the bifurcation diagram. The bifurcation diagram of the system (1) versus parameter $\alpha$ is shown in Figure 3(a). For a quantitative measure of the system dynamics, Lyapunov exponent [Farmer, 1982] versus the parameter $\alpha$ is displayed on the same figure (Figure 3(a)) with the bifurcation diagram. These results show a good agreement between
the values of the Lyapunov exponent and the observed bifurcation diagram. The presence of a positive Lyapunov exponent along with the observed strange attractor and bifurcation diagram indicate chaotic behavior in the system. We conclude that the attractor of the introduced system (1) which is illustrated in Figure 2 is a chaotic attractor.

In order to understand the sensitivity of the dynamical behavior of the system (1) versus the delay \( \tau \), the variation of the Lyapunov exponent versus the delay is displayed on the Figure 3 (b) with the
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3. Chaotic Time-delay Sampled-data System

Analog time-delay is usually implemented using an artificial delay line [Namajunas et al., 1995; Losson et al., 1993; Mykolaitis et al., 2003; Yalcin & Ozoguz, 2007; Buscarino et al., 2011]. This implementation does not permit to minimize both the number of physical components and the number of idealized elements required to accurately model the circuit. The delay part of a time-delay chaotic system has been already implemented on computer using analog-to-digital converter (ADC) and digital-to-analog converter (DAC) [Pham et al., 2012]. Furthermore, it has been shown that the system exhibits chaotic behavior in that implementation. In [Pham et al., 2012], an ADC is used to convert the state variable to digital value and it is delayed on logic gates. Then a DAC is used to convert the delayed state to analog signal. Here, we introduce a time-delay sampled-data system which is remodeled from the introduced system (1) where the delay part of the system is implemented with a digital circuit.

Block diagram of the system (1) is shown in Figure 4(a). The nonlinearity $f(x)$ of the system (1) is reformulated:

$$f(x) = f_c(h(x)) = \begin{cases} 1 & h(x) = 1 \\ -1 & h(x) = 0 \end{cases}$$

where $h(x(t))$ is a binary output function such that the output of function is 0 while $|x(t)| \leq 1$, else it is 1. This new formulation of the nonlinearity allows to implement $h(x)$ with two heaviside functions ($u(\cdot)$) such as

$$h(x) = u(x(t) - 1) + u(-x(t) - 1).$$

The nonlinearity of the system is a composition of the functions $h(\cdot)$ and $f_c(\cdot)$. Here, the function $h(\cdot)$ is the binary output function and nonlinear characteristic of the function $f(\cdot)$ can be realized by this function. The function $f_c(\cdot)$ which is given in Eq. (4) converts 0 to $-1$ and $f_c(1)$ is equal to 1.

Furthermore, the function $f(\cdot)$ is a time invariant function therefore one can write

$$f(T_{\text{Delay}}[x(t)]) = T_{\text{Delay}}[f(x(t))]$$

where $T_{\text{Delay}}[x(t)] = x(t - \tau)$. The above equation implies that the function of the delayed signal is equal to the delayed function of the signal. Therefore, the delay block $T_{\text{Delay}}[\cdot]$ can be placed after the nonlinear block which implements the function $f(\cdot)$. Hence, the new block diagram representation of the system is shown in Figure 4(b). In this work, the delay block is placed just before the $f_c(\cdot)$.

Here, we aim to use a digital circuitry to implement delay block $T_{\text{Delay}}[\cdot]$. In order to use a digital circuitry, the output signal of the $h(\cdot)$ function block might be converted into digital form by an ADC. Note that since the function $h(\cdot)$ is a binary output function, quantization and encoding operations performed
The mathematical model of the introduced chaotic time-delay sampled-data system is
\[
\dot{x}(t) = -x(t) + \alpha f(x(t_k - \tau)), \quad t_k \leq t < t_k + T_s
\]
where $T_s$ is the sampling period and $t_k$ is the $k^{th}$ sampling time. The system (7) has a similar strange attractor in $x(t) - x(t - \tau)$ plane for $\alpha = 2$, $\tau = 8$ and $T_s = 0.1$ as shown in Figure 6.

This attractor has been already used to realize a true random number generator by Yeniceri and Yalcin [Yeniceri & Yalcin, 2013]. In order to examine the dynamic of the system (7), $S = \{ x : x(t) = x(t - \tau) \}$ is again chosen as Poincaré section for computing the bifurcation diagram. Figure 7 shows the experimentally obtained bifurcation diagram versus parameter $\alpha$ for $T_s = 0.1$. Lyapunov exponent versus the parameter $\alpha$ is displayed on the same figure (Figure 7) with the bifurcation diagram. Figure 7 experimentally proves that the obtained attractor in Figure 6 is a chaotic attractor for the given parameter set. The Figures 3

\[\text{Fig. 5. Block diagram of the chaotic time-delay sampled-data system (7).}\]

\[\text{Fig. 6. Chaotic dynamics of the system (7) for } T_s = 0.1 \text{ in } x(t)-x(t-\tau) \text{ space. The characteristic shape of strange attractors of the system (1) (see in Figure 2) and the chaotic time-delay sampled-data system (7) for } T_s = 0.1 \text{ are similar.}\]
and 7 show that the systems (1) and (7) have similar dynamical behavior. Specially, the system dynamics are almost identical for the small sampling period which will be explored in the next section.

4. Study on The Sampling Period

Dynamics of sampled-data system depend on sampling period $T_s$. In the presented chaotic time-delay sampled-data system (7), the signal is binary in the input of the zero-order hold block (see Figure 5), an error occurs when the input signal changes the state within the sampling interval. Otherwise the output of the delay line will be equal to the output of the ideal delay block ($h(x(t-\tau)) = h(x(t_k-\tau))$). The gray region in Figure 8 represents this situation. The input signal might change any time between the two samples, therefore $h(x(t-\tau)) = h(x(t_k-\tau))$ until a state change (for example, the output of the delay line will be correct $h(x(t-\tau))$ value between time $t_2$ and $t_b$ (see Figure 8)). However, the output of the delay line will not be $h(x(t-\tau))$ between the time when the state change occurs and the next sampling time ($t_b$ and $t_3$ in Figure 8, respectively). In fact, the output of the delay line will be $h(x(t_3-\tau))$ instead of $h(x(t-\tau))$ where $t_b \leq t \leq t_3$. This error appears since the $x(t)$ is a chaotic signal and/or $h(x(t))$ and sampling signal are not synchronized. The amount of error depends on the sampling period $T_s$.

Choosing the $S = \{x : x(t-\tau) = -1\}$ as a Poincaré section, the corresponding bifurcation diagram is depicted on Figure 9 to illustrate the behavior of the system for variation of the sampling period. The system keeps its chaotic regime while $T_s \leq 0.26$. In order to have similar dynamical behavior with the system (1), $T_s$ should be chosen small. However, the system (7) exhibits chaotic dynamics depending on the bifurcation parameter $\alpha$ also. Figure 10 shows how the bifurcation parameter $\alpha$ effects the behavior of the system. In Figure 10, spectrums of Lyapunov exponent for $T_s = 0.02$, $T_s = 0.25$, $T_s = 0.4$ and $T_s = 0.6$ versus $\alpha$ are given in the same figure.

Lyapunov spectrums of the chaotic time-delay system (1) and the chaotic time-delay sampled-data system (7) for $T_s = 0.02$ which are given in Figure 3(a) and Figure 10 respectively, indicate that these two systems show the same dynamical behavior. The system (7) might be in a chaotic region for a large $T_s$ depending on $\alpha$ parameter (see Figure 10). However, we do not have a wide range of parameter values which keeps the system (7) in chaos. In order to better understand the dynamics of the system (7) and to have flexibility for the circuit which will be designed in the next section, Lyapunov-exponent spectrum is
Fig. 8. The output of the ideal delay line \( h(x(t - \tau)) \) and the output of the sample-and-hold delay line \( h(x(t_k - \tau)) \) where \( k = 1, 2, 3 \). \( h(x(t_k - \tau)) \) is obtained after the sampling of \( h(x(t - \tau)) \). These two signal will not be the same between \( t_b \) (when a state change occurs between two samples) and \( t_3 \) (the next sampling time).

Fig. 9. Bifurcation diagram and the spectrum of Lyapunov exponent of the introduced system (7) with \( \alpha = 2 \) and \( \tau = 8 \) versus \( T_s \).

calculated for both \( T_s \) and \( \alpha \), in the range of \([0.02, 1]\) and \([0.9, 3]\), respectively. The obtained Lyapunov exponents are displayed on \((T_s - \alpha)\)-plane (Figure 11) by mapping the Lyapunov exponent which is larger than 0 to a black dot. Gray region indicates that the system produces a periodic motion.

5. Circuit Realization and Experimental Results

As mentioned in Section 3, we aim to implement the delay block with a digital circuit. D-type flip-flop is a basic digital circuit element and it is basically a zero-order hold (ZOH) block which is required in our system. D-type flip-flop samples the binary state at its input at the rising edge of the clock signal or sampling signal and delays it one cycle. Note that, the use of D-type flip-flops considerably simplifies the chain because of the simple input-output relation of these flip-flops. The signal at the delay line output is \( h(x(t_k - \tau)) \) which is given by

\[
h(x(t_k - \tau)) = T_{\text{Delay}}[h(x(t_k))]
\]

where \( t_k \) is a sampling time.
Fig. 10. Lyapunov exponent spectrums of the system (7) for \( \tau = 8 \) versus \( \alpha \) are calculated for \( T_s = 0.02, T_s = 0.25, T_s = 0.4 \) and \( T_s = 0.6 \).

Fig. 11. Dynamical behavior of the time-delay sampled-data system (7) in \( (T_s - \alpha) \)-plane. Black region indicates that the system is in chaos. Gray region indicates that the system produces a periodic motion.

It should be noted that the output of the D-type flip-flop is constant between the sampling instants and the output is a continuous-time signal. In the chain, the input signal is sampled by the clock signal and this input occurs in the output of the chain after \( N_{FF} \) (\( N_{FF} \) is the number of flip-flops) clocks. Hence, the delay obtained by the chain is given with

\[
\tau = N_{FF} T_s
\]

where \( T_s \) is the clock period of the flip-flops.

In order to verify the feasibility of the proposed chaotic system, a practical circuit that realizes the
model equation in (7) is designed and built using off-the-shelf components. The diagram of the designed circuit is given in Figure 12 which is implemented using one capacitor, five resistors, three voltage comparators and two CFOAs (current feedback op amps, special op amps offering high-slew rate performance (AD844) [Toumazou et al., 1990]) operating in open-loop configuration.

The subcircuit depicted within dashed lines in Figure 12 built around two voltage comparators, three resistors denoted by $R_1$, $R_2$ and $R_3$, and the CFOA realizes the required nonlinear function $1 - h(x)$, which is the binary inversion of $h(x)$. The nonlinear voltage transfer of this subcircuit is given by:

$$v_h = -V_{CC}R_3\left(\frac{1}{R_1}u(v_C - V_b) - \frac{1}{R_2}u(v_C + V_b)\right).$$ (10)

For $R_1 = R_2$, the nonlinear voltage transfer becomes

$$v_h = \frac{V_{CC}R_3}{R_1}\left[1 - h\left(\frac{v_C}{V_b}\right)\right].$$ (11)

It should be noted that $v_h(t)$ corresponds to $[1 - h(x(t))]$, where $h(x)$ is defined in Eq. (5). Output levels of the comparator subcircuit are $\frac{R_3}{R_1}V_{CC}$ and 0. Hence, it has two stable states and it would be possible to implement $T_{Delay}[]$ block with a digital circuit after the output of the function $[1 - h(x)]$, which can be represented by the binary digits.

The subcircuit shown within the gray box realizes the delay function with binary output, $T_{Delay}[]$, and is composed of an FPGA based structure. The delay line is implemented on a low-cost 100K-gate FPGA (XC3S100E-4TQ144) and clocked by 100 MHz frequency signal generated by the oscillator on the board. The length of flip-flop chain ($N_{FF}$) is set to 20,000 in order to obtain needed delay time, $\hat{\tau} = 200\mu s$. The output of the flip-flop chain is given by:

$$v_d(\hat{t}) = v_h(\hat{t}_k - \hat{\tau}),$$ (12)

where $\hat{t}$ is the time, $\hat{t}_k$ is the sampling time and $\hat{\tau}$ is the amount of delay in seconds.
A voltage comparator \((V_r = 0.5V)\) which implements the block \(f_c(\cdot)\) is driven by the output of the delay line which yields
\[
v_f(\hat{t}) = V_{\text{CC}} \left[ 2 \cdot u \left( \frac{V_{\text{CC}} R_3}{R_1} \left( 1 - h \left( \frac{v_C(\hat{t}_k - \hat{\tau})}{V_b} \right) \right) - V_r \right) - 1 \right]. \quad (13)
\]

Briefly, Eq. (13) can be written by
\[
v_f(\hat{t}) = -V_{\text{CC}} f \left( \frac{v_C(\hat{t}_k - \hat{\tau})}{V_b} \right). \quad (14)
\]

The output of this block \((v_f)\) is connected to CFOA2 which is used for implementation of a voltage controlled current source. Routine analysis of the circuit (Figure 12) yields to the following equation:
\[
\dot{v}_C(\hat{t}) = -\frac{v_C(\hat{t})}{RC} + \frac{V_{\text{CC}}}{R_4 C} f \left( \frac{v_C(\hat{t}_k - N_{\text{FF}} \hat{T}_s)}{V_b} \right), \quad (15)
\]

where \(\hat{T}_s\) is the flip-flop clock frequency in seconds with \(\hat{t}_k \leq \hat{t} < \hat{t}_k + \hat{T}_s\).

By defining the following normalized variables \(x \equiv v_C/V_b, \tau \equiv N_{\text{FF}} \hat{T}_s/RC, \alpha = V_{\text{CC}} R_4/\hat{R}_4\), normalizing time using \(t = \hat{t}/RC\), and choosing \(V_b = 0.75V\) it can readily be shown that Eq. (15) is equivalent to the model equation (7).

The circuit in Figure 12 is built using the following passive component values: \(C = 5nF, R_1 = R_2 = 50k\Omega, R_3 = 33k\Omega\) and \(V_{\text{CC}}\) is set to 5V. Hence, the voltage of delay line input is in the range of [0,3.3]V. The value of \(R\) and \(\hat{R}_4\) are made adjustable to set desired \(RC\) and \(\alpha\) values.

Agilent’s DSO6104A oscilloscope, which has 1 GHz bandwidth through its 4 Gsps rate, is utilized to analyse the system. Time waveform of the capacitor voltage, \(v_C(t)\) corresponding to the variable \(x\) in Eq. (1) is captured by this digital oscilloscope. But, the captured signal is downsampled to 1 Msps by the oscilloscope in order to reduce the data size of the waveform. The value of adjustable resistor \(R\) is set to 5K\(\Omega\) with \(C = 5nF\) and \(\hat{\tau} = 200\mu s\) to make \(\tau = 8\). A 200 ms of sampled signal record, which is 200K samples long, is taken to computer. In this system, only \(v_C(\hat{t})\) can be measured, because the binary signal \(b(v_C(\hat{t}_k))\) is delayed instead of \(v_C(\hat{t})\). Therefore, \(v_C(\hat{t} - \hat{\tau})\) is obtained from the signal recorded and transferred to the computer. Phase portrait of a 40ms interval, which is plotted using the recorded data, is shown in Figure 13.

Based on the spectrum of the Lyapunov exponents on the \((T_s - \alpha)\)-plane (Figure 11), it is possible to decrease the number of flip-flops on the delay line. The amount of the delay is the product of \(N_{\text{FF}}\) and \(T_s\) as given in Eq. (9). With a constant proper \(\alpha\) value, \(T_s\) can be increased, which provides decrease in \(N_{\text{FF}}\), and can be still in the chaotic regime. The \(\alpha\) values greater than 2 yield a chaotic behavior band for \(T_s\) values smaller than approximately 0.2. As an example, for \(\alpha = 2.5\), the phase portraits for different \(T_s\) values are depicted in Figure 14. The phase portraits on the left column of the figure are drawn with the captured data from the circuit realization. The phase portraits on the right column belong to the computer simulation results. \(T_s = 0.001\) for Figures 14(a) and 14(b), \(T_s = 0.020\) for Figures 14(c) and 14(d), \(T_s = 0.250\) for Figures 14(e) and 14(f) while \(\tau = 8\) for all experiments. So, the numbers of utilized flip-flops are 8000, 400 and 32, respectively. Apparently, both the simulation and the circuit realization still exhibit the chaotic attractor when \(N_{\text{FF}}\) is decreased from 8000 to 32. Moreover, experiments with smaller number of flip-flops than 32 validate Figure 11 with non-chaotic behavior. Although it is easy to implement chains longer than 8000 flip-flops using current FPGAs, requiring few number of flip-flops strengthens the simplicity of the presented chaotic system.

6. Conclusion

In this paper, a chaotic delay differential equation has been introduced which includes binary time-delay feedback function. This function allows to use simplified digital circuitry to implement time-delay block. Time-delay sampled-data system has been obtained when this block is implemented by a digital circuit. To the best of our knowledge, this is the first chaotic sampled-data system which is reported with its
mathematical model and its circuit realization. Chaotic dynamics of the introduced time-delay and time-delay sampled-data systems have been verified by numerical analysis. The detailed numerical analysis of the introduced systems shows that the systems are in chaos in a wide range of the system parameters. When the implementation of the systems is considered, realization of the obtained chaotic time-delay sampled-data system becomes much more practical than the chaotic time-delay systems. Furthermore, the circuit realization has been significantly simplified using the nonlinear analysis of the time-delay sampled-data system.

References


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Fig. 14. $v_C(t_k - \tau) - v_C(t)$ phase portraits of circuit realization for (a) $T_s = 0.001$, (c) $T_s = 0.020$, (e) $T_s = 0.250$ and of simulations for (b) $T_s = 0.001$, (d) $T_s = 0.020$, (f) $T_s = 0.250$. For all experiments $\alpha = 2.5$ and $\tau = 8$. This results demonstrate that the chaotic behavior of the system can be obtained with a small number of flip-flops down to 32 in conformity with Lyapunov exponent spectrum in Figure 11.