Design of 1.8V 1GHz 0.18μm CMOS LNA for GPS

Huazhu Liu
School of Electronics and Information Engineering
South China University of Technology
Guangzhou 510641, China
Department of Electronic
Dongguan University of Technology
Dongguan 523808, China

Qianhua He
School of Electronics and Information Engineering
South China University of Technology
Guangzhou 510641, China

Abstract—the low noise amplifier is the key part for front-end device of the receiver in the GPS. A 1.8V 0.18μm CMOS LNA for GPS applications has been designed. Two kinds of low noise amplifier (LNA) for single-end cascade structure and differential cascade structure respectively are presented in this paper. Cadence software is used to optimize the two circuits. It provides a series of good results in Noise figure, Linearity and Power dissipation. With a 1.8 V supply, the two LNAs achieve power gains of 19.5dB and 23dB, Noise figures of 1.9dB and 1.95dB. Besides, the input P1dB is -19.05dBm and -14.65dBm.

Keywords-GPS; CMOS; Low noise amplifier

I. INTRODUCTION

As the increasing of the wireless communication market, the design of low noise amplifier becomes important part which characterizes the whole receiver performance [1]. In radio-frequency front-end devices, the RF signals received from the antenna are amplified by low-noise amplifier (LNA) and then down-converted by the mixers to be low-frequency signals. As the receiver is required to detect a low power signal, an LNA with extremely low noise figure is required. In addition, the LNA must exhibit a large gain to suppress noise from the subsequent stages. Thus a low noise amplifier has been improved and analyzed widely. This LNA meets these requirements [2].

In this paper, we present two fully integrated 0.18μm CMOS 1 GHz LNAs. One is single-ended, another is differential. This design is based on a cascade configuration including inductive feedback to the common source amplifier for simultaneous noise and input impedance matching, and capacitive feedback to the common-gate transistor to simultaneously optimize for linearity, gain and stability performance [3]. Design detailed consideration and simulation results are presented in section II and III respectively.

II. SINGLE-ENDED LNA DESIGN

A single-ended 1GHz LNA is shown in Fig1. This amplifier has the commonly used cascaded architecture. The cascade structure is known as the best architecture that can achieve both power gain and low noise figure (NF) requirements [4-5]. The cascade configuration allows both FETs to use the same current and eliminating the need for coupling capacitors.

The input impedance is usually matched to 50Ω due to the sensitivity of the front-end filter to the input impedance of the low noise amplifier.

The input impedance of the cascade LNA can be given by

\[ Z_{in} = j\omega(L_1 + L_2) + \frac{1}{j\omega C_{gs}} + \left( \frac{g_m}{C_{gs}} \right) L_2 \]

where \( C_{gs} \) and \( g_m \) are respectively the gate-source capacitance and the Tran conductance of M2 transistor.

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Figure 1. The single-ended CMOS LNA

The matching condition of the input impedance is often difficult to achieve due to the process variation and the lack of good active and passive device models [5]. Because the required 50 Ω input matching the source inductor is very small, a large gate inductor is required to tune out the gate-source capacitance of the M2 transistor. This is a first order

Sponsored by Nature Science Foundation of China; Grant Number: 60572141.
approximation and when $C_{gd}$ is included in the FET equivalent circuit and the miller effect is taken into account, there required inductance increases. The degenerated Tran conductance should also remain high enough to guarantee the required transducer gain. The common-gate transistor M3 acts as a current buffer that provides impedance transformation and higher isolation between output and input of the low noise amplifier [6-8].

At the central frequency 1 GHz, the imaginary term of $Z_{in}$ will be zero, which gives

$$\omega (L_1 + L_2) - \frac{1}{\omega C_{gs}} = 0$$ (2)

From the above equation, $L_1$ is solved. All of the inductors are on-chip inductors, implemented on a high Q thick metal layer. The capacitors are metal-oxide-metal capacitors.

The single-ended LNA was simulated with the cadence SpectreRF simulator. Figures 2 to 5 show simulation results of the LNA. With a supply of 1.8V, at 1.0GHz, $S = -15$dB, $S = -12$dB, $S = -23$dB, the noise figure is 1.9dB, the input P1dB is -19.05dBm, the power dissipation is 4.6mW. If supply voltage goes down, the power dissipation will drop, with a smaller gain and bigger noise figure.

The layout of this LNA circuit is shown in Fig 6. It is somewhat big with 3 on-chip inductors, which occupy the most die area.

III. DIFFERENTIAL LNA DESIGN

The proposed differential cascade LNA is shown in Fig 7. M2 and M4 and associated inductors form the input stage, which also provides needed matching input impedance of 50$\Omega$. The use of inductive source degeneration through L2 and L4 has the benefit of simultaneous input and noise matching. At the input, the capacitor C1 and C4 is a DC blocking capacitor.
The cascade amplifier is inductively loaded with the inductor L3 and L5 to facilitate narrow-band operation at 1.0GHz while minimizing power dissipation. C5 and C6 provide AC coupling between the LNA and the following envelope detection stage. The gain of the amplifier is adjusted by controlling the biasing voltage of M5 and M6.

At the output, the inductor L3 and L5, the capacitors C5 and C6 compose an output LC resonance tank circuit [7-13]. Capacitors C5 and C6 perform capacitive transformation of the impedance level at the drain node to a desired lower output impedance level which is suited for reducing signal amplification. The DC current through the cascade stage is determined by the gate voltage of M2 and M4.

The LNA was simulated with the cadence SpectreRF simulator. Figures 8 to 11 show simulation results of the LNA. We find that the LNA achieves a noise figure of 1.95 dB with $S_{11} = -17\text{ dB}$ and $S_{22} = -14\text{dB}$. We also find that LNA performs a small signal gain of 19.5 dB with a -3dB gain bandwidth of 320MHz. Fig11 illustrated the 1dB compression is simulated to be -14.65dBm. Fig12 shows the layout of the LNA. It uses a compact of the LNA; the strategy is to make the layout symmetrical as far as possible. To reduce the gate and substrate resistance of the LNA input transistors, multiple fingers with gate contacts at both sides have been used. The LNA is biased in its nominal 5.45mW drawing a nominal bias current of 3.03 mA from a 1.8V power supply. Table 1 summarizes the performance of the two comparison LNAs.
IV. CONCLUSION

Two LNAs have been designed in a 0.18μm CMOS process. Both of them are fully integrated, without off-chip components. The single-ended LNA achieves a gain of 23dB, a noise figure of 1.9dB, with a supply of 1.8V, at 1.0GHz, S11 = -15dB, S22 = -12dB. The differential LNA achieves a gain of 19.5 dB, a noise figure of 1.95dB, with a supply of 1.8V, at 1.0GHz, S11 = -17dB, S22 = -14dB.

REFERENCES