PAPER

Analysis and Design of Sub-Threshold R-MOSFET Tunable Resistor

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SUMMARY The sub-threshold R-MOSFET resistor structure which enables tuning range extension below the threshold voltage in the MOSFET with moderate to weak inversion operation is analyzed in detail. The principal operation of the sub-threshold resistor is briefly described. The analysis of its characteristic based on approximations of a general MOS equation valid for all regions is given along with discussion on design implication and consideration. Experiments and simulations are provided to validate the theoretical analysis and design, and to verify the feasibility at a supply voltage as low as 0.5 V using a low-threshold devices in a 1.8-V 0.18 μm CMOS process.

key words: *MOSFET resistor, R-MOSFET resistor, sub-threshold techniques, low voltage techniques*

1. Introduction

With the continued reduction of supply voltages due to aggressive downsizing of transistors in modern CMOS processes, the design of analog circuits that co-integrate with digital circuits on the same chip with sufficient performance promises to be increasingly challenging. For analog filtering applications, continuous-time (CT) MOSFET-C and linearity enhanced R-MOSFET-C techniques that employ no switches as well as no anti-aliasing and smoothing filters have been demonstrated as attractive alternatives to sampled-data switched-capacitor (SC) filters at low voltages [1]–[4]. One major issue however for the low-voltage CT filters is the limited range of the gate voltage available for tuning the corner frequency through the MOSFET resistance so as to cope with inevitable process and temperature variations. Although this may be circumvented either by using native transistors, low threshold transistors or thick oxide transistors, a control voltage larger than the supply is often necessary, thereby necessitating a clock boosting circuitry which invariably poses reliability concerns on the devices. Another means is to employ the variable MOS capacitors [1], but a switched array of parallel *linear* capacitors for coarse tuning must be included to achieve a good linearity and adequate overall tuning range.

Recently, an enhanced structure that can extend the usability of the R-MOSFET approach by enabling MOSFET operation in moderate to weak (or sub-threshold) inversion, without significant impairment on linearity, was introduced [5]. The so-called sub-threshold R-MOSFET structure essentially relies upon a *cancellation* of the nonlinearity which can be *strongly* nonlinear such as that exhibited by a saturated sub-threshold MOSFET. This is in stark contrast to the existing R-MOSFET configurations that rely upon series and/or parallel linear resistor(s) to *suppress* the non-linearity and thus become ineffective at sub-threshold MOSFET operation. For the sub-threshold resistor to exhibit optimum linearity and tuning capability, it requires an appropriate design and this is the subject of this paper. In Sect. 2, the principal operation and detailed analysis, which leads to a perfect linearization in the sub-threshold resistor, are outlined. Also discussed in this section is a possible design guideline for good linearity performance over the required tuning range. Section 3 provides extensive analysis and design verification through experiments and simulations. This is followed by conclusions in Sect. 4.

2. Sub-Threshold R-MOSFET Analysis

2.1 Principal Operation

Figure 1 shows the sub-threshold R-MOSFET resistor where it consists of the linear resistors $R_1 - R_2$ and the MOS transistors $M_1 - M_2$. When compared to the simple series-parallel R-MOSFET resistor which comprises R_1, R_2 and M_1, the sub-threshold resistor of Fig. 1 employs the additional transistor pair, M_2. From another point of view, when compared to the dump configuration of the R-MOSFET resistor in [3] which comprises R_2, M_1 and M_2, the

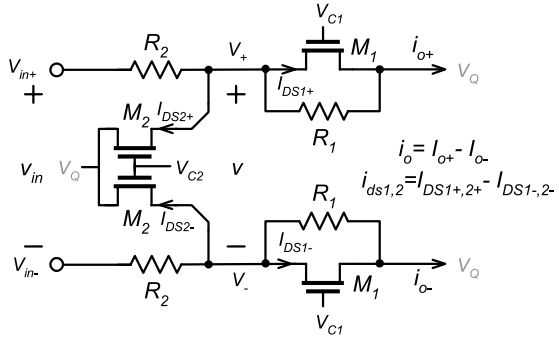

Fig. 1 Sub-threshold R-MOSFET tunable resistor structure.

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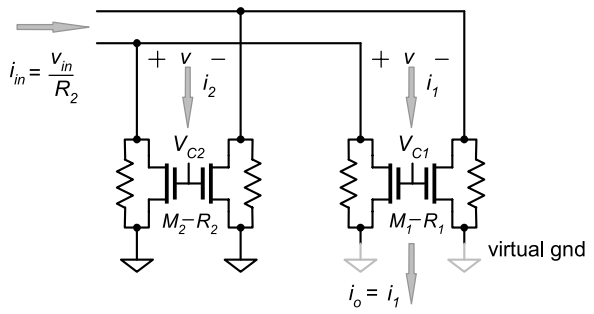

Fig. 2 Norton's equivalent circuit of sub-threshold R-MOSFET resistor.

sub-threshold resistor employs the additional resistor pair, R_1. Thus, the major differences lie in the fact that the sub-threshold resistor makes simultaneous use of both R_1 and M_2 and this offers linearity improvement, especially when the MOS transistors operate in the sub-threshold region.

An insight into its underlying principle can be gained by transforming the differential input voltage v_{in} and the series R_2 into its Norton's equivalent. The resultant circuit, after rearrangement for the sake of description, is as shown in Fig. 2, with all the voltage/current variables indicated being differential. The transformed circuit is essentially a parallel of two *nonlinear* resistance branches, each comprising a pair of linear resistors and MOSFETs. In operation, the equivalent input current $i_{in} = v_{in}/R_2$ is divided into two paths — one through the parallel combination of R_1 and M_1 to produce the output current $i_o = i_1$ with a nonlinear current-voltage relation $i_1 = G_1(v)$; the other through R_2 and M_2 to produce the current i_2 with a nonlinear relation, $i_2 = G_2(v)$, where v is the common differential voltage across the two branches. Note that the linear terms of $G_1(v)$ and $G_2(v)$ are mainly contributed by the linear resistors, while the nonlinear terms are mainly contributed by the MOSFETs. Thus, to achieve a perfectly linear relationship between $i_o = i_1$ and i_{in}, hence between i_o and v_{in}, it demands that the current division be linear. This can be accomplished when the two nonlinear branches are *linearly dependent*, i.e., $G_1(v) = \delta \cdot G_2(v)$ where δ is a constant, *regardless* of the nonlinear characteristic. It should be noted that such a linearization condition emphasizes the critical role of including both R_1 and M_2 in the sub-threshold resistor structure.

One important consideration now is the fact that, under a low supply voltage and a large signal swing, the MOSFET operation in the sub-threshold resistor can span not only from strong to moderate and weak inversion, but also from non-saturation to saturation. Thus, it is of prime importance to conduct detailed analysis that could lead to design guidelines so as to ensure good linearity over the resistance tuning range.

2.2 Sub-Threshold R-MOSFET Analysis

Due to such a wide coverage of the MOSFET's operation, it is necessary to employ a general current-voltage MOS equation valid for all regions. This can be given by [6]

$$I_{DS} = 2m\varphi_t^2\mu C_{ox}\frac{W}{L}\left(\ln^2\left[1+e^{\frac{V_{GB}-V_{T0}-mV_{SB}}{2m\varphi_t}}\right] - \ln^2\left[1+e^{\frac{V_{GB}-V_{T0}-mV_{DB}}{2m\varphi_t}}\right]\right) \quad (1a)$$

with

$$m = \left(1-\gamma/2\sqrt{V_{GB}-V_{T0}+\left(\gamma/2+\sqrt{\varphi_0}\right)^2}\right)^{-1} \quad (1b)$$

where $\phi_t = kT/q$ is the thermal voltage, μ is the carrier effective mobility in the channel, C_{ox} is the gate-oxide per unit area, W and L are the channel width and length, V_{T0} is the threshold voltage at $V_{SB} = 0$, γ is the body effect coefficient and ϕ_0 is a characteristic potential [6]. It is noted that the short-channel effects and the dependence of the mobility on the transversal field are not included in (1).

Consider the sub-threshold R-MOSFET resistor in Fig. 1. It is assumed that the input and output quiescent voltages are set at V_Q, the body voltage of all the MOSFETs at $V_B = 0$, the gate bias at V_{C1} for M_1, and at V_{C2} for M_2. For a balanced differential input, $\pm v_{in}/2$, Eq. (2) at the bottom of the page is obtained by applying KCL at the intermediate nodes with the voltages V_+ and V_- in Fig. 1, and taking their difference. In (2), $I_{Z1,2} = 2m\phi_t^2\mu C_{ox}W_{1,2}/L_{1,2}$, and i_{ds1} and i_{ds2} are the differential drain/source currents of the MOSFET pairs, M_1 and M_2, respectively. $i_o = i_{o+} - i_{o-}$ denotes the differential output current. To obtain manageable results that enable insight into the circuit operation, and also help offer a design implication, the following approximations are applied to (2). Due to the presence of the *linear* resistors R_1 and R_2, it is possible to assume that V_+ and V_- are also balanced similar to the input v_{in}, i.e., $V_+ = V_Q + v/2$ and $V_- = V_Q - v/2$, and hence the definition of the differential voltage v is $v = V_+ - V_-$. To help simplify the analysis, each variable in (2) is normalized by the following definitions: $x = v_{in}/2m\phi_t$, $z = v/2m\phi_t$, $a_{1,2} = (V_{C1,2} - V_{T0} - mV_Q)/2m\phi_t$, and $g_{1,2} = 2m\phi_t/I_{Z1}R_{1,2}$. Thus, it follows that (2) can be rewritten as

$$g_2(x-z) = \underbrace{\left(\ln^2\left[1+e^{a_1+mz/2}\right]-\ln^2\left[1+e^{a_1-mz/2}\right]\right)+g_1 z}_{y} + r\left(\ln^2\left[1+e^{a_2+mz/2}\right]-\ln^2\left[1+e^{a_2-mz/2}\right]\right) \quad (3)$$

with $r = I_{Z2}/I_{Z1}$ and $y = i_o/I_{Z1}$. With the use of Taylor series representation similar to [7] (for analysis of non-saturated strong inversion MOSFET resistors), the normalized differential current-voltage relation of the MOSFET pairs in (3) which involve a difference of square logarithmic operation can be expressed in a polynomial form with no even-order terms due to the balanced structure. Such an expansion with respect to z yields

$$\ln^2\left[1+e^{a+mz/2}\right]-\ln^2\left[1+e^{a-mz/2}\right] \approx c_1^n z + c_3^n z^3 + c_5^n z^5 \quad (4a)$$

with

$$\frac{v_{in}-(V_+-V_-)}{R_2}=\underbrace{\overbrace{I_{Z1}\left(\ln^2\left[1+e^{\frac{V_{C1}-V_{T0}-mV_-}{2m\varphi_t}}\right]-\ln^2\left[1+e^{\frac{V_{C1}-V_{T0}-mV_+}{2m\varphi_t}}\right]\right)}^{i_{ds1}}+\frac{(V_+-V_-)}{R_1}}_{i_o}+\overbrace{I_{Z2}\left(\ln^2\left[1+e^{\frac{V_{C2}-V_{T0}-mV_-}{2m\varphi_t}}\right]-\ln^2\left[1+e^{\frac{V_{C2}-V_{T0}-mV_+}{2m\varphi_t}}\right]\right)}^{i_{ds2}} \quad (2)$$

$$c_1^n=\frac{2me^a}{1+e^a}\ln(1+e^a) \quad (4b)$$

$$c_3^n=\frac{m^3e^a}{12(1-e^a)^3}\left(3e^a+\ln(1+e^a)-e^a\ln(1+e^a)\right) \quad (4c)$$

$$c_5^n=\frac{m^5e^{2a}}{960(1+e^a)^5}\cdot\left[5\left(3-e^a\left(6-e^a\right)\right)+2\left(1-e^a\right)\left(\cosh(a)-5\right)\ln(1+e^a)\right] \quad (4d)$$

where c_1^n, c_2^n and c_5^n (with the superscript "n") are the *normalized* Taylor's coefficients. Note from (4b) that the first-order coefficient is reduced to $c_1^n = 2a$ for $a \gg 0$ (strong inversion MOSFETs) and, after de-normalization, this yields the usual small-signal characteristic of a non-saturated MOSFET resistor [6]. To further simplify the analysis, the difference of square logarithmic operation is approximated by a third-order polynomial, i.e., the fifth-order coefficient c_5^n in (4d) is omitted. The validity of this simplification will be discussed soon. Following this, by substituting the third-order Taylor's series in (4) into (3), after some rearrangement, we obtain

$$g_2x=\underbrace{(g_1+c_{11}^n)z+c_{31}^nz^3}_{y}+\underbrace{\left(g_2+rc_{12}^n\right)z+rc_{32}^nz^3}_{h} \quad (5)$$

where $c_{11,31}^n$ are the normalized coefficients for the MOSFET pair M_1 and $c_{12,32}^n$ are those for M_2. It is observed from (5) that, for a linear characteristic between x and y, h must be linearly dependent on y, i.e., $h = \delta y$ where δ is a constant. It is interesting to note that, with reference to the Norton's equivalent circuit of Fig. 2, the variable y corresponds to the normalized current $i_o/I_{Z1} = i_1/I_{Z1}$ in the M_1-R_1 branch, and h corresponds to the normalized current i_2/I_{Z1} in the M_2-R_2 branch. By using (5), the linear dependence condition implies the following relation:

$$\frac{g_2+rc_{12}^n}{g_1+c_{11}^n}=r\cdot\frac{c_{32}^n}{c_{31}^n}=\delta. \quad (6)$$

Using (5) and (6), we obtain $y = g_2(1+\delta)^{-1}x$. After denormalizing the associated variables, the differential characteristic of the sub-threshold R-MOSFET resistor is thus given by

$$i_o=R_{eff}^{-1}v_{in}=\left[(1+\delta)R_2\right]^{-1}v_{in}. \quad (7)$$

For ease of implementation and characterization, the transistor pairs M_1 and M_2 should be integer multiples of the same unit MOSFET. By assigning the number of unit transistors at n_1 for M_1 and at n_2 for M_2, the parameter relation for a perfect linearization can be obtained by de-normalizing (6), and this yields

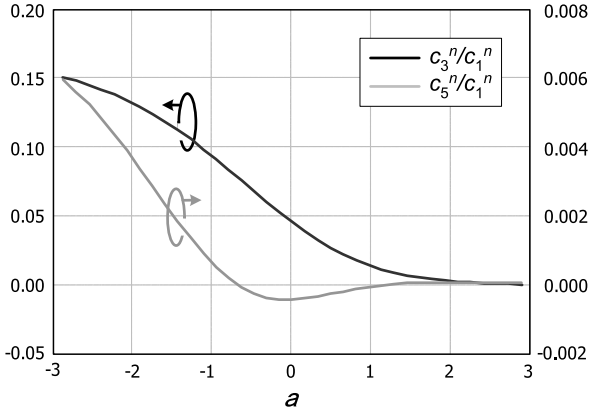

Fig. 3 Normalized Taylor's coefficients ratios c_3^n/c_1^n and c_5^n/c_1^n of MOSFET pair's normalized I-V characteristics.

$$\frac{R_2^{-1}+n_2\cdot c_1(V_{C2})}{R_1^{-1}+n_1\cdot c_1(V_{C1})}=\frac{n_2\cdot c_3(V_{C2})}{n_1\cdot c_3(V_{C1})}=\delta \quad (8)$$

where $c_{1,3}(V_C)$'s are the *normal* coefficients of the third-order polynomial describing the differential current-voltage characteristic of the unit MOSFET pair at the gate control voltage V_C. Note that these may be obtained by de-normalizing (4b) and (4c).

From the analysis outlined above, Eqs. (7), (8) are central to the analysis and design of the sub-threshold R-MOSFET resistor. Inspection of (8) also reveals that scaling of the effective resistance from R_{eff} to $k \cdot R_{eff}$ can be simply obtained, without upsetting the linearization condition, by modifying R_1, R_2 by the factor k and n_1, n_2 by the inverse $1/k$.

It is important to point out that the third-order polynomial approximation applied in the forgoing analysis is valid for MOSFET operation in strong to moderate inversion. This is evident as shown in Fig. 3 which provides the plots versus a of the ratios of the third-order and the fifth-order to the first-order normalized coefficients, c_3^n/c_1^n and c_5^n/c_1^n, using (4). At weak inversion operation (approximately at $a < -1$ or $(V_{C1} - V_{T0} - mV_Q) < -2m\phi_t$), the characteristic of the MOSFET pair becomes increasingly nonlinear and it can be seen from the ratio plots that the fifth-order term can no longer be omitted. Nevertheless, as will be evident in the experiments and simulations of Sect. 3, if the coefficients $c_{1,3}(V_C)$ in (8) are to be determined *empirically* from the unit MOSFET characteristic at various V_Cs, instead of being calculated from (4b), (4c), it is possible to fit the characteristics with the third-order polynomial while still obtaining a reasonable accuracy. In this way, the use of the developed equations in (8) can be extended down to weak

MOSFET operation. In fact, such empirical coefficient determination is valid for more general conditions [7]. That is, with proper fitting values of c_1 and c_3, all the second-order effects omitted in (1) are automatically incorporated. Since this approach is simple and yet provides good accuracy in practice, it will be employed in Sect. 3.

2.3 Design Discussion

For an ideal operation of the sub-threshold R-MOSFET resistor, when the main control voltage V_{C1} of M_1 is changed, the auxiliary control voltage V_{C2} of M_2 should be adjusted accordingly in order to maintain good linearity over the entire resistance tuning range. For ease of implementation however, it should be more convenient to maintain V_{C2} at a constant voltage. In such a case, the condition for a perfect non-linearity cancellation is satisfied at a *single* set of V_{C1} and V_{C2} through proper selection of R_1, R_2 and the dimensions of M_1 and M_2 according to (8). Only a partial cancellation is obtained at other set of control voltages. As will be demonstrated by both experiments and simulations, the constant V_{C2} scheme proves to be effective for moderate linearity applications, provided that particular attention is paid to satisfying the linearization condition at a set of V_{C1} and V_{C2} within the sub-threshold operation of the MOSFETs where the nonlinearity is most pronounced. With such a design consideration, adequate resistance tunability with good linearity over the entire range can be ensured.

3. Performance Verification

3.1 Experimental Results

The integrity of the analysis and design, and the functionality of the sub-threshold R-MOSFET resistor, were first verified via breadboard implementation using the n-channel MOSFET of an ALD1106 transistor array as the unit transistor. To facilitate the test, the R-MOSFET resistor was built around off-the-shelf opamps with negative feedback using linear resistors to form a differential inverting amplifier where the differential output current i_o in Fig. 1 can be measured indirectly via the amplifier's output voltage. For this breadboard design, the terminal input/output quiescent voltages were chosen at $V_Q = 0.5$ V. Measurement indicates the extrapolated nominal threshold voltage of the MOSFET at $V_{T0} \approx 0.65$ V and this is increased to $V_{TB} \approx 0.88$ V for $V_D = V_S = V_Q = 0.5$ V and $V_B = 0$. Therefore, the gate control voltage V_C below $V_Q + V_{TB} \approx 1.38$ V covers the sub-threshold operation. For the selected V_C range from 1.25 V to 1.50 V, the measured differential characteristic of the ALD1106 nMOS pair at $V_Q = 0.5$ V are depicted in Fig. 4. Also given are the calculated plots based on the extracted polynomial coefficients c_1s and c_3s (using MATLAB) in Table 1 for each corresponding V_C where close agreement with measurement is observed.

For ease of tuning, the scheme with a fixed gate voltage for V_{C2} was adopted. In this design example, the numbers

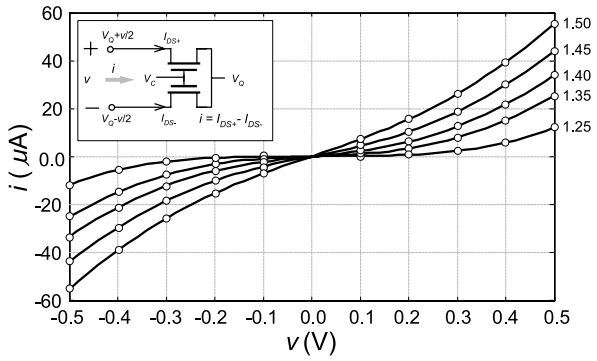

Fig. 4 Measured (solid) and calculated (marker) differential characteristics of ALD1106 unit MOSFET pair at different V_Cs.

Table 1 Empirical coefficients for ALD array MOSFET pair.

V_C	1.25	1.30	1.35	1.40	1.45	1.50
c_1/c_3	0.022	0.098	0.238	0.454	0.717	1.033
$(\cdot 10^{-4})$	/1.35	/1.79	/1.89	/1.77	/1.62	/1.46

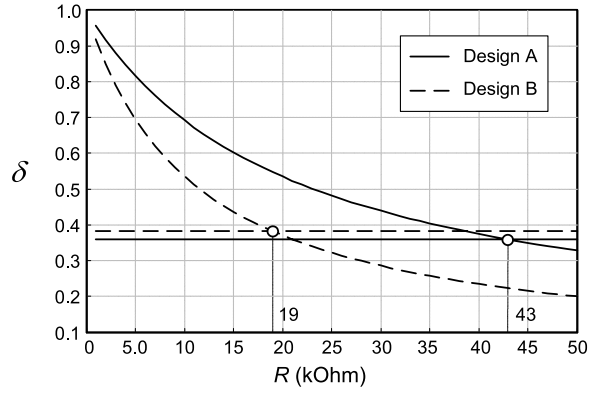

Fig. 5 Design curves for sub-threshold resistor using ALD1106.

of the unit transistors at $n_1 = 2$ and $n_2 = 1$ and an identical resistance $R_1 = R_2 = R$ were selected. To determine the linearization conditions, the ratios on the left- and right-hand sides of (8) are plotted against the resistance R, where the intersection between the two curves indicates the designed resistance value. Based on the extracted coefficients in Table 1, the plots for two example designs for linearization at different V_Cs are shown in Fig. 5. For design A with the linearization at $V_{C1} = 1.35$ V and $V_{C2} = 1.25$ V, the intersection yields $R = 43\,\mathrm{k}\Omega$. For design B with the linearization at $V_{C1} = 1.40$ V and $V_{C2} = 1.25$ V, we obtain $R = 19\,\mathrm{k}\Omega$. In the test, available resistor values were used, i.e., $R = 50\,\mathrm{k}\Omega$ for design A, and $R = 20\,\mathrm{k}\Omega$ for design B. It should be noted that the selected $V_{C2} = 1.25$ V for both designs results in the operation of M_2 at ~130 mV less than the threshold voltage.

Figure 6 shows the measured resistance characteristics, which were extracted from the measured small-signal voltage gain versus V_{C1} at an input v_{in} of 0.1 V_p (differential peak voltage). Also given for comparison are the calculated resistances using (7) based on the coefficients in Table 1. It is seen that R_{eff} can be tuned from 55 kΩ to 97 kΩ, yield-

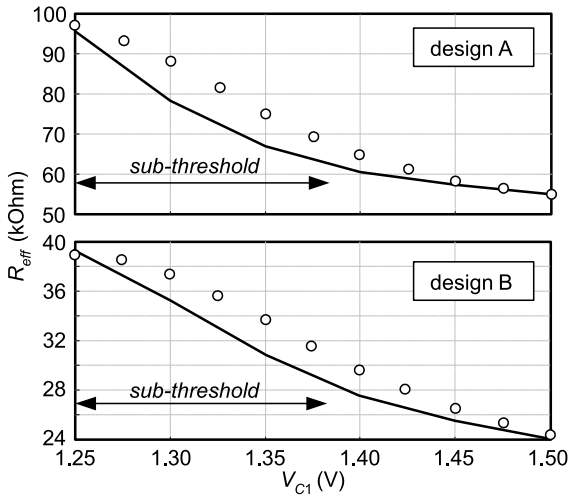

Fig. 6 Measured (marker) and calculated (solid) small-signal resistance versus V_{C1}.

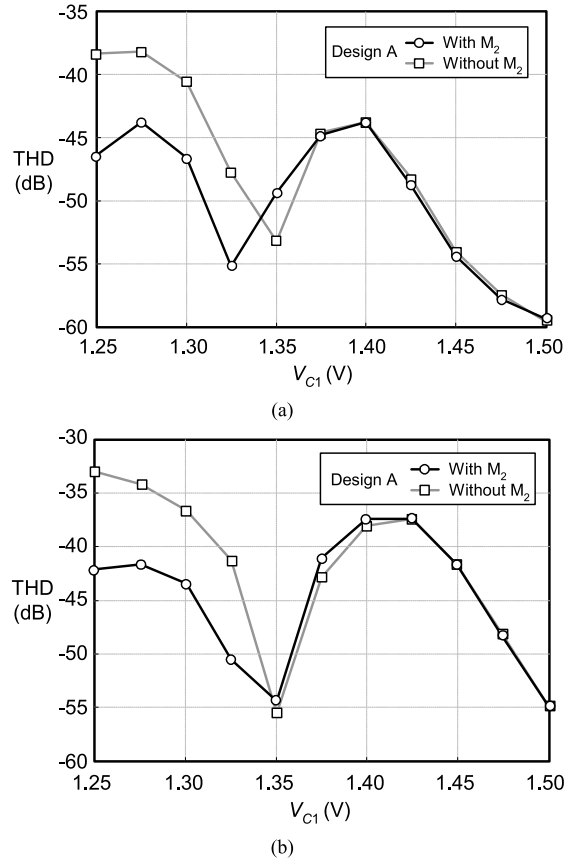

Fig. 7 Measured THD performances at 10 kHz input frequency of design A at (a) 0.4 V_p input and (b) 0.8 V_p input.

ing the tuning ratio at ~1.76 for design A. For design B, R_{eff} can be tuned from 24.5 kΩ to 38 kΩ, giving the tuning ratio at ~1.55. Also, based on the measured values, the sub-threshold operation in the MOSFETs covers the resistance tuning range by more than 50% for both designs A and B.

Figures 7 and 8 show the measured total harmonic dis-

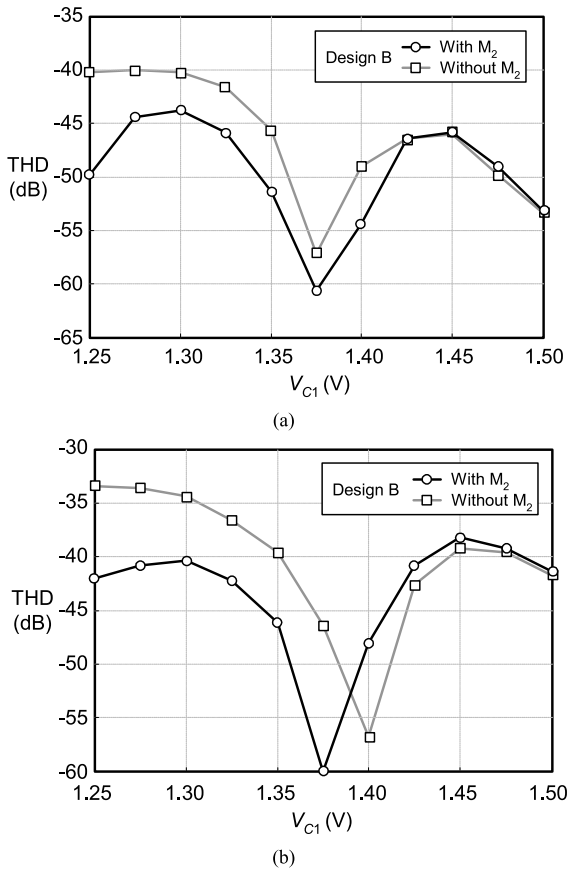

Fig. 8 Measured THD performances at 10 kHz input frequency of design B at (a) 0.4 V_p input and (b) 0.8 V_p input.

tortion (THD) of the output voltage v_o versus V_{C1}, at v_{in} = 0.4 V_p and 0.8 V_p (differential peak voltage). For design A, the plots indicate the dips in the THD of the sub-threshold resistor at the intermediate control voltage V_{C1} = 1.325 V at 0.4 V_p, and at V_{C1} = 1.35 V for the test inputs at 0.8 V_p. For design B, the dips occur at V_{C1} = 1.375 V for both of the test inputs. These voltage locations are in close agreement with the design specifications, i.e., at V_{C1} = 1.35 V for design A, and at V_{C1} = 1.40 V for design B. Some discrepancies are mainly due to the approximation of the MOSFET characteristics by the third-order polynomial.

Also included for comparison in Figs. 7 and 8 are the THD plots when the transistor pair M_2 in Fig. 1 was removed and the circuit was turned into the conventional series-parallel R-MOSFET resistor. As observed, the proposed sub-threshold resistors can provide THD improvement, particularly over the V_{C1} range where M_1 operates in sub-threshold inversion. For the range of V_{C1} where M_1 is in strong operation, almost identical linearity is displayed between the two resistors as the effect of M_2 becomes negligible.

3.2 Simulation Results

The performance of the sub-threshold R-MOSFET resistor

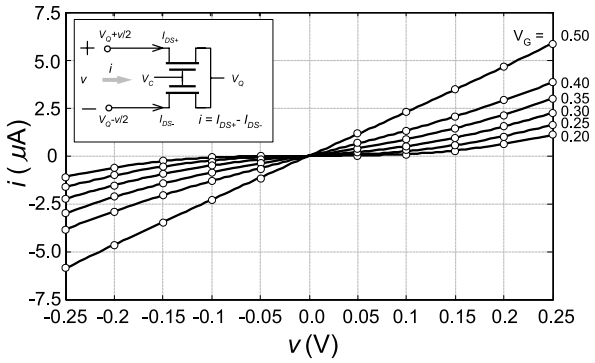

Fig. 9 Simulated (solid) and calculated (marker) differential characteristics of the low-threshold unit MOSFET pair at different V_Cs.

Table 2 Empirical coefficients for low threshold MOSFET pair.

V_C	0.2	0.25	0.3	0.35	0.4	0.50
c_1/c_3	0.003	0.019	0.045	0.082	0.127	0.228
$(\cdot 10^{-4})$	/0.677	/0.785	/0.766	/0.629	/0.427	/0.108

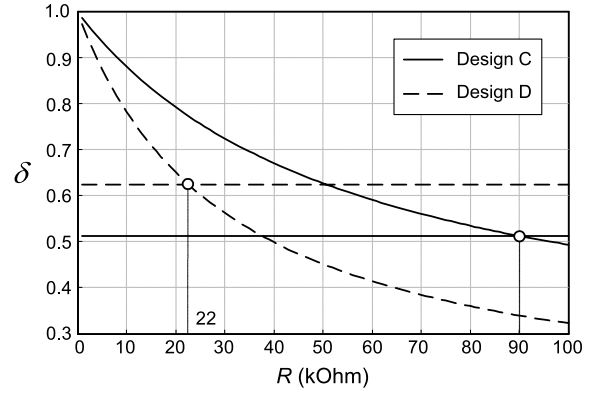

Fig. 10 Design curves for sub-threshold resistor using 0.18 μm CMOS.

in IC implementation was also demonstrated via simulation using the *low-threshold* n-channel MOSFET of the UMC 1.8-V 0.18 μm CMOS process with the gate tuning voltage below the supply at 0.5 V. Unlike the transistor array implementation, the output current $i_o = i_{o+} - i_{o-}$ in Fig. 1 was measured directly in simulation. For this example application at a 0.5-V supply, the quiescent voltage V_Q was set at a half-supply level, $V_Q = 0.25$ V. The unit transistor was selected at $W/L = 1.1\,\mu$m/4.0 μm. As extrapolated from simulation, the threshold voltage of the MOSFET is $V_{TB} \approx 0.05$ V at $V_D = V_S = V_Q = 0.25$ V and $V_B = 0$ V whereas the nominal value is $V_{T0} \approx 0.01$ V. Thus, the transistor enters sub-threshold operation at V_C below $V_Q + V_{TB} \approx 0.30$ V. The simulated and calculated differential characteristics of the unit MOSFET pair at various V_Cs are shown in Fig. 9, and the extracted polynomial coefficients that fit the curves are given in Table 2.

Similar to the breadboard design, the fixed gate voltage scheme for V_{C2} was employed and $R_1 = R_2 = R$ was selected. In design C, the numbers of the unit transistors were given at $n_1 = 4$ and $n_2 = 2$ and the perfect linearization condition was set at $V_{C1} = 0.30$ V and $V_{C2} = 0.25$ V. By using (8) and the extracted coefficients in Table 2, Fig. 10 shows the design curves [cf. Fig. 5 for designs A-B] where $R = 90\,\mathrm{k}\Omega$ is obtained for design C. For design D, another linearization condition at $V_{C1} = 0.35$ V and $V_{C2} = 0.25$ V, was selected and this yields $R = 22\,\mathrm{k}\Omega$. Note that for both designs, the control voltage $V_{C2} = 0.25$ V results in the operation of M_2 at ∼50 mV less than the threshold voltage.

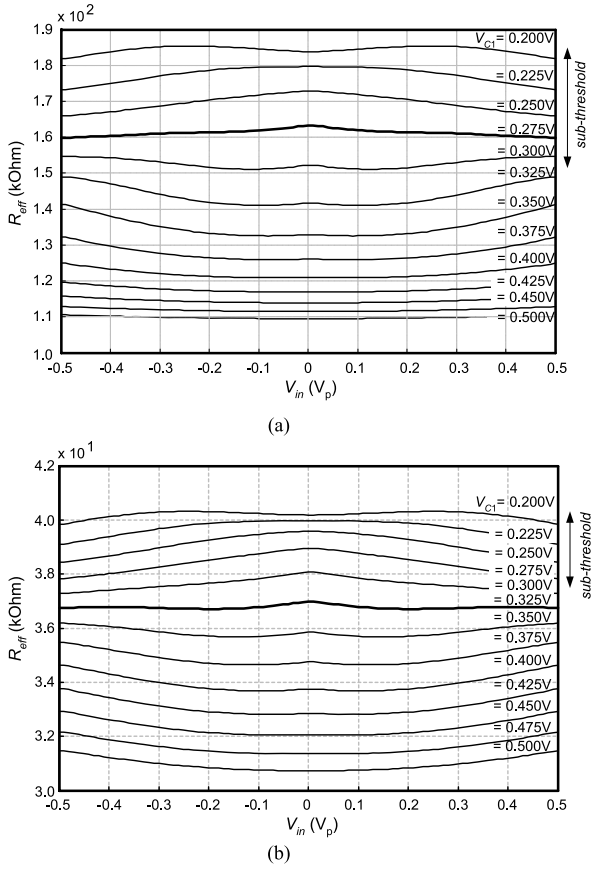

Fig. 11 Simulated resistance characteristics at different V_Cs for (a) Design C and (b) Design D.

Figures 11(a), (b) show the simulated resistance characteristic under typical process and temperature for designs C and D with V_{C1} ranging from 0.2 V to 0.5 V and the differential peak input v_{in} between $-0.5\,\mathrm{V_p}$ and $0.5\,\mathrm{V_p}$. It is noticed that the simulated characteristics are close to straight lines at V_{C1}= 0.275 V for design C and V_{C1} = 0.325 V for design D in close agreement with the specifications. For design C, R_{eff} can be tuned from 110 kΩ to 184 kΩ with the tuning ratio at ∼1.67, and from 30.8 kΩ to 40.6 kΩ with the tuning ratio at ∼1.32 for design D. Also note from the plots that the sub-threshold operation in the MOSFETs occupies about 40% of the resistance tuning range for design C, and about 30% for design D.

Figure 12 shows the simulated THD performances versus V_{C1} at $v_{in} = 0.5\,\mathrm{V_p}$. Compatible with the resistance plots of Fig. 11, the distortions of the sub-threshold resistors under typical process and temperature exhibit interme-

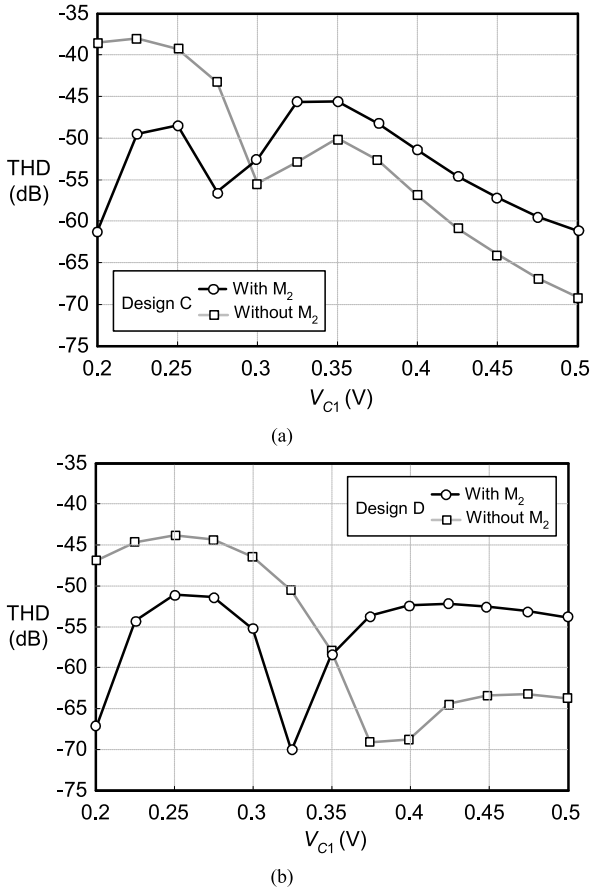

Fig. 12 Distortion performances of sub-threshold and series-parallel resistors at typical conditions and 10 kHz input for (a) Design C and (b) Design D.

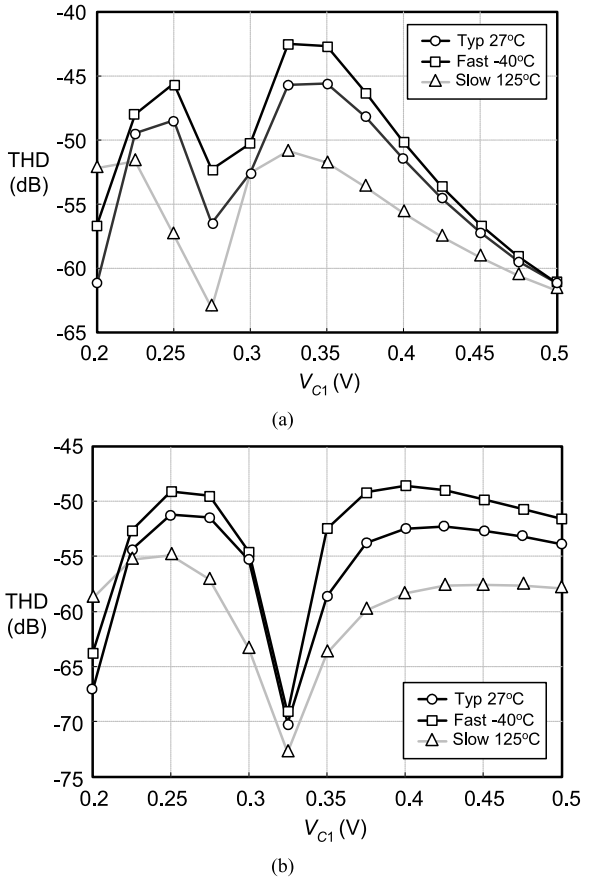

Fig. 13 Distortion performances at extreme conditions (a) Design C and (b) Design D.

diate dips at V_{C1} = 0.275 V for design C, and at V_{C1} = 0.325 V for design D. Also included in the figure are the THD plots of the corresponding series-parallel R-MOSFET resistors. Similar to the measured results of Figs. 7 and 8, improvement in the THD for the range of V_{C1} which yields sub-threshold operation in M_1 is clearly observed. Unlike the measured results however, the series-parallel counterparts exhibit somewhat less distortion at strong operation in M_1. This is due to the fact that, for designs C and D, M_2 was selected to operate at ∼50 mV below the threshold voltage, as compared to ∼130 mV for the case of designs A and B. This results in over-compensation of the nonlinearity in M_1 by M_2 when M_1 enters a triode strong region of operation with a linear characteristic. Nonetheless, it can be seen from Fig. 12 that the sub-threshold resistors could offer better overall THD performance over the tuning voltage, extending down to weak inversion operation in the MOSFETs.

To demonstrate robustness of the sub-threshold R-MOSFET resistor, the simulated THD performances over extreme process and temperature conditions are given in Figs. 13(a), (b) where the intermediate drops of the THDs at the same corresponding V_{C1}s under the typical conditions are noticed for both designs. Also, the plots indicate the THD better than −42 dB in the sub-threshold resistor over the extreme conditions.

To investigate the impact of component mismatches on linearity, systematic mismatches at 10% were introduced to the resistor pairs R_1 and R_2, as well as the channel width W of the transistor pairs M_1 and M_2. For the threshold mismatch in the transistor pairs, it was set at 5% of the supply voltage, i.e., ΔV_{TB} = 25 mV. The resulting simulated THDs versus inputs under the assigned mismatches are given in Fig. 14 alongside the plots with perfect matching, both at typical conditions of designs C and D. Note that the THD plots are given at V_{C1} = 0.25 V since this yields the worst distortion performances in both designs under sub-threshold operation in M_1 and M_2 [cf. Fig. 12]. It is seen that such mismatches cause the distortion to increase at low inputs by as much as 9 dB, and this is primarily due to considerable increase in the second harmonic distortion components. At larger inputs, the degradation in the THD is successively reduced. At the maximum input of 0.5 V_p, the distortion level is practically intact for design C, where it is increased by less than 1 dB for design D, suggesting good robustness in linearity against mismatches at high input levels.

Also simulated was the performance of the sub-threshold resistors in terms of the frequency response. These are as shown in Figs. 15(a) and 15(b) for the i_o/v_{in} characteristics at typical conditions and different V_{C1}s. It is evident

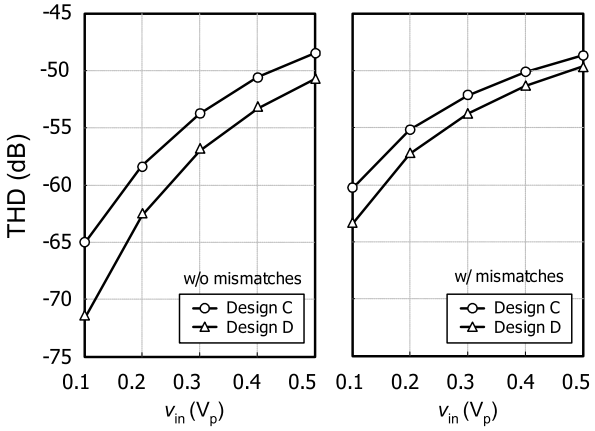

Fig. 14 Simulated THD performances versus input for design C and D under typical conditions at V_{C1} = 0.25 V with and without systematic mismatches.

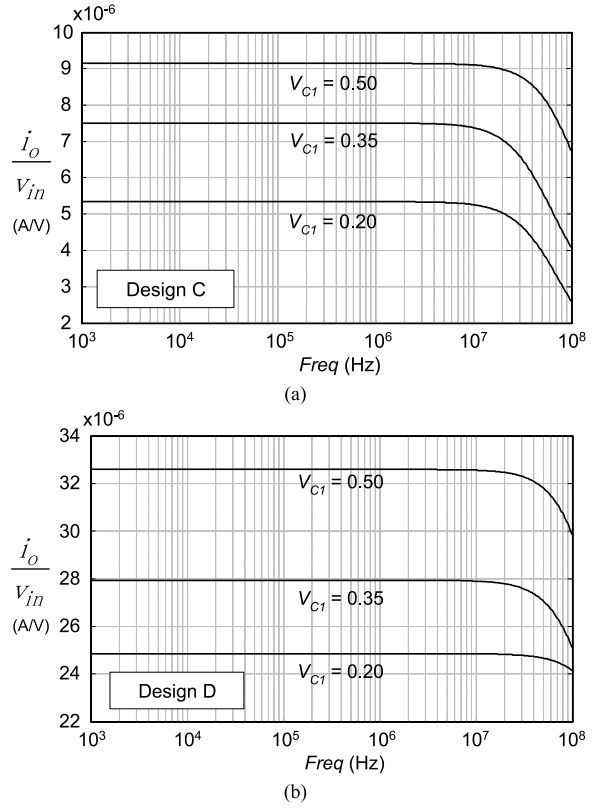

Fig. 15 Simulated frequency responses at V_{C1} = 0.2 V, 0.35 V and 0.5 V for (a) Design C and (b) Design D.

that the operation up to several tens of MHz is feasible for the resistances of design C and D which are in the order of ten to hundred kilo-ohms [cf. Fig. 11]. Finally, to verify the scaling property, both the sub-threshold R-MOSFET resistors were scaled by a factor k = 1/4, i.e., with R_1 = R_2 = 22.5 kΩ, n_1 = 16 and n_2 = 8 for design C, and R_1 = R_2 = 5.5 kΩ, n_1 = 16 and n_2 = 8 for design D. Simulation indicates corresponding reduction of the effective resistances [cf. Fig. 11] by a factor of four whereas there is practically no change on the distortion performances [cf. Figs. 12–14].

4. Conclusions

The analysis, design and performance verification of the sub-threshold R-MOSFET tunable resistor with extended MOSFET operation from traditional non-saturated strong inversion to saturated sub-threshold inversion have been presented. The operation of the sub-threshold resistor was described to rely upon a parallel of two non-linear resistive branches with a linear dependency to achieve a linear input/output characteristic. The analysis was first outlined based on a general MOS equation valid for all regions of operation. Various approximations including the use of a third-order polynomial to represent the characteristic of a MOSFET pair were subsequently introduced and this led to operational insight and practical design conditions of the sub-threshold resistor to ensure a good linearity over the tuning range. Extensive verification of its functionality and performance was given via breadboard experiments, and its feasibility in IC realization via simulation. Based on the achievable distortion performances, the sub-threshold resistor technique should prove very useful for a very low supply continuous-time filter implementation with a moderate linearity requirement.

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References

[1] S. Chatterjee, Y.P. Tsividis, and P. Kinget, "0.5-V analog circuit techniques and their applications to OTA and filter design," IEEE J. Solid-State Circuits, vol.40, pp.2373–2387, Dec. 2005.
[2] G. Vemulapali, P.K. Hanumolu, Y.J. Kook, and U.K. Moon, "A 0.8-V accurately tunned linear continuous-time filter," IEEE J. Solid-State Circuits, vol.40, pp.1972–1977, Sept. 2005.
[3] U.K. Moon and B.S. Song, "Design of a low-distortion 22-kHz fifth-order bessel filter," IEEE J. Solid-State Circuits, vol.28, pp.1254–1263, Dec. 1993.
[4] Y.P. Tsividis, M. Banu, and J. Khoury, "Continuous-time MOSFET-C filters in VLSI," IEEE J. Solid-State Circuits, vol.21, pp.15–30, Feb. 1986.
[5] A. Worapishet and P. Khumsat, "Sub-threshold R-MOSFET tunable resistor technique," Electron. Lett., vol.43, no.7, March 2007.
[6] Y.P. Tsividis, Operation and Modeling of The MOS Transistor, 2nd ed., McGraw-Hill, 1999.
[7] M. Banu and Y.P. Tsividis, "Detailed analysis of non-idealities in MOS fully integrated active RC filters based on balanced networks," IEE Proc. G, vol.131, pp.190–196, Oct. 1984.

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