ALD metal-gate/high-κ gate stack for Si and Si$_{0.7}$Ge$_{0.3}$ surface-channel pMOSFETs


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Abstract

ALD high-κ dielectrics and TiN metal-gate were successfully incorporated in both Si and Si$_{0.7}$Ge$_{0.3}$ surface-channel pMOSFETs. The high-κ gate dielectrics used included Al$_2$O$_3$/HfO$_2$/Al$_2$O$_3$, Al$_2$O$_3$/HFO$_2$/Al$_2$O$_3$, and Al$_2$O$_3$. The Si transistors with Al$_2$O$_3$/HfO$_2$/Al$_2$O$_3$ showed a sub-threshold slope of 75 mV/dec. and a density of interface states of $3 \times 10^{10}$ cm$^{-2}$V$^{-1}$. No obvious degradation of the Si channel hole mobility was observed. The Si$_{0.7}$Ge$_{0.3}$ pMOSFETs with the various high-κ gate dielectrics demonstrated enhanced transconductance, drive current and channel hole mobility compared with the Si reference.

1. Introduction

As the aggressive down-scaling in CMOS technology continues, the need for high-κ gate-dielectrics in place of the traditional SiO$_2$ increases in order to provide extremely scaled equivalent oxide thickness (EOT) on the order of 1 nm for effective control of short channel effect (SCE) without remarkable increase of gate leakage current [1]. High-κ dielectric materials such as the oxides, silicates or aluminates of Hf and Zr are being intensively investigated [2-4]. Particularly, HfO$_2$ has shown good properties with a dielectric constant up to 20, reasonable barrier height (1.5 eV) towards both conduction band minimum and valence band maximum of Si, and good thermal stability with Si. Recently, thin ALD high-κ gate dielectrics were successfully incorporated in both Si and Si$_{0.7}$Ge$_{0.3}$ surface-channel pMOSFETs [20]. The high-κ dielectrics used included Al$_2$O$_3$/HfO$_2$/Al$_2$O$_3$, Al$_2$O$_3$/HFO$_2$/Al$_2$O$_3$, and Al$_2$O$_3$. The Si transistors with Al$_2$O$_3$/HfO$_2$/Al$_2$O$_3$ showed a sub-threshold slope of 75 mV/dec. and a density of interface states of $3 \times 10^{10}$ cm$^{-2}$V$^{-1}$. No obvious degradation of the Si channel hole mobility was observed. The Si$_{0.7}$Ge$_{0.3}$ pMOSFETs with the various high-κ gate dielectrics demonstrated enhanced transconductance, drive current and channel hole mobility compared with the Si reference.

2. Device fabrication

The devices were fabricated on p-type Si (100) substrates using a conventional CMOS process. The n-well was uniformly doped to $3 \times 10^{17}$ cm$^{-3}$. After the formation of LOCOS isolation, channel implantation was performed to form a retrograde channel profile with a surface concentration of $4 \times 10^{18}$ cm$^{-2}$. A 10-nm thick undoped strained Si$_{0.7}$Ge$_{0.3}$ layer and its underlying Si buffer were selectively grown to form the Si$_{0.7}$Ge$_{0.3}$ surface-channel pMOSFET, using reduced-pressure CVD. A 20-nm thick undoped Si layer was grown for the Si channel devices. The thickness and composition for the epitaxial layers are nominal values obtained on blanket calibration wafers. Prior to the deposition of the metal-gate/high-κ stack, the wafers were cleaned in a dilute HF solution (0.5 % in H$_2$O) and rinsed with de-ionized water. Al$_2$O$_3$/HfO$_2$/Al$_2$O$_3$ (0.5/4/0.5 nm) laminate film was deposited on Si devices in an ALCVD reactor using Al(CH$_3$)$_3$, HfCl$_4$, and H$_2$O at 300 °C. For the Si$_{0.7}$Ge$_{0.3}$ pMOSFETs, three kinds of 5-nm thick high-κ dielectrics were deposited: Al$_2$O$_3$/HfO$_2$/Al$_2$O$_3$ (0.5/4/0.5 nm), Al$_2$O$_3$ (5 nm) and Al$_2$O$_3$/HfAlO$_3$/Al$_2$O$_3$ (0.5/4/0.5 nm). For the TiN deposition, TiCl$_4$ and NH$_3$ were used. The stoichiometry of the TiN layer was 1:1. After gate patterning, TiN metal gate was dry-etched by using a gas chemistry of BCl$_3$ and Cl$_2$. After extension and deep source/drain implantations, the samples were annealed at 930 °C in N$_2$ for 10 s. Post-metalization sintering was performed in forming gas at 400 °C for 30 min. Finally, the samples were annealed in H$_2$O vapor at 300 °C for two hours. The schematic cross-section of a fabricated Si$_{0.7}$Ge$_{0.3}$ surface-channel pMOSFET is shown in Fig. 1.
3. Results and discussion

The C-V data for the various high-\(\kappa\) dielectrics of Si and Si\(_{10.7}\)Ge\(_{0.3}\) pMOSFETs are shown in Fig. 2. An EOT of 3.4, 2.8 and 2.3 nm was extracted for the Si\(_{10.7}\)Ge\(_{0.3}\) pMOSFETs with Al\(_2\)O\(_3\), Al\(_2\)O\(_3\)/HfAlO\(_x\)/Al\(_2\)O\(_3\) and Al\(_2\)O\(_3\)/HfO\(_2\)/Al\(_2\)O\(_3\), respectively, which indicates the presence of a \(\sim\)1.3-nm thick interfacial SiO\(_2\) using \(\varepsilon_r=10\) for Al\(_2\)O\(_3\) and 20 for HfO\(_2\) [9]. The interfacial SiO\(_2\) was likely introduced prior to the ALCVD processing. The Si pMOSFET showed a similar EOT compared to the Si\(_{10.7}\)Ge\(_{0.3}\) channel pMOSFETs with the Al\(_2\)O\(_3\)/HfAlO\(_x\)/Al\(_2\)O\(_3\) gate dielectric, \(\varepsilon_r=14\) was obtained for the HfAlO\(_x\). The kinks observed on the C-V curves of the Si\(_{10.7}\)Ge\(_{0.3}\) devices in the accumulation region around \(V_C=\pm 1\) V are likely to result from slow interface states close to the conduction band of the surface Si\(_{10.7}\)Ge\(_{0.3}\) layer [10]. The strained Si\(_{10.7}\)Ge\(_{0.3}\) layer has a bandgap of 0.92 eV, smaller than that for Si (1.1 eV). Hence with the same Al\(_2\)O\(_3\)/HfAlO\(_x\)/Al\(_2\)O\(_3\), both Si\(_{10.7}\)Ge\(_{0.3}\) and Si devices enter the accumulation at a similar gate voltage, while the gate voltage at which inversion occurs is considerably more negative for the Si device resulting in a larger voltage interval on the C-V curve (Fig. 2).

The work function of the ALD TiN gate was determined experimentally as 5.0 eV, on a separate wafer with MOS capacitors of thermally grown SiO\(_2\) to different thicknesses. As evident in Fig. 2, no gate depletion effect was found due to the use of the TiN metal-gate for both Si\(_{10.7}\)Ge\(_{0.3}\) and Si channel devices. The extracted threshold voltages of the fabricated Si\(_{10.7}\)Ge\(_{0.3}\) and Si transistors with different gate lengths are shown in Fig. 3. The differences in threshold voltage among the Si transistors and the Si\(_{10.7}\)Ge\(_{0.3}\) transistors with both Al\(_2\)O\(_3\)/HfO\(_2\)/Al\(_2\)O\(_3\) and Al\(_2\)O\(_3\)/HfAlO\(_x\)/Al\(_2\)O\(_3\) can be partly explained by the valence band offset between the Si and strained Si\(_{10.7}\)Ge\(_{0.3}\) layers and by the different EOT values obtained for the high-\(\kappa\) dielectrics. The threshold voltages of the Si\(_{10.7}\)Ge\(_{0.3}\) transistors with the Al\(_2\)O\(_3\), however, are considerably higher than the simulated ideal ones, indicating that there could be large amounts of negative fixed charges in the Al\(_2\)O\(_3\) layer. The Al\(_2\)O\(_3\) dielectric also showed a substantially higher density of slow traps than the two-sandwiched dielectrics [11], according to low-frequency noise measurements. The origin of the fixed charges and/or slow states in the Al\(_2\)O\(_3\) is being investigated.

The density of interface states for the Si transistor was measured to be \(3\times 10^{11}\) cm\(^2\)eV\(^{-1}\), using charge-pumping method. The density of interface states for the Si\(_{10.7}\)Ge\(_{0.3}\) transistors with the various high-\(\kappa\) dielectrics, however, ranged from \(1.6\times 10^{12}\) to \(1.8\times 10^{12}\) cm\(^2\)eV\(^{-1}\). The density of gate leakage current for the Si\(_{10.7}\)Ge\(_{0.3}\) and Si transistors is shown in Fig. 4. Though the leakage currents for the Si\(_{10.7}\)Ge\(_{0.3}\) devices with the various high-\(\kappa\) dielectrics is generally higher than that for the Si device, which is likely caused by the higher density of interface states, they are still comparable to that of a Si transistor with SiO\(_2\) of the same EOT [12].

The \(I_{DS}\)–\(V_{GS}\), \(g_{m}\)–\(V_{GS}\) and \(I_{DS}\)–\(V_{DS}\) characteristics for the Si and Si\(_{10.7}\)Ge\(_{0.3}\) transistors with \(L_G=10\) \(\mu\)m and \(W_G=50\) \(\mu\)m are shown in Fig. 5, Fig. 6, and Fig. 7, respectively. The Si transistor displays a good sub-threshold behavior with a sub-threshold slope of 75 mV/dec. (Fig. 5). The Si\(_{10.7}\)Ge\(_{0.3}\) transistor with the same high-\(\kappa\) dielectric Al\(_2\)O\(_3\)/HfAlO\(_x\)/Al\(_2\)O\(_3\), however, shows a higher sub-threshold slope, 110 mV/dec., due to the higher density of interface states. The difference in sub-threshold slope for the Si\(_{10.7}\)Ge\(_{0.3}\) transistors, 135 mV/dec. for Al\(_2\)O\(_3\) and 105 mV/dec. for Al\(_2\)O\(_3\)/HfO\(_2\)/Al\(_2\)O\(_3\), is mainly due to the EOT difference since the density of interface states is similar for the devices. Improvements in both peak transconductance (Fig. 6) and drive current (Fig. 7) up to 30 % are found for the Si\(_{10.7}\)Ge\(_{0.3}\) transistor with Al\(_2\)O\(_3\)/HfAlO\(_x\)/Al\(_2\)O\(_3\), compared to the Si transistor with the same high-\(\kappa\) stack. As expected, the Si\(_{10.7}\)Ge\(_{0.3}\) transistor with Al\(_2\)O\(_3\)/HfO\(_2\)/Al\(_2\)O\(_3\) shows the highest transconductance and drive current since its EOT is the smallest. The Si\(_{10.7}\)Ge\(_{0.3}\) transistor with Al\(_2\)O\(_3\) still shows higher transconductance and drive current than the Si transistor, despite of its larger EOT value.
The Si and Si$_{0.7}$Ge$_{0.3}$ transistors of $L_G$=0.6 $\mu$m were also found to be well-performing, similarly to their counterparts of $L_G$=10 $\mu$m, though the threshold voltages differed (Fig. 3). In Fig. 8, the $I_{DS}$–$V_{GS}$ characteristics for such short-channel devices are shown. No degradation of the sub-threshold slope can be found for the transistors. Similar improvements in transconductance and drive current were also found for the Si$_{0.7}$Ge$_{0.3}$ transistors compared to the Si ones.

The channel hole mobility was evaluated for all transistors using the standard split C-V technique. The results are shown in Fig. 9, along with the universal mobility curve for holes in Si as reference. No obvious mobility degradation is found for the Si transistor since its effective mobility results coincide with the universal curve. This observation implies the great potential of replacing the traditional poly-Si/SiO$_2$ gate stack with an ALD metal-gate/high-$\kappa$ gate stack. For the Si$_{0.7}$Ge$_{0.3}$ devices with the various high-$\kappa$ dielectrics, the mobility is consistently higher than the universal curve at $E_{eff}$ above 0.65 MV/cm. The Si$_{0.7}$Ge$_{0.3}$ transistors with either Al$_2$O$_3$/HfAlO$_x$/Al$_2$O$_3$ or Al$_2$O$_3$/HfO$_2$/Al$_2$O$_3$ show an enhancement in hole mobility amounting to 35% at $E_{eff}$=0.9 MV/cm, as compared to the Si reference or the universal mobility data. At low effective electric field, however, lowered mobility values are observed for the Si$_{0.7}$Ge$_{0.3}$ transistors. In addition, the decrease in mobility towards low effective field does not follow the usual sharp roll-off due to Coulomb scattering by the ionised charge in the channel. This behavior is attributed to the presence of a high density of interface states, which makes the extraction of carrier mobility by the standard
with Al-pMOSFETs has been demonstrated. The Si transistor of $L_0=0.6 \mu$m when the Al degradation of the channel hole mobility was observed. Despite the apparent mobility degradation at low electric field [12], accurate mobility extraction requires correct split C-V technique unreliable at low effective electric field. It is clear that the enhanced channel hole mobility in the Si transistor is responsible for the improved transconductance and drive-current for the Si$_{0.7}$Ge$_{0.3}$ transistors discussed above.

4. Conclusion

A successful integration of ALD high-$\kappa$ dielectric and TiN metal-gate into a standard CMOS process for fabrication of both Si and Si$_{0.7}$Ge$_{0.3}$ surface-channel pMOSFETs has been demonstrated. The Si transistor with Al$_2$O$_3$/HfAlO$_3$/Al$_2$O$_3$ showed fairly low sub-threshold slope of 75 mV/dec. and low density of interface states of $3\times10^{11}$ cm$^{-2}$eV$^{-1}$. No obvious degradation of the channel hole mobility was observed when the Al$_2$O$_3$/HfAlO$_3$/Al$_2$O$_3$ gate dielectric was used in the Si transistor. Although a higher density of interface states and a larger sub-threshold slope were observed, the Si$_{0.7}$Ge$_{0.3}$ pMOSFETs with various high-$\kappa$ gate dielectrics demonstrated enhanced transconductance, drive current and channel hole mobility, as compared with the Si reference. The Si$_{0.7}$Ge$_{0.3}$ transistors with Al$_2$O$_3$/HfO$_2$/Al$_2$O$_3$ exhibited the greatest improvements in transconductance and drive current without further degradation of the channel hole mobility, compared with the Si$_{0.7}$Ge$_{0.3}$ devices with Al$_2$O$_3$/HfAlO$_3$/Al$_2$O$_3$ or Al$_2$O$_3$.

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References