Extended Operation of Cascade Multicell Converters Under Fault Condition

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Abstract—Multilevel converters are an interesting alternative for high power drives, due to their good quality output signals. Despite their advantages, the large number of components required increases the fault probability. Among the multilevel topologies, the cascade multicell converter presents advantages when operating under internal fault conditions, due to its high modularity. Previous works proposed to compensate the unbalanced operation due to a fault by changing the canonical fundamental output phase shift to precalculated angles, depending on the fault condition. This solution assumes that, if the maximum output phase voltage on each leg is used, the maximum line-to-line voltage will be at a maximum as well. This paper shows how this assumption is not always valid and presents the optimum angles and modulation indexes that must be used in order to obtain the maximum balanced load voltages.

Index Terms—Converters, fault tolerance, multilevel converters.

I. INTRODUCTION

AFTER two decades, multilevel converters are still in continuous development in fields such as Static Compensators [1]–[3], photovoltaics [4]–[6], topologies [7]–[9], and modulation and control techniques [10], [11]. All the multilevel topologies, namely, neutral point clamped [12], cascade multicell (CM) [13], [14], and flying capacitor [15], require a large amount of components [16] in order to distribute the voltage and, hence, the power among them. An associated issue related to a high number of components is an increase in the probability of internal fault. However, most multilevel converters allow themselves to be reconfigured in order to work in an under-rated operation mode [14], [17].

This paper is focused on the CM converter operation after an internal fault condition has been detected, either by sensing each power switch or using a more sophisticated method [17]–[19]. A good characteristic of CM converters is that faulty cells can be isolated from the system by using an external switch [T in Fig. 1(b)] that even allows the faulty cell to be replaced by a new one without turning off the system [20]. Then, the problem becomes how to obtain the highest power level with the remaining operative cells.

In [21], the redundant states of the CM converter are used to avoid the switching states that are no longer available due to the fault. As space-vector modulation is used, the well-known hexagon obtained from the α–β transformation changes its geometry, and depending on the fault, a nonregular hexagon or even a rhombus is obtained. Then, a diminished maximum balanced stationary voltage vector, defined by a circular trajectory, is reached.

A different approach is used in [20], where triangular carrier-based PWM modulation is used. In this paper, the fundamental output voltage phase shifts are used to recover the balanced operation. As the phase shift between the inverter output voltages is no longer 120°, a fundamental component is injected into the common mode voltage between the inverter and load neutral points, which not only increases the load voltages but also the voltage stress on the motor bearings, which can lead to a parasitic current sent through them [22], [23].
This paper is focused on the same approach as [20]. An additional degree of freedom is used to calculate the proper fundamental phase-shift angles, in order to provide a solution for faults not covered in that work. As will be shown in Section III, in some cases, a higher balanced line-to-line voltage can be obtained if the modulation index in the higher output inverter voltage is properly set. Moreover, this not only can increase the power delivered to the load but also significantly reduces the possibility that some cells start to regenerate power (a problem briefly announced in [24]), which can severely damage the converter.

Experimental results obtained with an 11-level laboratory prototype are provided to validate the analytical background.

II. CM INVERTER

A. Normal Operation

The CM inverter introduced in [13] and [14] is based on the cascade connection of several structures, known as cells, as shown in Fig. 1(a). Generally, each cell is composed by an H-bridge inverter and an isolated dc voltage source, which can be obtained from the following:

1) a diode bridge fed by a secondary of a multipulse transformer and a capacitive dc link [14] [Fig. 1(b)];
2) a photovoltaic panel [4], [6];
3) batteries [25]–[27].

However, other topologies have been proposed in literature [28], [29].

As the cells are connected in series, the total output voltage for i cells per phase is

$$v_y = v_{yn} = \sum_i v_{yi}, \quad y \in \{a, b, c\}$$  \hspace{1cm} (1)

as shown in Fig. 2(a) for a five-cell-per-phase CM inverter.

On the other hand, each H-bridge can generate up to three voltage levels between its terminals $v_{yi}$; then, the maximum number of voltage levels that can be reached is

$$\hat{l} = 2i + 1.$$  \hspace{1cm} (2)

Many modulation techniques have been developed for this topology [3], [10], [30]–[32]. In this paper, the phase-shifted PWM modulation will be used, due to its easy implementation, modularity, and real application [33].

B. Operation Under Internal Fault

As previously stated, the CM inverter is a fully modular structure. In the case of internal fault of one or more cells per phase, they can be bypassed and hence isolated from the system through an external switch $T$, as shown in Fig. 1(b), while the load can be powered by the rest of the inverter cells. However, while the converter works in fault state, the load will be fed by unbalanced voltages, unless special control and/or modulation schemes are considered.

In [20] and [24], this unbalance, generated by the asymmetrical inverter voltage magnitudes, is compensated by changing the natural 120° fundamental phase shift between the output voltages, by solving the nonlinear equation system

$$V_a^2 + V_b^2 - 2V_a V_b \cos(\alpha) = V_b^2 + V_c^2 - 2V_b V_c \cos(\beta)$$  \hspace{1cm} (3)

$$= V_c^2 + V_a^2 - 2V_c V_a \cos(\gamma)$$  \hspace{1cm} (4)

$$\alpha + \beta + \gamma = 360^\circ$$  \hspace{1cm} (5)

where $\alpha = \angle(\vec{v}_a, \vec{v}_b)$, $\beta = \angle(\vec{v}_b, \vec{v}_c)$, and $\gamma = \angle(\vec{v}_c, \vec{v}_a)$.

In the following sections, the notation $A-B-C$ will be used to denote different fault operation cases, where $A$, $B$, and $C$ will indicate the number of operative cells in the respective phase. As an example, for an 11-level CM, if two cells fail in phase $c$, this notation will lead to 5-5-3. This case is shown in Fig. 2(b), where the inverter and line-to-line voltages are clearly unbalanced. Then, if the load is an electrical machine, pulsating torque will be observed. By using (3)–(5) to rebalance the load voltages, the fundamental output voltage phase-shift angles obtained are

$$\alpha = 95^\circ$$

$$\beta = 132.5^\circ$$

$$\gamma = 132.5^\circ.$$

Then, a balanced line-to-line voltage of 7.36 per unit (p.u.) (an operation 15% lower than normal) is reached, as shown in Fig. 2(c).

Table I summarizes the fundamental phase-shift compensation (FPSC) angles and the maximum line-to-line voltage for...
TABLE I

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>α</th>
<th>γ</th>
<th>$V_{ab}$, pu</th>
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<td>138°</td>
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<td>71°</td>
<td>144°</td>
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<td>111°</td>
<td>137°</td>
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<tr>
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<td>97°</td>
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<td>100°</td>
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<td>3</td>
<td>94°</td>
<td>94°</td>
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<td>60°</td>
<td>60°</td>
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<td>60°</td>
<td>3.48</td>
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<td>1</td>
<td>60°</td>
<td>60°</td>
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<td>5</td>
<td>1</td>
<td>1</td>
<td>60°</td>
<td>60°</td>
<td>1.73</td>
</tr>
</tbody>
</table>

* Balanced line-to-line voltages cannot be obtained with this combination.

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Fig. 3. Operation under fault after the fundamental phase-shift method is applied: (a) 5-3-2 and (b) 4-3-2 faults.

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the possible faults of an 11-level CM inverter. Note, however, that, for some fault conditions, there is no available solution.

III. PROPOSED METHOD

A. Load Voltage Improvement

The previously described method is based on the idea that higher inverter voltages will lead to higher load voltages, which seems to be an obvious assumption. However, it can be observed from Table I that, in fault operation, that idea is not always true. As an example, the operation state 5-3-2 gives a balanced line-to-line voltage of 4.37 p.u., while 4-3-2 gives 4.96 p.u., which is 13.5% higher with one cell less in phase $a$. Both fault conditions, after the FPSC, are shown in Fig. 3.

In mathematics, it is a well-known fact that the biggest difference between two vectors $\vec{a}$ and $\vec{b}$ will occur when the angle between them is 180°; thus, $\vec{l} = \vec{a} + \vec{b}$ reaches a magnitude of

$$||\vec{l}|| = ||\vec{a}|| + ||\vec{b}||.$$  \hfill (6)

This condition is also valid for phasors and, hence, for line-to-line voltages. For a 4-3-2 operation, the angle between $\vec{v}_b$ and $\vec{v}_c$ is $\beta = 187°$, and the line-to-line voltage is close to 5 p.u. On the other hand, for a 5-3-2 operation, the angle is $\beta = 120°$, reducing the line-to-line voltage to 4.36 p.u.

To reach $\beta = 180°$, for 4-3-2, it would be necessary to “push” the inverter neutral point $n$ toward the triangle formed by the line-to-line voltages, which is not possible because phase $a$ cannot increase its voltage over 4 p.u. to keep balanced line-to-line voltages. For 5-3-2, however, it is necessary to “pull” $n$ toward the line-to-line triangle. Fortunately, this can be easily done by reducing the total voltage of $\vec{v}_a$ from $V_a$ to $V'_a$, by properly adjusting the modulation index in this phase only.

Using Fig. 4(a), $V'_a$ and the fundamental phase-shift angles can be calculated as follows:

$$V'_a = \sqrt{V_b^2 + V_b V_c + V_c^2}$$  \hfill (7)

$$\alpha = \arcsin \left( \frac{\sqrt{3} V_b + V_c}{2 V'_a} \right)$$  \hfill (8)

$$\gamma = 180° - \alpha$$  \hfill (9)

$$\beta = 180°.$$  \hfill (10)

Then, for the 5-3-2 operation [see Fig. 4(b)], $V'_a = 4.36$ p.u., $\alpha = 74°$, and $\beta = 96°$, reaching the maximum theoretical balanced line-to-line voltage of 5 p.u.

Note that the proposed method can be applied only when the solution achieved by the traditional FPSC locates the inverter neutral point outside the line-to-line triangle. Table II shows the calculated magnitudes and angles for such cases. It is important to remark that the proposed method can also find a solution for all cases.

B. Load Power Factor Effect

In [24], a relevant drawback of FPSC is mentioned. Depending on the fault and in the load parameters, an inverter phase can receive instead of supply power to/from the load. Then, the cell capacitors of such phase will tend to increase their voltages, which can lead to their destruction, unless clamping circuits or active rectifiers at the input side of each cell [29], [34] are used.

This phenomena can be explained through Fig. 5. The balanced load voltages $v_A$, $v_B$, and $v_C$ generate balanced load...
TABLE II

Benchmark Between Proposed Technique and Previously Reported Method

<table>
<thead>
<tr>
<th>a</th>
<th>b</th>
<th>c</th>
<th>Phase compensation</th>
<th>Proposed method</th>
<th>Increment</th>
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<td>-</td>
<td>60° 60° 4.59 10.9°</td>
<td>63.1° 4.59</td>
<td>5 60° 8.8° 49.4°</td>
</tr>
<tr>
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<td>-</td>
<td>60° 60° 4.37 23.42°</td>
<td>63.1° 4.37</td>
<td>5 60° 14.3% 36.58°</td>
</tr>
<tr>
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<td>1</td>
<td>-</td>
<td>- - - 60° 3.6 4</td>
<td>60° -** -**</td>
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<tr>
<td>5</td>
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<td>- - - - 60° 4</td>
<td>60° -* -**</td>
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<td>- - - - 73.9° 60°</td>
<td>60° -** -**</td>
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<td>- - - - 90° 3.6 4</td>
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<td>60° -** -**</td>
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<tr>
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<td>2</td>
<td>-</td>
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<td>90° 3.48 2</td>
<td>60° 15% 60°</td>
</tr>
<tr>
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<td>2</td>
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<td>60° -** -**</td>
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<td>79.4° 2.65 3</td>
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<td>60° 60° 1.73 0°</td>
<td>90° 1.73 2</td>
<td>60° 15% 60°</td>
</tr>
</tbody>
</table>

+ Can not be implemented.
** Can not be calculated.

Fig. 5. Phase-shift relationships between inverter and load variables under fault.

currents \( i_a, i_b, \) and \( i_c \), where the phase shift between the currents and the voltages \( \phi_o \) depends on the load characteristic. On the other hand, the phase shift between the inverter voltages and the load current will not only depend on the load characteristic but also on the phase shift between the inverter and load voltages \( \phi_a, \phi_b, \) and \( \phi_c \), according to

\[
\varphi_y = \angle(\vec{v}_y, \vec{v}_y) = \varphi_y - \phi_o, \quad y \in \{a, b, c\},
\]

Then, for each inverter, phase load can be seen as follows:
1) mainly resistive \( \varphi_y \approx 0° \);
2) mainly inductive \( \varphi_y < 0° \);
3) mainly capacitive \( \varphi_y > 0° \);
4) an active load \( 90° < \varphi_y < 270° \).

As previously explained, this last case is the most critical and must be avoided if diode-based rectifiers are used at the input of the cells; therefore, restrictions in the FPSC or load characteristics must be used. Note that the method proposed in Section III-A also applies an FPSC, and thus, the previously described phenomena affects it too.

To calculate the maximum load angle value that avoids the dc-link voltage increase \( \phi_o \) or the equivalent maximum inverter to load voltage phase shift, it is necessary to locate the inverter and load neutral points. By setting the origin at point \( c \), the coordinates for both neutral points are

\[
v_N = (x_N, y_N) = \left( \frac{V_{ll}}{2}, \frac{V_{ll}}{2} \sqrt{3} \right)
\]

\[
v_n = (x_n, y_n) = \left( \frac{V_c V_{ll}}{V_c - V_b \cos(\xi)}, \frac{V_c V_b}{V_{ll}} \sin(\xi) \right)
\]

\[
\xi = \begin{cases} 
\beta, & \beta < 180^\circ \\
360^\circ - \beta, & \beta \geq 180^\circ 
\end{cases}
\]

where \( V_{ll} = \|\vec{v}_{ab}\| = \|\vec{v}_{bc}\| = \|\vec{v}_{ca}\| \).

Then, the load to inverter phase shifts are

\[
\phi_a = \arcsin \left( \frac{V_{ll} - 2x_n}{2V_a} \right)
\]

\[
\phi_b = \arcsin \left( \frac{y_n}{V_b} \right) - 30^\circ
\]

\[
\phi_c = \arcsin \left( \frac{y_n}{V_c} \right) - 30^\circ
\]

Note that all the phase shifts are different and depend on the magnitudes of their respective inverter voltages.

By using (11), the maximum values for \( \hat{\phi}_o \) can be calculated for any fault. Table II shows the values for \( \hat{\phi}_o \) for each case, where the proposed method can be used. Note that, compared with FPSC, the proposed method not only lets a larger voltage be applied to the load but also a larger load angle can be used, increasing the operation range of the system and improving the availability of the system for all cases.

IV. RESULTS

The proposed compensation technique was tested in an 11-level 4-kW CM prototype shown in Fig. 6. This prototype is based on IR4GPC30 insulated-gate bipolar transistors, each one switching at 1 kHz. The overall converter is controlled by a TMS320C6713 DSP, which generates the references for the 15 cells, and an XC3S400 field-programmable gate array (FPGA), which handles all the peripherals required for the modulators.

The experimental results of the proposed fault correction strategy on the load voltage improvement and the load power
factor will be independently analyzed through the 5-3-2 and 5-4-1 faults, respectively. For each of the tests, the most relevant converter parameters are summarized in Table III.

### A. Load Voltage Improvement in 5-3-2 Fault

The electrical variables for the reconfiguration sequence in this case can be seen in Fig. 7. At up to $t = 40$ ms, the system operates in normal conditions. In Fig. 7(a), it is clearly seen that balanced 11-level voltages are generated at the inverter output, while, as can be seen in Fig. 7(c), balanced nominal currents are provided to the load. Fig. 7(d) shows that the common mode voltage through normal operation is only composed by high frequency commutations.

The fault occurs at $t = 40$ ms, when two cells on phase $a$ and three cells on phase $c$ fail and are instantly short circuited. In Fig. 7(a), the effect of this fault is shown, where phase $b$ now operates with seven levels while phase $c$ operates with only five levels. As, up to this moment, no compensation has been applied, line-to-line voltages become unbalanced [Fig. 7(b)], providing unbalanced currents to the load [Fig. 7(c)]. It is important to notice from Fig. 7(d) that, after the fault, the common mode voltage has a significant fundamental component.

As discussed in Section II-B, balanced line-to-line voltages, and, hence, load voltages, can be obtained by adjusting the phase angle between the inverter output voltages through Table I. This compensation is applied at $t = 120$ ms, obtaining balanced line-to-line voltages while inverter voltages are unbalanced, as shown in Fig. 7(a) and (b), respectively. The effect of the FPSC on the output currents can be seen in Fig. 7(c), where balanced currents are obtained with considerably less amplitude in relation to normal operation. An important drawback of this reconfiguration strategy is its effect on the common mode voltage. Fig. 7(c) shows that this voltage increases its fundamental amplitude dramatically to nearly 200 V, which can lead to unbearable stress on the machine bearings.

The compensation proposed in Section III-A is applied at $t = 200$ ms. A small increase in the line-to-line voltages can be seen in Fig. 7(b), which leads, as predicted by Table II, to an increase of the output current amplitude by $\approx 14.25\%$ in relation to the previous situation [Fig. 7(c)]. It can be noted from Fig. 7(d) that the proposed method reduces the fundamental amplitude of the common mode voltage, generating a more bearable operation condition for the load.

### B. Load Power Factor Effect in 5-4-1 Fault

To test the proposed method on the load power factor, the converter was tested under the 5-4-1 fault using the respective parameters shown in Table III. It should be noted that, under these conditions, the load presents an angle of $\phi_o \approx 40^\circ$, which is larger than the allowed load angle of $\phi_o = 10.9^\circ$ that can be driven using the method proposed in [20]. The results for this test are shown in Fig. 8.

Up to $t = 40$ ms, the converter operates under normal conditions, applying balanced 11-level voltages on its output [Fig. 8(a)] and, hence, balanced currents to the load [Fig. 8(b)]. As can be seen in Fig. 8(a), after $t = 40$ ms, one cell on output phase $b$ and four cells on output phase $c$ present internal faults and are short circuited immediately. Naturally, under this condition, output currents, shown in Fig. 8(b), become unbalanced.

The compensation through Table I is applied at $t = 120$ ms. As mentioned in Section III-B, due to the load and operation characteristics, after this compensation is applied, the remaining cell on phase $c$ receives energy from the output. The diode-based rectifier does not allow power to be taken from the dc link to the grid; thus, this energy is stored in the dc-link capacitor, increasing its voltage. This situation is shown after $t = 120$ ms in Fig. 8(c). It can be seen that the dc-link capacitor of the operating cell on phase $c$ increases its voltage by almost 50% in four fundamental cycles. If no actions are taken, the sustained operation under this condition will lead to the destruction of the operating cell in phase $c$.

At $t = 200$ ms, the fundamental phase angles and the amplitude of phase $a$ are changed to the proposed values shown in Table II. Under these conditions, the dc-link voltage of the operating cell on phase $c$ decreases dramatically, finally reaching its normal value. In addition, balanced and 8.8% higher output currents are provided to the load [see Fig. 8(b)], allowing the load to be continuously driven in these conditions.

### V. CONCLUSION

The modularity of the CM converter lets balanced currents be provided to the load even under faulty operation. In this paper, an enhancement to the FPSC fault correction strategy was proposed for the CM converter. Under certain fault conditions, the new strategy can increase the power supplied to the load. Moreover, the fundamental component of the common mode voltage is considerably reduced when applying the new reconfiguration strategy, creating a more bearable operation condition for the load.
In addition, the effect of both revised reconfiguration strategies on the load power factor was deeply studied. It was shown that, by using the existing reconfiguration technique on some particular faults, it is probable that the load will provide power to one or more output phases, increasing the voltage of their dc-link capacitors. On the other hand, by using the proposed
reconfiguration strategy, the load operating range is considerably increased, allowing to continuously provide balanced voltages to the load at all operating conditions.

All the previously mentioned features were validated through experimental results.

REFERENCES


