Design of a New mm-Wave Low Power LNA in 0.18 µm CMOS Technology

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Abstract: A new low power 33 GHz low noise amplifier (LNA) is proposed in a 0.18µm CMOS technology. It is composed of a single-stage cascode topology consisting of two Common-Gate (CG) amplifiers which provides gain requirements in high frequencies with very low power dissipation. The designed LNA achieves a power gain of 12 dB, IIP3 of -1dBm, and noise figure from 2.96-3.86 dB over the 3dB bandwidth from 30-36GHz frequency range. This LNA consumes 7.6 mW from a 1.8-V power supply.

Keywords: CMOS, low noise amplifier, millimeter wave (mm-Wave)

1. Introduction

The demand of larger bandwidth in communication systems motivates RF circuits to move towards higher frequencies. Pushing bipolar [1] and, preferably, CMOS technology to such speeds, designers must cope with broadband characterization of active and passive devices like CG amplifiers and transmission lines. For wideband applications, previously reported results were mostly fabricated in III–V or SiGe technologies to take advantage of the superior transistor characteristics. Lately, CMOS technology has also become an excellent candidate for wideband monolithic microwave integrated circuit (MMIC) amplifiers owing to the continuous scaling of device feature sizes [2, 3].

As expected, among the RF blocks the LNA is one of the most critical circuits since it is the first block receiving the desired signals. It must provide low noise figure (NF), high linearity, and enough gain over its 3dB bandwidth consuming low power which is challenging in millimeter wave frequencies because the gain and noise performance of LNAs strongly deteriorate as frequency increases. Although the device scaling gives good unity gain frequency and maximum frequency of oscillation, it makes some challenges such as lower supply voltage and linearity problems [4, 5].

In this paper, a new cascode structure is proposed for mm-Wave LNA in a 0.18µm CMOS technology. In this topology, proper usage of passive elements in matching networks helps to achieve sufficient gain consuming low power dissipation. The paper is organized as follows. In section 2, the design of amplifier is proposed. Simulation results are shown in section 3, and finally section 4 concludes the work.

2. Amplifier Design

In this section transistors biasing, matching networks, and noise reduction of LNA is discussed.

2.1 Amplifier Topology Selection

There are different topologies for LNAs such as multiple stage and cascade, which satisfy the low power requirement by reducing supply voltage [3, 6]. In these architectures, using cascode structure for LNA stages is preferred due to more compact elements and dissipating less power especially in mm-Wave frequencies [7].

On the other hand due to weakly dependency of CG stages to \((w_0/w_I)\) ratio in contrast to CS ones, it provides better low noise performance in larger bandwidth in high frequency design [8]. Regarding small degeneration and gate series inductances required for the input matching of a common source (CS) stage, CG amplifier is more suitable. However, the required 50-Ω input resistance translates specific transconductance \((gm)\) for CG transistor which limits noise reduction of the amplifier. It is worthy to say that in such high frequencies, power saving issues limit increasing the gs of transistors.

In this work, a new cascode LNA is proposed for mm-Wave applications, which is composed of two CG stages, providing high gain and better noise performance over a large bandwidth while dissipating low power.

2.2 Transistor Biasing and Matching Networks

The topology of LNA is shown in Fig. 1(a). Designing this circuit for mm-Wave applications needs some considerations on transistor biasing. It includes proper finger width and current density described by [2, 9]:

...
\[ J = \frac{I_{DS}}{W} \]  

Where \( J \) is the current density, \( I_{DS} \) denotes the drain current, and \( W \) is the transistor width. In this way, transistors are sized as reported in Table I according to the current density and transconductance.

As frequency increases, designing the matching networks gets more critical. So we should prevent the reflection and leakage especially in parasitic nodes of transistors to achieve enough gain. As shown in Fig. 1(b), the input impedance is expressed:

\[ Z_{in} = \left( \frac{sL_s}{sC_{gss1}} + \frac{1}{1 + g_{ms}r_{ds1}} \right) \]

where \( L_s \) is the source inductance, \( C_{gss} \) is the input capacitance while \( Z_L \) and \( r_{ds1} \) are output load impedance and drain-to-source resistance of \( M_1 \), respectively. Neglecting \( Z_L \) and \( r_{ds1} \) it can be written as

\[ Z_{in} = \left( \frac{sL_s}{sC_{gss1}} \right) \]

In ideal case, the inductor is designed to resonate with parasitic capacitance of \( M_1 \), i.e. \( C_{in} \), which provides a wideband matching for input port. It is worthy to say that gate-to-drain capacitance of \( M_1 \) deteriorates our matching which can slightly be improved with \( L_m \) in lower side of band. As discussed in [4] this simple equation has been used in many reported designs but in millimeter wave frequencies it is too approximated due to neglecting gate drain capacitance and load effects. It should be noted that having small degenerated inductance, considering bondwire effects, can deteriorate the performance of the LNA for these frequencies.

As can be seen in Fig. 1(b), the stage transconductance is slightly increased using capacitor \( C_j \) in the source of the transistor. The transconductance is:

\[ g_{ms} = \left( \frac{C_j + C_{gss1}}{C_j} \right) \times \frac{1}{R_j} \]

Considering the input matching, \( C_j \) should not be selected too small.

As shown in Fig. 2, in the second stage, \( L_m \) provides an inter-stage matching with \( C_{g2} \) which resonate as series LC circuit and enhances the input voltage of this stage expressed as,

\[ \frac{V_{in}}{Z_{in}} = \frac{Z_sZ_1}{Z_s + Z_{in} + Z_1} \times i_{M1} \]

Where \( Z_s \) is drain impedance of \( M_1 \), \( Z_1 \) is the source impedance of \( M_2 \), and \( Z_{in} \) refers to impedance of \( L_m \). Thus, the power gain of LNA is increased as illustrated in Fig. 3.

It should be noted that transmission lines give better performance for matching networks in millimeter wave applications.

2.3 Noise

Since the poor quality factor of passive networks and the noise of active elements and substrate, designing high performance LNAs is more difficult in millimeter wave applications. As a result, optimum topologies such as cascode architectures using less passive components with strict design are more feasible in high frequency circuits. Also, the transistor's noise can be decreased by narrow finger width and proper current density referred in section 2.2. Furthermore, gate-induced noise for CG topology is a weak function of \( \frac{V_G}{W/L} \) ratio compared to CS [8]. Therefore, the CS stage can be replaced by this stage as shown in Fig. 1(a).

In this paper, inter-stage matching network mentioned in section 2.2 reduces the noise of cascode transistor [7] as shown in Fig. 4. Neglecting drain-to-source resistance
and correlation between thermal noise and gate induced noise of transistor for simplicity, the LNA overall noise factor in resonance is

\[
F = 1 + \frac{\gamma}{4} + \frac{\delta}{5} \left( \frac{\omega_0}{\omega} \right)^2 + \frac{4\gamma}{\omega L_m} \left( \omega_0^2 + \omega^2 R_{L_m} \right) + \frac{1}{\omega L_m} \left( \frac{Z_m(j\omega) + Z_i(j\omega)}{1 + \alpha^2} \right)^2
\]

(6)

Where \(\gamma, \alpha, \) and \(\delta\) are process dependant parameters [10]. \(w_0\) and \(w_T\) refer to center frequency of band and unity gain frequency of transistor, respectively while the second term in this equation shows the gate induced noise of transistor and the third term is thermal noise of input stage. As can be seen in Fig. 4, thermal noise is dominant noise of the interested band while the other slightly changes the noise figure.

![Graph showing NF vs Frequency for different LNA configurations](image)

**Fig. 4:** eliminating the noise of cascode stage by \(L_m\)

<table>
<thead>
<tr>
<th>Transistor</th>
<th>((W/L)_1)</th>
<th>((W/L)_2)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>((2^*25/0.18))</td>
<td>((2^*25/0.18))</td>
</tr>
<tr>
<td>Passive elements</td>
<td>(L_x)</td>
<td>(L_m)</td>
</tr>
<tr>
<td></td>
<td>0.2nH</td>
<td>0.6nH</td>
</tr>
</tbody>
</table>

**TABLE I: Device Dimension**

<table>
<thead>
<tr>
<th>Process Corner</th>
<th>(P_{dc}) (mW)</th>
<th>IIP3 (dBm)</th>
<th>NF (dB)</th>
<th>(S_{21}) (dB)</th>
<th>(S_{22}) (dB)</th>
<th>(S_{11}) (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF,-40(^\circ)</td>
<td>1.186</td>
<td>-3</td>
<td>2.65-3.49</td>
<td>&lt; -2</td>
<td>13.1</td>
<td>&lt; -9.5</td>
</tr>
<tr>
<td>TT,27(^\circ)</td>
<td>7.5</td>
<td>-1</td>
<td>2.96-3.86</td>
<td>&lt; -2</td>
<td>12</td>
<td>&lt; -11</td>
</tr>
<tr>
<td>SS,85(^\circ)</td>
<td>4.76</td>
<td>0</td>
<td>3.6-5</td>
<td>&lt; -2</td>
<td>10</td>
<td>&lt; -11</td>
</tr>
</tbody>
</table>

**TABLE II: LNA Performance on Process Corners**

**3. Simulation Results**

The proposed LNA shown in Fig. 1(a) is designed in a 0.18\(\mu\)m CMOS technology and simulated using Advanced Design System (ADS). Fig. 5 depicts the power gain, input and output return loss, and noise figure of mm-Wave LNA.

The circuit is simulated in three different process corners and the worst results over the 3dB bandwidth of the LNA are reported in Table II. The proposed LNA can be used in Zero-IF mm-Wave receivers with no need to image rejection filters so the output port can be directly connected to the mixer.

Also, two tone RF signals that carry -20dBm power were used to verify the linearity of the LNA over the 6GHz bandwidth. As shown in Fig. 6, the worst IIP3 of the circuit is -1dBm which takes place at the end of the band i.e. 36GHz.

This LNA consumes 7.6 mW power dissipation from a single 1.8V voltage supply. All of the circuit parameters are illustrated in Table I. To compare the proposed mm-Wave LNA with other reported LNA chips, we used the figure of merit, FOM, as

\[
FOM = \frac{G \times IIP3 \times f}{(F-1) \times P_{dc}}
\]

(7)

Where \(G\) is power gain, \(IIP3\) refers to 3\(^{rd}\) order intercept point, \(f\) is center frequency, \(F\) denotes the noise factor, and \(P_{dc}\) is the dc power consumption [11]. Table III summarizes the performance of designed LNA along with the results of previously published LNAs using standard 0.18\(\mu\)m CMOS technology. Due to the good FOM compared to the reported designs [12-14], the proposed LNA is expected to have a better performance in fabrication.

**4. Conclusion**

A high performance low power low noise amplifier is designed in a 0.18\(\mu\)m CMOS technology for Ka band. The LNA has single-stage cascode architecture which provides sufficient gain with low noise figure over its 6GHz bandwidth.
TABLE III: Comparison of mm-Wave LNA performance

<table>
<thead>
<tr>
<th>Ref.</th>
<th>3dB.BW, GHz</th>
<th>$S_{11}$ dB</th>
<th>Power mW</th>
<th>NF dB</th>
<th>Gain dB</th>
<th>IIP3 dBm</th>
<th>FOM(dB.GHz)</th>
<th>Technology year</th>
</tr>
</thead>
<tbody>
<tr>
<td>[12]</td>
<td>22-26</td>
<td>&lt; -5</td>
<td>14</td>
<td>4.5</td>
<td>13.1</td>
<td>0.54</td>
<td>16.4</td>
<td>0.18-µm 2005</td>
</tr>
<tr>
<td>[13]</td>
<td>-</td>
<td>&lt; -10</td>
<td>26.9</td>
<td>4.6</td>
<td>10.2</td>
<td>3</td>
<td>16.4</td>
<td>0.18-µm 2006</td>
</tr>
<tr>
<td>[14]</td>
<td>38-42</td>
<td>&lt; -11</td>
<td>36</td>
<td>7.5</td>
<td>15</td>
<td>-8</td>
<td>0.5</td>
<td>0.18-µm 2009</td>
</tr>
<tr>
<td>This work†</td>
<td>30-36</td>
<td>&lt; -11</td>
<td>7.6</td>
<td>2.96-3.86</td>
<td>12</td>
<td>-1</td>
<td>37.7</td>
<td>0.18-µm</td>
</tr>
</tbody>
</table>

† Simulation Results

The designed LNA gives a minimum NF of 2.96 dB in the whole 30-36GHz bandwidth. It also shows input return loss better than -10 dB, $S_{11}$ of 12 dB and IIP3 of -1dBm. The power consumption is only 7.6 mW from 1.8V power supply.

![Fig. 6: Simulated IIP3 at end of band i.e.36GHz.](image)

5. Acknowledgment

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References