A Novel Hybrid PLL Frequency Synthesizer Using Single Electron and MOS Transistors

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Abstract — This paper proposes a novel hybrid phase-locked loop (PLL) using single electron transistor (SET) and metal-oxide-semiconductor (MOS) transistor. A novel hybrid voltage controlled oscillator (VCO) and hybrid logic gates using SET and MOS transistors are used to construct the hybrid PLL. The hybrid VCO has several advantages: a wide frequency tuning range, low power dissipation and large load capability. We study the performances of the hybrid PLL circuit by HSPICE simulator. Simulation results demonstrate that the hybrid circuit could well operate as a PLL at room temperature. The power dissipation of the PLL circuit is lower than 10uW.

Index Terms — Phase-locked loops (PLL), Voltage controlled oscillator (VCO), hybrid, single electron transistor (SET), metal-oxide-semiconductor (MOS), SPICE

I. INTRODUCTION

One of the challenges in nanoelectronics is to develop information-processing systems utilizing quantum effects and nanodevices. The phase-locked loop (PLL) circuit is a very important functional device widely used in modern communication systems. As recent progress in fabrication technology has pushed the device dimension toward 10nm scale, how to realize low power and small area integrated PLL using novel nanodevices is an important issue.

Among various nanodevices, single electron devices are very promising for their small size and ultra low power consumption [1]. This paper proposes a novel hybrid phase-locked loop (PLL) using single electron transistor (SET) and metal-oxide-semiconductor (MOS) transistor. A novel hybrid voltage controlled oscillator (VCO) and hybrid logic gates using SET and MOS transistors are used to construct the hybrid PLL. The hybrid SET/MOS VCO circuit possesses the merits of both the SET devices and the MOS devices. Compared with pure single-electron based oscillators, the oscillation frequency of the circuit can be effectively tuned by the external control voltage, and the circuit processes good load capability and large signal swing. Compared with conventional MOS VCO, the circuit has a simple structure and the power dissipation is ultra low. All of critical components in PLL are implemented by the hybrid SET/MOS structure. The circuit could work under room temperature. Compared with conventional PLLs, the power dissipation of this circuit is very low.

The remainder of this paper is organized as follows. Section II describes the structure of the hybrid PLL circuit and the structure of its components. Section III presents the simulation methodology and results for the hybrid circuit. The simulation results demonstrate that the circuit can perform frequency synthesizer operation. Section IV concludes the paper.

II. SET/MOS HYBRID PLL CIRCUIT

Fig. 1 shows the schematic of the hybrid PLL which is similar to a conventional PLL. It consists of a hybrid phase-frequency detector (PFD), a charge pump (CP), a hybrid VCO, a low pass filter (LPF) and a counter-type frequency divider. The small drain-source current of the SET ensures the low power dissipation of the total circuit.

First we present the operating principle of the hybrid VCO. Fig. 2 shows the schematic of the proposed SET/MOS hybrid VCO circuit. The circuit consists of three delay units, an input control voltage terminal $V_{\text{in}}$, a bias voltage terminal $V_{\text{set}}$, an output voltage $V_{\text{out}}$ and a power supply $V_{\text{dd}}$. The hybrid VCO circuit is similar to the conventional MOS ring oscillator. It connects three delay units in series that form a ring. Each delay unit receives an input voltage signal from the previous unit and outputs a voltage signal to the input terminal of the next unit. If the
inverting voltage gain of the delay unit is large enough, the circuit can oscillate and its oscillation frequency depends on the total delay time of the delay unit. In the proposed VCO circuit, the delay time can be controlled by the voltage \( V_\text{ctrl} \). Therefore the circuit can perform the voltage-controlled oscillation well.

![Fig. 2. Schematic of the SET/MOS hybrid VCO circuit. The delay unit is enclosed by the dotted rectangle.](image)

The delay unit in the hybrid VCO circuit consists of a dual gate SET, a PMOS transistor as a constant current (CC) load and a NMOS transistor as a cascade device. Actually it is the SET/MOS literal circuit proposed by Inokawa et al. [2]. The operating principle of the delay unit is briefly described as below. The output current \( I_0 \) of the CC load is set to be at the middle point between the peak and the bottom values of the Coulomb oscillating drain-source current \( I_{\text{dsSET}} \) of the SET. When the input voltage is low, \( I_{\text{dsSET}} \) is very low and the output voltage of the inverter unit is high because the SET operates in nearly cut off region. When the input voltage gradually increases, \( I_{\text{dsSET}} \) gradually increases above \( I_0 \) and the output voltage sharply switches to low value. In order to ensure that the swing of the output voltage of the delay unit is consistent with the swing of its input voltage, the output swing of the inverter is designed to be \( e/2C_g \), which is half of the Coulomb oscillation period. Here \( C_g \) is the gate capacitance of the SET, \( e \) is the electron charge.

The gate voltage \( V_{\text{ctrl}} \) of the PMOS transistor is used to change the output current of the CC load and the delay time of each unit. The oscillation frequency \( f_{\text{osc}} \) of the circuit could be approximately given by

\[
f_{\text{osc}} = \frac{I_0}{N C_{\text{tot}} e / 2 C_g},
\]

where \( N \) is the number of the delay units, \( C_{\text{tot}} \) is the total load and parasitic capacitance between the output terminal and the ground. So with appropriate parameters, \( f_{\text{osc}} \) could be effectively controlled by \( V_{\text{ctrl}} \). The parameters of the circuit can be determined as follows. First we consider the parameters of the SET. To achieve a high oscillation frequency, the tunnel junction resistance \( R_s \) and \( R_d \) of the SET should be as low as possible. So we choose \( R_s = R_d = 90k \). The tunnel junction capacitance \( C_s \) and \( C_g \) is designed to be 0.16aF to ensure that the circuit could operate at room temperature. Because the output voltage swing of the delay unit is \( V_{\text{swing}} = e/2C_g \), in order to get large output voltage swing, we choose \( C_g \) to be 0.1aF, and the corresponding output voltage swing is 0.8V. The bias voltage \( V_{\text{gsset}} \) should be a little larger than \( V_{\text{dsset}} + V_{\text{th}} \), to keep the SET drain-source voltage of SET approximately constant and to make the output voltage swing large enough. Here \( V_{\text{dsset}} \) is the drain-source voltage of SET which is around 100mV, \( V_{\text{th}} \) is the threshold voltage of the NMOS transistor. The supply voltage \( V_{\text{dd}} \) should be larger than \( V_{\text{swing}} \), so we choose \( V_{\text{dd}} \) to be 1V.

![Fig. 3. (a) Under different configurations, this hybrid circuit could serve as AND/NAND/OR/NOR gates. (b) Schematic of an edge-triggered D-flip-flop using hybrid SET/MOS NOR gates.](image)

For other components of the PLL circuit, we could use hybrid logic gate to implement the hybrid PFD and hybrid divider. Fig. 3(a) shows the schematic of the parallel SET/MOS hybrid logic gate with two inputs. This circuit could be used as a configurable elementary logic gate for the hybrid PLL circuit. Although pure SET logic has ultra low power dissipation, for room temperature operation and driven capability a hybrid structure maybe more practical. The drain of the SET is connected to the NMOS gate and the drain of the NMOS is the output terminal of the unit. The SET has two input gates and one phase control gate. The drain output voltage of SET oscillates with the summation of the input voltages, \( V_{\text{in1}} \) and \( V_{\text{in2}} \). The phase control gate is connected to a fixed voltage \( V_b \) to adjust the phase of the output voltage. The NMOS transistor operates in its sub-threshold region so that the drain voltage \( V_{\text{dsset}} \) of the SET could be exponentially amplified [5]. With appropriate device parameters, under different \( V_b \) and load current \( I \), we can use this circuit to realize all basic logic functions. When both \( V_b \) and \( I \) are low, if both \( V_{\text{in1}} \) and \( V_{\text{in2}} \) are low, \( V_{\text{dsset}} \) is designed to be larger than the threshold voltage \( V_{\text{th}} \) of the NMOS transistor, so the output voltage \( V_{\text{out}} \) is low. If one of the
input voltages is high, \( V_{\text{dsSET}} \) will be smaller than \( V_{\text{TH}} \), so \( V_{\text{out}} \) goes high. This is the OR function. When \( V_b \) is high and \( I_b \) is low, the phase characteristic of the SET is shifted so that the circuit could realize the NOR function. When \( V_b \) is low and \( I_b \) is high, only when both \( V_{\text{in1}} \) and \( V_{\text{in2}} \) are high could \( V_{\text{dsSET}} \) be smaller than \( V_{\text{TH}} \), so this is the AND function. And when both \( V_b \) and \( I_b \) are high, the circuit realizes the NAND function. Fig. 3 (b) shows the schematic of an edge-triggered D flip-flop that consists of hybrid NOR gates.

Divider could be constructed directly using a series of hybrid D-flip-flops. However, simulation results show that the maximum operating frequency of the divider is limited to around 100MHz due to the small operating current and nonideal characteristic of the hybrid NOR gate. For higher frequency, we could also use conventional MOS dividers, but the width to length ratio of the MOS transistors should be small to ensure low power dissipation. We could also use the novel hybrid logic gates to implement hybrid PFD. The maximum operating frequency of the proposed PFD is around 5MHz, with a power dissipation of 800nW. However, single electron devices offer possibility for novel structures. For instance, the multilevel memory using single electron turnstile [6] could be directly used as a counter-type divider. We will discuss these structures elsewhere.

We used a conventional CP and a simple two-stage LPF for the PLL circuit. Because the hybrid VCO has a large voltage-frequency convert ratio, the charging current of the CP is designed to be around 300nA, so the power dissipation of the CP and LPF is less than 500nW.

### III. Simulation Method and Results

The proposed circuits are SET/MOS hybrid circuits, which is hard to simulate only by using the MOS circuit simulation method or the SET circuit simulation method. But if the capacitance of the interconnection node between SET and MOS devices in the hybrid circuit is large enough, the SET could be regarded as an independent element and we could use SPICE macro model to describe its behavior [7]. Therefore we use the compact SPICE macro model [7] to describe the behavior of the SET. We simulate the hybrid PLL circuit by SPICE. We used the MOS transistors with 90nm technology node and we used the Predictive Technology SPICE model of MOS transistor [8] to simulate the MOS transistors.

Fig. 4 shows the frequency tuning characteristic of the hybrid oscillator, which indicates that the oscillation frequency approximately increases linearly with \( I_0 \) as predicted. The oscillation frequency ranges from 300MHz to 500MHz with a center frequency of 400MHz. The voltage-frequency convert ratio \( K_{vco} \) is 2250MHz/V. Simulated duty cycle is very close to 50%. If we change the device parameters, the hybrid VCO could operate at different frequency ranges. The maximum oscillation frequency will get further advance with smaller MOS device geometry.

In the proposed circuit, \( I_0 \) is designed to be 100-250nA, so the overall power dissipation is very low. Simulation results show that, with a 1V voltage supply and a 400MHZ oscillation frequency, the power dissipation of the whole circuit is around 500nW, which is very low. This is because the output of each delay unit is connected to the small gate capacitance of SET and the total amount of the transferred charge during oscillation is small.

The phase noise of the SET/MOS hybrid VCO could be theoretically evaluated as follows. The single-sideband phase noise spectrum of a ring oscillator could be calculated by equations given in [3]. Because the noise current injected during a transition between two logic states of the inverter delay unit has the largest effect [3], we set the operating point of the hybrid circuit for phase noise calculation at the middle transition point. The noise power spectral densities could be divided into two parts: the intrinsic SET noise and the MOS noise. The calculated drain-source current noise spectral density of MOS is 4.54\(^{-26}\)A\(^2\)/Hz. We used steady master equation to calculate the intrinsic SET noise and make approximations for low frequency [4]. The current noise spectral density of the SET is 5.82\(^{-26}\)A\(^2\)/Hz. Fig. 5 shows the in-all phase noise of the hybrid VCO circuit between 100 KHz and 1 MHz offset from the 400MHz center frequency. At an offset
frequency of 1MHz, the phase noise is -73.0dBc/Hz. However, this relative poor noise performance is mainly caused by the small total capacitance of the circuit, not by the inherent characteristic of SET.

Fig. 5. The phase noise of the SET/MOS hybrid VCO at a central frequency of 400MHz.

IV. CONCLUSION

This paper proposed a novel PLL using SET and MOS transistors. The PLL circuit has a classical structure, consists of VCO, PFD, LPF and divider. First we developed a novel hybrid SET/MOS VCO circuit. The hybrid VCO has a wide frequency tuning range, low power dissipation and large load capability. The oscillation frequency of the VCO circuit can range from 300MHz to 500MHz. The power dissipation of the VCO is 500nW. The hybrid logic gates are then used to construct the PFD and the divider. We use a SPICE macro model to describe the behavior of SET and simulate the performances of the hybrid PLL circuit by HSPICE simulator. Simulation results demonstrate that the hybrid PLL can operate well at room temperature. The power dissipation of the whole PLL circuit is less than 10uW. Although there maybe some tradeoff between low power dissipation and low phase noise performance of the circuit, we believe this study demonstrated the potential application of single electron devices in future information processing applications.

REFERENCES