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Digital tanlock loop architecture with no delay

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This article proposes a new architecture for a digital tanlock loop which eliminates the time-delay block. The \( \pi/2 \) (rad) phase shift relationship between the two channels, which is generated by the delay block in the conventional time-delay digital tanlock loop (TDTL), is preserved using two quadrature sampling signals for the loop channels. The proposed system outperformed the original TDTL architecture, when both systems were tested with frequency shift keying input signal. The new system demonstrated better linearity and acquisition speed as well as improved noise performance compared with the original TDTL architecture. Furthermore, the removal of the time-delay block enables all processing to be digitally performed, which reduces the implementation complexity. Both the original TDTL and the new architecture without the delay block were modelled and simulated using MATLAB/Simulink. Implementation issues, including complexity and relation to simulation of both architectures, are also addressed.

Keywords: time-delay digital tanlock loop; no-delay digital tanlock loop; phase shifter; acquisition; locking range; jitters

1. Introduction

Phase-locked loops (PLLs) are widely used in communication systems for modulation, demodulation and synchronisation operations. For example, the receivers in modern wireless communication systems contain PLLs that perform carrier synchronisation and symbol timing recovery tasks (Guan-Chyun and Hung 1996; Gardner 2005; Best 2007). PLLs are also extensively used in microprocessors, digital signal processors and control systems (Fitz and Cramer 1995; Guan-Chyun and Hung 1996; Stephens 2001; Crawford 2007).

The basic block diagram of a conventional PLL is shown in Figure 1. In this feedback system, the phase detector (PD) block compares the phase of the input ‘reference’ signal \( (F_{ref}) \) with the phase of the output signal \( (F_N) \). The output of the PD is used to drive the voltage-controlled oscillator (VCO) block. When the system is in its locked state, the negative feedback adjusts the VCO output so as to maintain a small and constant phase difference between the PD input signals. When this is achieved, the PD input signals will have the same frequency. The optional divider block \( (\div N) \) can be used to generate a

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low-noise high-frequency signal that is required in some applications (Stephens 2001; Gardner 2005; Best 2007).

Early generations of PLLs were designed using a variety of analogue circuit techniques. However, due to some inherent drawbacks of analogue circuits such as component tolerance and with the emergence of digital integrated circuit technologies, the design of an all digital PLL (DPLL) became a reality.

The DPLL shown in Figure 2 is similar to the analogue PLL of Figure 1 except that the blocks are all digitally implemented. The digital phase detector (DPD) block is a phase-to-digital converter that senses the phase difference between input signal \( F_{\text{ref}} \) and the divided version \( F_N \) of the digital controlled oscillator (DCO) output signal \( F_{\text{DCO}} \). As stated earlier, the divider block is optional. The output of the DPD is digitally filtered by the digital loop filter and used to drive the DCO (Staszewski et al. 2005; Kratyuk, Hanumolu, Moon, and Maryaram 2007; McCune 2010).

The extensive literature on DPLLs has many architectures and implementation techniques for the block diagram of Figure 2. The various approaches depend upon the target application and the system implementation technology. A DPLL architecture that has a number of desirable attributes, which include linearity and insensitivity to variations in input signal power, is the time-delay digital lock loop (TDTL; Hussain, Boashash, Hassan-Ali, and Al-Araji 2001). The TDTL solved the practical implementation issues.

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**Figure 1.** Block diagram of a typical analogue PLL.

**Figure 2.** Block diagram of a typical DPLL.
that affected its predecessor, the digital tanlock loop (DTL), by replacing the Hilbert transformation (HT) block with a simple time-delay unit (Jae and Chong 1982). Essentially, the TDTL consists of two sample and hold blocks, a PD, a digital filter, a digitally controlled oscillator and a time-delay block. This mixed-signal system accepts an analogue signal at its input but digitally performs all the processing. This means that the system can be easily implemented in a digital or a mixed-signal process. However, the replacement of the HT by a time-delay unit led to a slight degradation in the linearity of the locking range characteristic (Al-Qutayri, Al-Araji, and Al-Moosa 2006; Al-Araji, Hussain, and Al-Qutayri 2006). A number of possible solutions have been proposed in the literature to overcome this problem including the use of a variable time-delay block (Al-Qutayri, Al-Araji, Al-Ali, and Anani 2009; Al-Araji, Al-Ali, Al-Qutayri, Anani, and Ponnapalli 2010; Al-Ali, Al-Araji, Anani, Al-Qutayri, and Ponnapalli 2010). This article proposes an improved TDTL architecture that overcomes the nonlinearity problem through the elimination of the time-delay block. This new no-delay DTL architecture is referred to as no-delay digital tanlock loop (NDTL). The NDTL system modifies the design of the DCO circuitry so that two sampling signals with $90^\circ$ phase shift are generated in order to maintain the quadrature relationship between the two channels of the system.

In this article, Section 2 presents the system architecture and analysis, while the noise analysis of the system is detailed in Section 3. The testing results are presented in Section 4. The circuit implementation complexity of the system is discussed in Section 5. Finally, the conclusions of this article are given in Section 6.

2. NDTL system architecture and analysis

2.1. NDTL architecture

The architecture of the proposed NDTL system is shown in Figure 3. The centre frequency of the DCO is set at twice the overall loop DCO (L-DCO) free-running frequency ($f_0$). The DCO signal is then used to drive the two counters whose outputs are used to sample the input signal $x(t)$. Since there is a phase shift of $90^\circ$ between the outputs of the counters, the quadrature relationship between the two sampling signals is preserved without the need for a phase-shifter in one of the channel’s arms.

2.2. NDTL analysis

Let the input signal to the loop be a sinusoid as given by Equation (1)

$$x(t) = A \sin(\omega_0 t + \theta(t))$$

where $A$ is the amplitude of the signal, $\omega_0$(rad/s) the free running frequency of the DCO and $\theta(t)$ the information-bearing phase in radians. Following a analysis similar to that described in Hussain et al. (2001), Al-Araji et al. (2006) and Al-Qutayri et al. (2006), there are two sampling intervals of the DCO between the sampling instants $t(k+1)$ and $t(k)$, which are given by

$$T_1(k) = T_0 - c(k - 1)$$

$$T_2(k) = T_0 - c(k - 1) + \frac{\pi/2}{\omega_0}$$
where \( T_0 = \frac{2\pi}{\omega_0} \) is the free-running period of the DCO and \( c(k - 1) \) the output of the digital filter at the previous sampling instant.

The total times up to the \( k \)th sampling instant for both sampling intervals can be defined as

\[
t_1(k) = \sum_{i=1}^{k} T(i) = kT_0 - \sum_{i=0}^{k-1} c(i) \tag{4}
\]

and

\[
t_2(k) = \sum_{i=1}^{k} T(i) = kT_0 - \sum_{i=0}^{k-1} c(i) + \frac{\pi/2}{\omega_0} \tag{5}
\]

The discretised signals generated by the samplers are

\[
x(k) = A \sin[\omega_0 t_1 + \theta(k)] \tag{6}
\]

\[
y(k) = A \sin[\omega_0 t_2 + \theta(k)] \tag{7}
\]

Substituting Equations (4) and (5) in Equations (6) and (7), respectively, yields

\[
x(k) = A \sin \left[ \theta(k) - \omega_0 \sum_{i=0}^{k-1} c(i) \right] \tag{8}
\]

\[
y(k) = A \sin \left[ \theta(k) - \omega_0 \sum_{i=0}^{k-1} c(i) \frac{\pi \omega_0}{2\omega} \right] = A \cos \left[ \theta(k) - \omega_0 \sum_{i=0}^{k-1} c(i) \right] \tag{9}
\]
The phase error between the input signal and the DCO is given by

$$\phi(k) = \theta(k) - \omega_0 \sum_{i=0}^{k-1} c(i)$$  \hspace{1cm} (10)

Therefore, both Equations (8) and (9) may be redefined as

$$x(k) = A \sin[\phi(k)]$$  \hspace{1cm} (11)

$$y(k) = A \cos[\phi(k)]$$  \hspace{1cm} (12)

When the signals $x(k)$ and $y(k)$ are applied to the PD, the generated error signal $e(k)$ between the two arms of the loop is

$$e(k) = f\left[\tan^{-1}\left(\sin\{\phi(k)\} / \cos\{\phi(k)\}\right)\right] = f\left[\tan^{-1}(\tan(\phi(k)))\right] = f(\phi(k))$$  \hspace{1cm} (13)

where $f(\gamma) = -\pi + (\gamma + \pi) \mod 2\pi$ and $\phi(k)$ is the phase error.

Consequently, the degradation in the linearity of the TDTL system caused by the time-delay unit is eliminated (Hussain et al. 2001; Al-Araji et al. 2006; Al-Qutayri et al. 2006).

Since $c(k) = D(z)e(k) = K_1 f[\phi(k)]$, where $D(z)$ is the loop filter transfer function and $K_1$ the loop gain, two system difference equations can be derived from Equations (4), (5) and (13), as follows

$$\phi_1(k+1) = \phi(k) - \omega D(z)e(k) + \Lambda_0$$  \hspace{1cm} (14)

$$\phi_2(k+1) = \phi(k) - \omega D(z)e(k) + \Lambda_0 + \frac{\Lambda_0}{4}$$  \hspace{1cm} (15)

From Equations (14) and (15), it can be shown that

$$\phi_2(k+1) = \phi_1(k+1) + \frac{\Lambda_0}{4} = \phi_1(k+1) + \frac{\pi}{2}\left(\frac{\omega - \omega_0}{\omega_0}\right)$$  \hspace{1cm} (16)

$$\phi_2(k+1) = \phi_1(k+1) + \frac{\pi}{2}\left(\frac{1-W}{W}\right)$$  \hspace{1cm} (17)

where $W = \frac{\omega}{\omega_0}$ and $\Lambda_0 = 2\pi\left(\frac{\omega - \omega_0}{\omega_0}\right)$.

From Equation (17), it is evident that apart from a phase shift of $\frac{\pi}{2}\text{ (rad)}$, Equations (14) and (15) are similar. Therefore, the sampling signal given by Equation (2) is used to follow the zero crossing of the incoming input signal whilst the shifted signal of Equation (3) samples the input signal with a phase shift of $90^\circ$. This maintains the quadrature relationship between the two channels without the need for a phase shifter for the purpose of locking. Therefore, the final difference equation is

$$\phi(k+1) = \phi(k) - \omega c(k) + \Lambda_0$$  \hspace{1cm} (18)

2.2.1. First-order locking range analysis

For the first-order loop

$$c(k) = D(z)e(k) = K_1 f[\phi(k)]$$  \hspace{1cm} (19)
Using Equations (1) and (3) and following a analysis similar to that described in Hussain et al. (2001), Al-Araji et al. (2006) and Al-Qutayri et al. (2006), the difference equation and the locking range, depicted in Figure 4, for the NDTL first-order system are given by Equations (20) and (21), respectively. The locking range of the first-order TDTL is also included in Figure 4 for comparison.

\[
\phi(k+1) = \phi(k) - K_1'\phi(k) + \Lambda_0
\]

(20)

\[
2|1 - W| < K_1 < 2W
\]

(21)

where \(\phi(k)\) is the phase error at the instant \(k\), \(\Lambda_0 = \frac{2\pi(\omega_0 - \omega_0)}{\omega_0}\), \(K_1' = \omega G_1\), \(G_1\) the loop filter coefficient, \(W = \frac{\omega_0}{\omega_0}\), and \(K_1 = WK_1'\).

2.2.2. Second-order locking range analysis

Using Equations (1) and (3), for the second-order loop that uses the first-order accumulation digital filter with transfer function \(D(z) = G_1 + G_2/(1 - z^{-1})\), the loop difference equation and the locking range, of Figure 5, are given by Equations (22) and (23). Figure 5 shows also the locking range of the second-order TDTL.

\[
\phi(k+2) = 2\phi(k+1) - rK_1'\phi(k+1) + K_1'e(k) - \phi(k)
\]

(22)

\[
0 < K_1 < \frac{4W}{1+r} \quad \text{and} \quad r > 1
\]

(23)

where \(r = 1 + G_1/G_2\), and \(G_1\) and \(G_2\) are the filter coefficients.
3. Noise analysis of the NDTL

The input signal is corrupted by an AWGN (additive white Gaussian noise) with a zero mean and two-sided power spectrum density of $G_{nw}(f) = \frac{n_0}{2}$. Therefore, the autocorrelation can be given by the inverse Fourier Transform of $G_{nw}(f)$ as $R(\tau) = \frac{n_0\delta(\tau)}{2}$ (Peebles 2000; Haykin 2008), where $\delta(\tau)$ represents the Dirac Delta function. As a result, $R(\tau) = 0$ for $\tau \neq 0$; so, any two different samples of this kind of noise are uncorrelated and for this reason they are statistically independent (Mehrotra 2002; Kandeepan 2009).

Since the NDTL has a discrete nature, the Chapman–Kolmogorov equation is used to study the statistical analysis of the phase-error process (Jae and Chong 1982; Hussain et al. 2001; Al-Araji et al. 2006). The noise $\eta(k)$’s are mutually independent at any $k$ instant. Therefore, the phase-error process $\phi(k)$ can be regarded as a first-order, discrete time and continuously variable Markov process, which is also governed by modulo $2\pi$. The variable Markov process states that the first-order Markov process depends only on the previous state. As a result with a given initial phase error $\phi(0)$, the probability density function (pdf) of $\phi(k)$ will satisfy the Chapman–Kolmogorov equation (Jae and Chong 1982; Hussain et al. 2001; Al-Araji et al. 2006).

Assuming that the sampled noise process $\{n(k)\}$ is a sequence of independent and identical disturbances ($iid$) Gaussian random variables with zero mean and a variance $\sigma_n^2$, the noise samples $\{\eta'(k)\}$ (sampled the shifted signal of Equation (3)) is also an $iid$ sequence with the same mean and variance.

Both inputs in Equations (11) and (12) are independent Gaussian random variables with the following statistical characteristics (Jae and Chong 1982)

$$E[x(k)] = A \sin(\phi(k))$$

$$E[y(k)] = A \cos(\phi(k))$$

$$\text{var}[x] = \text{var}[y] = \text{var}[n] = \text{var}[n'] = \sigma_n^2$$

Figure 5. Locking range of both second-order NDTL and TDTL.
where \( n' \) is of the noise that is sampled at 90° phase shifts, \( E[\ ] \) the expectation (mean) and \( \text{var}[\ ] \) the variance. Consequently, the joint pdf \( g(x, y) \) of the Gaussian random variables \( x \) and \( y \) is given by

\[
g(x, y) = \frac{1}{2\pi\sigma_n^2} \exp \left[ -\frac{1}{2\sigma_n^2} \left\{ (x - A \sin(\phi(k)))^2 + (y - A \cos(\phi(k)))^2 \right\} \right] \tag{27}
\]

As AGWN has a disturbance effect on both amplitude and phase, both \( x \) and \( y \) can be redefined as in Equations (28) and (29), respectively.

\[
x(k) = R_k \sin(e(k)) \tag{28}
\]

\[
y(k) = R_k \cos(e(k)) \tag{29}
\]

where both random variables \( R_k \) and \( e(k) \) have the following limits \( 0 < R_k < \infty \) and \(-\pi < e(k) < \pi \). The joint pdf of both random variables \( R_k \) and \( e(k) \) can be obtained from Equation (27) and the pdf \( p[e(k)] \) can be computed by integrating over the range from zero to infinity with respect to \( R_k \) to get

\[
p[e(k)] = \frac{1}{2\pi} \left[ \exp(-\alpha) + f(\alpha, k) \exp \left[ -\alpha \sin^2(e(k) - \phi(k)) \int_{-\infty}^{\phi(k)} \exp(-\omega^2/2) \, d\omega \right] \right] \tag{30}
\]

where \( \alpha = \frac{A^2}{2\sigma_n^2} \) is the signal-to-noise ratio (SNR) and \( f(\alpha, k) = \sqrt{2\alpha} \cos[e(k) - \phi(k)] \).

It is obvious that the peak of \( p[e(k)] \) occurs at \( e(k) = \phi(k) \) in the modulo 2\( \pi \) sense; \( e(k) \) is usually around \( f[e(k)] \) in the presence of noise, and therefore can be decomposed into the term \( f[e(k)] \) and the random variable \( \eta(k) \) as in Equation (31).

\[
e(k) = f[e(k)] + \eta(k) \tag{31}
\]

where \( n(k) \) lies in the interval \((-\pi - f[\phi(k)], \pi - f[\phi(k)])\).

Using Equations (30) and (31), the pdf of the random phase-error noise disturbance \( p[\eta(k)] \) can be expressed from as

\[
p(e) = \frac{1}{2\pi} \left[ \exp(-\alpha) + \frac{\sqrt{\alpha} \cos \eta}{\sqrt{\pi}} \exp\left[ -\alpha \frac{\sin^2 \eta}{2} \right] \right] + \text{erf}\left( \sqrt{2\alpha} \cos \eta \right) \tag{32}
\]

where

\[
\text{erf}[x] = \frac{1}{\sqrt{2\pi}} \int_{0}^{x} \exp(-\omega^2/2) \, d\omega
\]

### 3.1. Statistical behaviour of the first-order NDTL in AGWN

From Equation (20), the difference characteristic equation in the presence of noise of the first-order NDTL can be expressed as

\[
\phi(k + 1) = \phi(k) - k'_i f[\phi(k)] + \Delta_0 + k'_i \eta(k) \tag{33}
\]

The noise \( \eta(k) \)'s are mutually independent for different values of \( k \). Therefore, the phase-error process \( \phi(k) \) can be regarded as a first-order discrete time and continuously variable Markov process. The first-order Markov process depends only on the previous state; so with a given initial phase error \( \phi(0) \), the pdf of \( \phi(k) \) will satisfy Chapman–Kolmogorov equation (Jae and Chong 1982; Hussain et al. 2001; Al-Araji et al. 2006) in Equation (34).
\[ p_{k+1}(\phi | \phi_0) = \int_{-\infty}^{\infty} q_k(\phi | u)p_k(u | \phi_0)du \]  

(34)

where \( p_{k+1}(\phi | \phi_0) \) is the pdf of \( \phi(k) \) given an initial condition \( \phi(0) \) and \( q_k(\phi | u) \) the transition pdf of \( \phi(k+1) \) given \( \phi(k) \).

If \( \phi(k) \) is limited to \((-\pi, \pi)\), Equation (33) can be given by

\[ \phi(k + 1) = \phi(k) - K_0' \phi(k) + \Lambda_0 + K_0' \eta(k) \]  

(35)

By squaring both sides of Equation (35) and then taking the statistical expectation, the steady-state variance can be attained as follows (Jae and Chong 1982; Kandeepan 2009)

\[ \text{Var}[\phi_{ss}] = \frac{K_0'}{2 - K_0'} E[\eta^2] = \int_{-\pi}^{\pi} E[\phi_{ss}] p(\eta)d\eta \]  

(36)

3.2. Statistical behaviour of the second-order NDTL in AGWN

In the presence of noise and from Equation (22) the difference equation of the second-order NDTL is

\[ \phi(k + 1) = 2\phi(k + 1) - rK_1' e(k + 1) + K_1' e(k) - \phi(k) - rK_1' \eta(k + 1) + K_1' \eta(k) \]  

(37)

Equation (37) consists of two first-order difference equations that describe two Markov processes, which can be solved in a manner similar to the first-order DTL (Jae and Chong 1982).

The mean and variance are given by Equations (38) and (39), respectively.

\[ E[\phi_{ss}] = 0 \]  

(38)

\[ \text{Var}[\phi_{ss}] = \frac{2(r - 1) + K_1'(r + 1)}{4 - K_1'(r + 1)} E[\eta^2] \]  

(39)

4. Simulation results

The TDTL and the NDTL were modelled and subsequently simulated using MATLAB/Simulink. This enabled extensive performance evaluation of each architecture and subsequent comparison between them under the same input conditions. This section presents some of the extensive set of results used to compare NDTL and TDTL. The simulations were performed in both noisy and noise-free environments.

The performance of the first- and second-order NDTL systems was evaluated in comparison with that of the respective first- and second-order TDTL systems. The evaluation process included applying various sudden frequency steps and frequency shift keying (FSK) input signals. The sudden frequency changes, which are either less or higher than the DCO free running frequency, are indicated by a negative or a positive step, respectively. This test is usually used to evaluate the acquisition time required by the system to reach its steady state (Al-Araji et al. 2006).
Starting with frequency step test, in the noise-free environment, Figure 6 illustrates the response to positive frequency steps for both the NDTL and the TDTL, respectively. It can be seen that NDTL requires nearly one-third of the time needed by the TDTL to achieve locking state. This is reflected in the much reduced number of samples that the NDTL requires to reach steady state. Another way to express the same results is to use phase-plane plots which show the consecutive phase error samples $\phi(k)$ and $\phi(k+1)$ of both the NDTL and TDTL. The phase-plane plots, following the application of a positive step, for the first- and second-order NDTL and TDTL are depicted in Figures 7 and 8, respectively. The improvement in the acquisition time is more profound with the second-order topology compared with the first-order one. This is due to the fact that the loop filter of the second-order loop is triggered by double the L-DCO free running

Figure 6. (a) Positive frequency step input, (b) first-order NDTL and TDTL phase-error responses and (c) second-order NDTL and TDTL phase-error responses with a positive frequency step of 0.2.
frequency. This will improve the climbing mechanism of the accumulation filter to reach the steady state in half the time required by the TDTL.

The NDTL system was also tested with FSK input signal in noise-free environment and the results, for FSK demodulation, are shown in Figure 9. It is clear that the acquisition time of the NDTL is three times faster that of the TDTL. This is attributed to the fact that the NDTL uses a DCO with double free running frequency, i.e. shorter intervals between the zero crossing, which reduces both the phase error and acquisition time.

Another performance test was carried out under AWGN where both the first- and second-order NDTL were evaluated and compared with TDTL of the same order. Figure 10 shows the phase noise pdf for the first-order NDTL and TDTL for input SNR = 7 dB. The figure shows the pdf values for various input frequency steps. It is clear, from Figure 10 that the first-order NDTL has better performance than the TDTL when positive or negative frequency steps were applied. Furthermore, it is evident from Figure 10 that the NDTL margin of performance improvement increases with the increase in the input frequency step. This results from the additional phase error that the time-delay block in the TDTL brings to the system as the input signal frequency increases. Figure 11 shows the phase noise pdf for the second-order NDTL and TDTL systems for an input of SNR = 7 dB when applying various step inputs. It is clear that the NDTL system outperformed the TDTL especially for higher frequency steps.

![Figure 7. First-order phase planes of: (a) NDTL and (b) TDTL with a positive frequency step of 0.2.](image-url)
The final test is jitter performance, which is evaluated by comparing the difference in time of the zero crossing point between the original signal in noise-free environment and the NDTL output affected by the AWGN noise. Jitter values have a critical impact on many communication systems. The impact of noise on the jitter performance was tested and the results are illustrated in Figure 12, which indicates that the NDTL outperforms the TDTL as the SNR ratio decreases. For the second-order loop, the NDTL is slightly better than the TDTL.

5. TDTL and NDTL implementation

The viability of implementing the TDTL on a reconfigurable platform that uses an FPGA (field programmable gate array) was investigated in previous work (Al-Qutayri et al. 2006; Al-Araji, Al-Qutayri and Al-Humaidan 2008). It was demonstrated that the real-time performance of the TDTL closely resembles the simulation results achieved using the model developed for MATLAB/Simulink. The synthesis process of the prototype TDTL used a Xilinx System Generator to generate the necessary hardware description language for the device-optimised block-set from within Simulink. The structure of the reconfigurable first-order TDTL is shown in Figure 13 (Al-Qutayri et al. 2006).

Figure 8. Second-order phase planes of: (a) NDTL and (b) TDTL with a positive frequency step of 0.2.
In the FPGA implementation depicted in Figure 13, the system block that is relatively complex to implement is the arctan PD. This was implemented using the CORDIC algorithm, which can translate trigonometric functions into the necessary...
digital circuits (Gutierrez and Valls 2009). Overall the TDTL used a small part of the FPGA chip.

The focus of the research work described in this article is on the system architecture. The validity of the simulation model of the original TDTL was verified through comparison with physical implementation in the earlier work outlined above. Having said that, comparing the NDTL and the TDTL, it is possible to see that the modified DCO only requires two additional flip-flops which has a very small cost in terms of gate count. At the same time, the NDTL does not require the delay block which may need to be a true analogue block in some applications. Optimised implementation of the NDTL, as well as other TDTL architectures, in a practical system will depend on the overall system specifications and the target technology. For example, synthesis for full-custom or application specific integrated circuit implementation can result in more optimised circuitry compared with that for an FPGA.
Figure 12. Jitter performance for a range of SNR: (a) first order and (b) second order, frequency step of 0.1, and $K_1=1$.

Figure 13. Structure of the reconfigurable TDTL.
6. Conclusions
A DTL with no-time-delay unit (NDTL) has been proposed. The system uses two sampling frequencies with a phase shift of $\pi/2$ (rad) to preserve the quadrature sampling relationship between the two loop channels. This enhances the linearity of the PD characteristics of the TDTL. The system was evaluated in the presence as well as in the absence of noise. The acquisition performance was assessed, in a noise-free environment, by subjecting it to frequency steps that cause sudden changes in the DCO free running frequency. In addition, the acquisition performance was also evaluated using FSK input signal. The NDTL system performance showed a clear improvement in the acquisition time compared with the TDTL. The improvements in the results are even more pronounced with the second-order NDTL. The acquisition is shown to be three times faster with the new loop compared to the TDTL system.

By adding AWGN to the input signal, two performance evaluation tests were performed. They included the pdf and phase noise (jitter). Both tests indicated that the NDTL system outperformed the TDTL. For the pdf test, the first-order NDTL has better performance than the TDTL when positive or negative frequency steps were applied. The margin of improvement increases with the increase of the input frequency step. This results in additional phase error (i.e. non-linearity) that the time-delay block in the TDTL brings to the system as the input signal frequency increases. For the second-order systems, the NDTL system outperformed the TDTL especially for higher frequency steps. The impact of noise on the jitter performance shows that both first- and second-order NDTL systems have better jitter compared with TDTL. Further, the proposed NDTL system can be entirely implemented digitally, which reduces circuit complexity.

References


