W/Cu TSVs for 3D-LSI with Minimum Thermo-Mechanical Stress.

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Abstract - High density 3D-LSI with W-TSV for signal line and Cu-TSV for power/GND line, and Cu-TSV containing W stress absorbing layers were investigated for the induced thermo-mechanical stress in 3D-LSI Si die/wafer after wafer thinning and bonding using micro-Raman spectroscopic technique. Stress mapping analysis revealed that W-TSV has induced less thermo-mechanical stress in LSI Si, whereas the Cu-TSV has induced large amount of stress. Further, Cu-TSV with W stress absorbing layer showed much reduced residual thermo-mechanical stress as compared to the pure Cu-TSV, i.e for 6 µm diameter Cu-TSV with W layer showed < +100 MPa of tensile stress after heating at 400 °C, whereas the Cu-TSV without W layer revealed > -300 MPa of compressive stress after heating at 400 °C. This property can be readily employed to minimize the residual thermo-mechanical stress in the bonded high density 3D-LSI.

I. Introduction

By and large it has been recognized that three dimensional (3D) integration of various functional chips is one of the most promising techniques to meet the growing demand for the low-cost and high-performance large scale integrated circuit (LSI) system [1] 3D LSI has several advantages over 2D-LSI such as short wire length, low pin capacitance, high-speed operation, low power consumption, high feasibility for parallel processing, and low cost. Both through-silicon via (TSV) and metal microbumps are the two key elements in realizing the high performance 3D LSIs. Both Cu and W are most commonly used via-fill material, but they have different advantages and disadvantages with each other. Since Cu resistivity is very low (1.6 µΩ·cm) as compared to the resistivity of W (4.9 µΩ·cm) , Cu is more preferred than W. However, the Cu-TSV poses two bigger threats for the device performance (i) the co-efficient of thermal expansion (CTE) value of Cu is ~17×10⁻⁶/K nearly six times higher than the Si CTE, ~2.6×10⁻⁶/K. Such a large difference in CTE value exerts a large negative thermo-mechanical stress (compressive) followed by a positive stress (tensile) in the active Si at vicinity of TSV, when the whole die cools down to room temperature after bonding [2]. (ii) other deleterious role of Cu-TSV is the back-metal contamination that occurs during the wafer thinning and planarization. Since the contaminated Cu diffuses into the active region of the device from the ground surface during chip stacking, ultimately leads to deterioration in device performance [3].

Fig. 1: Schematic view of cross-sectional 3D-LSI containing Cu-TSVs with W stress absorber for P/G lines and W-TSVs for signal lines.
In this study we would like to address the issue of thermo-mechanical stress induced in the active Si by Cu-TSVs. In order to suppress the induced thermo-mechanical stress by Cu, we have sandwiched a layer of hard metals such as Ti, Ta or W between the via-fill metal and the barrier metal layers. It is expected that the sandwiched hard metal layer may either absorb or arrest the stress developed by the via-metal Cu. Since W can also be used as a via-metal, in this work we have used W as a stress absorber. The schematic diagram for the 3D-LSI is shown in fig. 1. In the figure, the Cu-TSV which will be used in the power/ground (P/G) line contains the stress-absorbing W layer. This W layer was formed during the fabrication of the W-TSVs for the in the signal line. We have fabricated two types of W-TSVs with fully-filled and partially-filled (annular) structures by time-modulated W chemical vapor deposition (CVD) process and investigated the residual thermo-mechanical stresses induced by each W-TSV in the vicinal silicon by micro-Raman spectroscopy ($\mu$RS).

II. Experimental details

(a) W/Cu-TSV formation

Shown in the flow-chart diagram of Fig. 2 is the process flow for the fabrication of W/Cu-TSV on the LSI wafer using W-chemical vapor deposition and Cu-electroplating techniques. The via holes with different size were fabricated into Si substrate by deep Si dry etching. After resist stripping, tetraethoxysilane (O$_2$-TEOS) CVD was deposited at 350 °C. Subsequently, tungsten silicide (WSix) layer was deposited on O$_2$-TEOS dielectric layer as an adhesion layer to W by CVD at 350 °C. Followed by W to the thickness of 0.9 to 1.5 µm was deposited into via holes by time-modulated W-CVD at 350 °C.[4,5]. Two types of W-TSVs with fully-filled and annular shape structures were formed simultaneously as shown in fig. 2. It is clear that we have obtained good coverage of dielectric and adhesion layer along all through the TSV wall and bottom. Over the partially filled TSV (fig. 2b), a barrier layer of Ta and the seed layer of Cu, 100 nm each was deposited via sputtering. Then, this has been set in to the Cu plating path to fill via. Cross sectional optical image for as obtained Cu-TSV with W stress absorbing layer is shown in fig.3.

(b) Evaluation of stress distribution using $\mu$RS

$\mu$RS is a versatile method to analyze the residual remnant strain/stress in the Si not only qualitatively, but also quantitatively. $\mu$R spectra were recorded in backscattering mode on a confocal microscope equipped with a CCD detector using Ar$^+$ 488 nm laser. The incident light was polarized along the width of the microbump. The laser light was focused on the Si surface through a 100X objective lens. The sample was moved on a XY-translation stage in steps of 0.5 µm and at each position a Raman spectrum of Si was recorded. A Lorentz function was fitted to the Si-Raman peaks in order to determine the peak frequency, $\omega$. In addition, one of the laser plasma lines was fitted because these lines are Rayleigh scattered and their frequency is independent of stress in the Si, and they were used as a reference. The laser spot size and spatial resolution were respectively 1µm and 0.4 cm$^{-1}$, and the laser energy was kept below 1.4 mW on the sample surface.

The relation between stress/strain in Si and the Raman frequency
is quite complex, since all the non-zero strain tensor components influence the position of the Raman peak. However, in most of the cases it is assumed as linear for stress determination. In the present case we have used \( \sigma (\text{MPa}) = -434 \times \Delta \omega \,(\text{cm}^{-1}) \) and \( \sigma_{xx} + \sigma_{yy} (\text{MPa}) = -434 \times \Delta \omega \,(\text{cm}^{-1}) \) respectively for uniaxial and biaxial stress in the (100) plane of Si.

### III. Results and Discussion

Shown in fig. 4 is the thermo-mechanical stress induced in 780 \( \mu \text{m} \) thick Si die by the 10 \( \mu \text{m} \) diameter Cu TSVs after cooled down to room temperature from the annealing temperature of 400 °C for 30 min. It is clear that large negative stress (compressive) is present in the vicinity of TSV, and relatively a small positive stress (tensile) is present far from the TSV. In our previous studies [2,6] it was found that regardless of the TSV size the compressive stress in the vicinity of TSV was always accompanied by tensile stress and then becomes stress free state for the TSV pitch values greater than two times the TSV-width. On contrary in the present study, where the pitch value is less than the twice the TSV-width or the TSV spacing is less than the size of TSV-width, we have observed only a negative stress all along the x and Y direction. It is due to the fact that the stress from adjacent TSVs were added up in x and y direction resulting into only compressive stress. Similar kind of compressive stress distribution along the was also observed for the LSI chip containing an array of TSVs with size and spacing values of 7 mm and 3 mm, respectively [6,7].

It is well known that the filled via metal produced negative and positive stresses in Si at the vicinity of TSV region after die cooling. By and large, this thermo-mechanical stress leads to chip cracking and device degradation, hence one has to design the TSV layout structure carefully. The thermo mechanical stress is generated by the difference in coefficient of CTE of via metal and the Si. The CTE of W is \( 4.5 \times 10^{-6} /\text{K} \), and it is higher than the CTE value of Si, \( 4.2 \times 10^{-6} /\text{K} \). Since there exists only a small CTE difference between Si and W, it is worthy to employ W-TSV for signal lines [8, 9].

Fig. 5 shows the \( \mu \text{RS} \) data obtained for the test chip with completely filled W-TSVs having diameter and pitch values of 3 \( \mu \text{m} \) and 6 \( \mu \text{m} \), respectively. We obtained a relatively large compressive stress value for the as-filled state. However, this large compressive value decreases with increase in the post annealing temperature and finally it reached a minimum stress values at the center of the via space region after annealing at 300 °C and beyond. This observation reveals that the as-grown W-CVD films released its internal stress at various anneal temperatures, and hence minimum induced stress in the via space region. From our previous data it is worth mentioning that the observed W-TSV induced stress values are much lower than the Cu-TSV induced stress values. It confirms that the smaller CTE difference between W and Si helps to reduce the remnant stress, which is highly suitable for signal line.

![Fig. 4: 2D-stress distribution in LSI die containing an array of Cu TSVs with 10 \( \mu \text{m} \) diameter.](image)

![Fig. 5: Line stress profile obtained for the fully filled W-TSV at various annealing temperatures.](image)

![Fig. 6: Line stress profile obtained for the Cu-TSV with W-stress absorbing layer.](image)
We have also attempted to reduce the thermo-mechanical stress in the Cu-TSVs region. By sandwiching a conformal layer of relatively hard material in between the dielectric and Cu (wherein the sandwiched material has smaller thermal mismatch with Si), one can either completely or partially suppress the propagation of induced stress by Cu-TSV (for P/G lines) into the active Si region. In this process, we used the as-formed partially filled W-TSVs formed during the W-TSV fabrication. What is shown in Fig. 6 is the line profile obtained over the P/G-Cu TSVs fabricated over the annular W-TSVs. The blue line represents the stress data obtained at the as-filled state and the yellow line corresponds to the stress profile data obtained after annealing at 400°C. It is worth to note that large compressive stress at the as-formed state was either cancelled or changed to tensile stress. It is primarily due to the absorbance of thermo-mechanical stress induced by the Cu by the relatively hard W. Therefore, it is possible to annihilate the stress induced by the Cu by appropriately managing the thickness of sandwiched W layer.

IV. Conclusions

In this work, we have successfully fabricated W-TSVs for signal lines and Cu-TSVs for P/G lines. μRS data revealed that Cu-TSVs for P/G lines exerts a large thermo-mechanical stress in the vicinity of TSV while the W-TSV for signal lines produces relatively less amount of thermo-mechanical stress in the stacked LSI. Cu-TSVs with W absorbing layer found to be highly useful to reduce the effect of Cu-TSV on active Si in the vicinity of Cu-TSVs.

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