Development of Via-Last 3D Integration Technologies
Using a New Temporary Adhesive System

T. Fukushima1,2, J. Bea1,2, M. Murugesan1,2, K.-W. Lee1,2, and M. Koyanagi1,2
1 New Industry Creation Hatchery Center, Tohoku Univ., Japan
2 Global Integration Initiative (GINTI), Tohoku Univ., Japan
E-mail: fukushima@bmi.niche.tohoku.ac.jp

Abstract—We develop new via-last backside-via 3D integration technologies using a unique temporary adhesive system in which visible-light laser is employed for wafer debonding from glass carriers. The advanced 3D and TSV researches are driven in order to fabricate Si interposers with high-density TSVs and highly integrated 3D hetero chips at Global INTEGRATION Initiative (GINTI) as a new system integration research center. High-TTV wafer thinning, notch-free backside via formation, and void-less bottom-up Cu electroplating are performed, and the resulting TSV daisy chains show good I-V characteristics.

Keywords—3D integration, TSV, Temporary bonding, Deep RIE, and Wafer thinning

I. INTRODUCTION

3D stacking with TSVs is an attractive system integration technology to dramatically increase signal processing speed and decrease power consumption of LSI without further scaling down device sizes. There are many options for 3D integration scenarios: via-first, via-middle, and via-last for TSV formation sequence. In the late 1980s, we have proposed wafer-to-wafer 3D integration technologies using vertical buried interconnections later called TSV's and implemented the pioneering fabrication of three-dimensionally staked device chips such as a 3D image sensor chip, a 3D shared memory, a 3D artificial retina chip, and a 3D microprocessor chip using via-first approaches [1]-[9]. In the recent 10 years, we have been addressing 3D integration researches including design/architecture/simulation, advanced chip-to-wafer 3D integration using self-assembly, reliability studies, and a wide variety of applications such as photonics, bio, and magnetics [10]-[45]. In this paper, we deal with via-last backside-via technologies that have great advantages on chip design and use of post BEOL processes. In addition, we introduce a new temporary adhesive system composed of two types of high-heat-resistant polymers to achieve thin chip/wafer transfer from carrier glass wafers to the corresponding target wafers.

II. FABRICATION PROCESSES

The fabrication processes for Si interposers was described in Fig. 1. First, the edge of 8- or 12-inch Si wafers having a plasma-TEOS oxide layer underneath Cu wirings were trimmed to give Si wafers with a little bit smaller diameter than the initial 8- or 12-inch wafers. Then, the smaller wafers were temporarily bonded to 8- or 12-inch support glass carriers with a high-heat-resistant temporary adhesive (A) that was easily debonded by using visible-light laser. A TGA curve of the temporary adhesive was shown in Fig.2, where 1% weight loss temperature was found to be 420°C. After temporary wafer bonding, the structure consisting of a thick Si wafer on a support glass carrier were thinned from the backside of the Si wafer by grinding and CMP processes until the Si wafer was reached to 50 μm in thickness. After plasma-TEOS oxide deposition and the following patterning of a photoresist (PMER P-CR1000°) layer, a SiO2/Si/SiO2 (1 μm/50 μm/1 μm) layer was etched by DRIE using Bosch process until the Cu wirings appear, resulting in deep Si vias with a diameter of 5, 10, or 15 μm. The subsequent process was the formation of TSV liners along the deep Si vias by plasma CVD. Then, the plasma-TEOS oxide deposited on the bottom of the deep Si vias were fully removed by selective DRIE that was able to remain the plasma-TEOS oxide on the surface of the deep Si vias. After that, Ti barrier and Cu seed layers were deposited by a sputtering method, followed by bottom-up Cu electroplating to give TSV completely filled with Cu. Next, the resulting Cu overburden was removed by etching to form a redistribution Cu layer as a backside wiring. Finally, the structure consisting the 50-μm-thick thin Si wafer, the first temporary adhesive (A), and the first support glass carrier was transferred to another 8- or 12-inch glass support wafer using the second temporary adhesive (B) and debonded from the former glass support carrier. After the first temporary adhesive (A) is cleaned off, electrical characteristics were measured.

III. FABRICATION RESULTS

Fig.3 shows the result of the edge trimming of Si wafer to be bonded to another glass support wafer. As seen from this figure, the target depth of 150 μm is precisely obtained. Fig.4 shows the photomicrographs of the edge of the wafer bonded with the glass wafer through the temporary adhesive. The two wafers are glued with the temporary adhesive without voids and running off the trimmed edge area of the Si wafer. Fig.5 shows thickness uniformity of the thinned wafer bonded on the glass wafer through the temporary adhesive. TTV resulted from grinding and CMP for the structure consisting of the thin Si wafer, the temporary adhesive, and the thick glass support carrier is within 1 μm, and the surface roughness is below Ra 0.1 nm. In our 3D research center “GINTI”, an i-line stepper with an alignment function using IR is installed to further increase alignment accuracies between photomasks and patterns formed on the top surface of Si wafers to be flipped and bonded to glass carries. As is seen from Fig.6, the high
alignment accuracies within 100 nm are obtained. After Bosch process, the SiO$_2$/Si/SiO$_2$ structure in the thinned Si wafer is successfully etched to give deep Si vias without notch and large scallop, as shown in Fig.7. After TSV liner deposition, the following SiO$_2$ etching on the via bottom shows excellent selectivity: the etch rate of the plasma-TEOS oxide formed on the bottom of the deep Si vias is approximately 30% lower than that formed on the surface of the vias, as shown in Table 1. The deep Si vias are completely filled with Cu without any void or seam. The thinned Si wafer having Cu wirings is temporarily and stably bonded during high-temperature and high-vacuum processes, and the Si wafer is successfully transferred again to the corresponding glass support wafer. Fig. 8 shows an SEM cross-sectional view of the resulting 40-μm-pitch TSV daisy chain. Fig. 9 shows I-V characteristics of the TSV daisy chain. From the data of the I-V curves obtained from the daisy chain with more than 5,000 TSVs, the TSV resistances including Cu wirings is approximately 18 mΩ/TSV that is sufficiently low for industrial use.

Fig.1 A process flow of via-last backside-via TSV formation.

Fig.2 TGA curve of a high-heat-resistant temporary adhesive.

Fig.3 Relationship between trimmed depth and target depth.

Fig.4 Photos of the edges of a Si wafer bonded on a glass.

Fig.5 TTV data of a thinned wafer after grinding and CMP.
Fig. 6 An IR image of Cu wirings and TSV mask patterns.

Fig. 7 SEM cross-section of 40-μm-pitch SiO₂/Si/SiO₂ vias.

Table 1 Oxide thicknesses and their etch rates after 1-min etch.

<table>
<thead>
<tr>
<th>Thickness of P-TEOS oxide in vias</th>
<th>50-μm-depth vias</th>
<th>10-μm-depth vias</th>
</tr>
</thead>
<tbody>
<tr>
<td>Viatop</td>
<td>1.22 μm</td>
<td>1.82 μm</td>
</tr>
<tr>
<td>Top sidewall</td>
<td>0.74 μm</td>
<td>0.90 μm</td>
</tr>
<tr>
<td>Bottom sidewall</td>
<td>0.32 μm</td>
<td>0.41 μm</td>
</tr>
<tr>
<td>Via bottom</td>
<td>0.15 μm</td>
<td>0.20 μm</td>
</tr>
<tr>
<td>Etch rate on via top</td>
<td>0.79 μm/μm/min</td>
<td>1.22 μm/μm/min</td>
</tr>
<tr>
<td>Etch rate on via bottom</td>
<td>0.53 μm/μm/min</td>
<td>0.74 μm/μm/min</td>
</tr>
</tbody>
</table>

Fig. 8 Cross-sectional view of a 40-μm-pitch TSV daisy chain.

Fig. 9 I-V curve for the 40-μm-pitch TSV daisy chain.

ACKNOWLEDGMENT

This work was performed in the Global INTEGRation Initiative (GINTI) at Tohoku University, Japan. We would like to acknowledge DISCO CORPORATION for supporting implementation of edge trimming and wafer thinning. We would like to acknowledge SPP Technologies Co., Ltd., for supporting implementation of SiO₂/Si/SiO₂ etching processes. We would like to acknowledge Tokyo Ohka Kogyo (TOK) Co., Ltd., for their material and temporary bonding supports. We would like to acknowledge DENSO CORPORATION and Tohoku MicroTec (T-Micro) Co., Ltd, for their valuable discussions.

REFERENCES

Bonding, and Interconnects Induced Local Strain/Stress in 3D-LSIs with Fine-
H. Kobayashi, T. Fukushima, T. Tanaka, and M. Koyanagi, “Wafer Thinning,
(2009), 531-534.
Integration Technology for System-on-Silicon (SOS)”, in IEDM Tech. Dig.,
T. Fukushima, T. Tanaka, and M. Koyanagi, “Surface-Tension-Driven Chip Self-Assembly with Load-Free Hydrogen Fluorides-Assisted Direct Bonding at Room Temperature for Three-


