Low-noise differential transimpedance amplifier structure based on capacitor cross-coupled $g_m$-boosting scheme

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Abstract

This paper presents a capacitor cross-coupled $g_m$-boosting scheme for differential implementation of common-gate transimpedance amplifier (CG-TIA). A differential transimpedance amplifiers (DTIA) is designed by this scheme using two modified floating-biased CG stage with improved low corner frequency. Despite conventional methods for single-ended to differential conversion that increase the power and the noise for the same gain, the new DTIA gives a higher gain and hence reduces the input-referred noise power. Design of the DTIA circuit using 0.13 $\mu$m CMOS technology illustrates near 1.7 dB improvement in the circuit sensitivity and 5.2 dB enhancement in transimpedance gain compared to its single-ended counterpart. Operation at very low frequencies and stable dc coupling to photodiode are other features of the proposed DTIA.

1. Introduction

In optical receivers, transimpedance amplifiers (TIA) are the most critical and noise-sensitive elements [1], as they act as the interface between the electronics and the optics. Compared to TIA with single-ended configuration, differential TIA is generally preferred because of providing better immunity to power supply and substrate noises. However, photodiodes (PD) produce a single-ended current and single-ended to differential conversion (SDC) methods generally increase power consumption, and degrade the noise performance [1,2].

In this paper, we develop a new method to obtain SDC in common-gate transimpedance amplifier (CG-TIA) by means of $g_m$-boosting principle. Theoretical foundations for gain, bandwidth and noise analysis are developed.

Rest of the paper is organized as follows. Section 2 summarizes the conventional SDC design methods. Section 3 describes the effectiveness of $g_m$-boosting technique for SDC design. Section 4 presents a new differential TIA structure and the circuit realization. In Section 5, we present the simulation results followed by discussions. Section 6 is dedicated concluding remarks. The paper includes three Appendices. Appendix A is devoted to noise analysis of the CG-TIA, while Appendices B and C cover the detailed analysis of transimpedance gain and noise of the differential TIA (DTIA), respectively.

2. Conventional SDC methods

A common approach for SDC in TIA circuits is using a differential pair at the output, which is implemented in three methods as described below. In the first method, a replica (dummy) circuit of the single-ended TIA can be integrated with the main one so as a differential signal would appear at the output [1,3], as shown in Fig. 1(a). This architecture suffers from several nonidealities: (i) the paths from input to the outputs of main and dummy TIA are not the same, leading to gain and phase discrepancy at the output, especially for high-frequency components of the signal [2]; (ii) the output signals are not fully differential and there would be an inherent dc offset (about half the output signal swing) between them, causing serious problems in choosing a decision threshold; (iii) if the circuit is dc coupled to the PD, the main TIA experiences photocurrent dc-level fluctuations, leading to instability in its dc-bias conditions which affects the dummy circuit too; (iv) a gain equal to that of single-ended one is achieved while the power consumption is doubled; and (v) the input-referred noise current of the circuit is $\sqrt{2}$ times that of single-ended one, degrading the sensitivity by 3 dB [1,2].

Fig. 1(b) depicts the second method for converting the output of a single-ended TIA to a differential signal. In this method, we extract the dc component of the output signal of the TIA by a...
RC low-pass filter. Then, this component is used along with the signal to feed the inputs of a differential pair. The output signal of the differential pair is free from offset. However, the filter requires a relatively large external capacitor due to its large time constant [2,4]. In addition, the variations in dc component of single-ended TIA output will leak to the differential output and may affects overall differential characteristics.

Fig. 1(c) illustrates the third method for SDC design. It uses an auto-dc-control circuit [5] to force the dc-output level of TIA to a fixed value, usually equal to the common mode voltage needed for subsequent circuitry. The output of the TIA and the dc-level drive a differential pair at the front-end of a limiting amplifier. The circuit complexity that offers extra power consumption is associated with this technique.

3. \( g_m \)-Boosting technique for SDC

The conventional CG configuration of TIA (CG-TIA) is shown in Fig. 2, where \( C_{in} \) includes PD parasitic capacitance and gate–source and source–bulk capacitances and \( C_{out} \) contains the input capacitance of the following stage plus gate–drain and drain–bulk capacitances. The transimpedance gain can be written as

\[
Z_I = \frac{g_m + g_{mb}}{g_m + g_{mb} + 1/R_S (1+S/\omega_{p,in})(1+S/\omega_{p,out})} \quad (1)
\]

where \( \omega_{p,in} = (g_m + g_{mb} + 1/R_S)c_{in} \) and \( \omega_{p,out} = 1/(R_0C_{out}) \) denote the input and output poles.

Neglecting channel-length modulation, input-referred noise current spectral density of the CG-TIA, as shown in (A.8), is approximately given by

\[
\omega_{n,in} \approx \frac{4kT}{R_S} + \frac{4kT/g_m + 1/R_0}{(g_m + g_{mb})^2} (\omega^2 C_{in}^2 + 1/R_0^2) \quad (2)
\]

where \( k \) is Boltzmann’s constant, \( T \) is the absolute temperature and \( \omega \) is the noise factor of the MOSFET.

By using \( g_m \)-boosting technique [6–9], illustrated in Fig. 3(a), the effective transconductance of the transistor is increased to \( g_{m,eff} = (1+A)g_m \), where \( A \) is the gain of the inverting amplifier connecting the source to gate. Note that \( g_m \)-boosted common-gate-low-noise amplifier (CG-LNA) exhibits lower noise figure than conventional CG-LNA. For instance, assuming an inverting amplifier without significant noise [7], the noise factor of \( g_m \)-boosted CG-LNA is \( F = 1 + \gamma/(A+1) \), while the noise factor of a conventional CG-LNA is \( F = 1 + \gamma/z \), where \( z = g_m/g_m \) [8].

Principle of a \( g_m \)-boosted CG-TIA is illustrated in Fig. 3(b). To identify how the \( g_m \)-boosting technique affects the system performance, consider transimpedance gain of the circuit

\[
Z_I = \frac{g_{m,eff} + g_{mb}}{g_{m,eff} + g_{mb} + 1/R_S (1+S/\omega_{p,in})(1+S/\omega_{p,out})} \quad (3)
\]

where \( \omega_{p,in} = (g_{m,eff} + g_{mb} + 1/R_S)c_{in} \) and \( \omega_{p,out} = 1/(R_0C_{out}) \). Comparing (3) with (2) for \( Z_I \) of a conventional CG-TIA, as given in (1), improvements in the dc gain and frequency response is apparent. For small values of \( R_S \), there is a considerable improvement in dc gain, while for larger values of \( R_S \), the improvement in frequency response would be more significant (considering that \( \omega_{p,in} \) is usually dominant pole).

Assuming the inverting amplification stage in Fig. 3(b) does not contribute significant noise and neglecting channel-length modulation, input-referred noise current spectral density of the circuit is

\[
\omega_{n,in} ^2 \approx \frac{4kT}{R_S^2} + \frac{4kT g_m + 1/R_0}{(g_{m,eff} + g_{mb})^2} (\omega^2 C_{in}^2 + 1/R_0^2) \quad (4)
\]

It is evident from (4) that the noise contributed by \( M_1 \) and \( R_0 \) to the input is reduced in \( g_m \)-boosted CG-TIA.

Implementing inverting amplifier in Fig. 3(a) as an active stage may introduce several design issues due to its noise contribution and power consumption. On the other hand, differential implementation of the \( g_m \)-boosting technique, as illustrated in Fig. 4(a), enables using positive gain stages, of course when input is a differential signal. Thus, it will be possible to utilize passive elements, such as capacitors for the specific case of \( |A| \approx 1 \), as the gain stage [6–8].

Even though, differential implementation of \( g_m \)-boosting technique usually is applied when input signal is also available in differential form, we will demonstrate that it is possible to utilize differential \( g_m \)-boosting technique in situations where input signal is in the single-ended form. Fig. 4(b) illustrates this idea, by a basic configuration of differential \( g_m \)-boosting technique as capacitor cross-coupling of two CG-TIA. Assuming \( C \) in Fig. 4(b) is sufficiently large compared to parasitic capacitances, \( v_{gs1} = -v_{gs2} \), where \( v_{gs1} \) and \( v_{gs2} \) represent the gate–source voltages of \( M_1 \) and \( M_2 \), respectively. Therefore, neglecting the
body effect and channel-length modulation, the drain current of $M_1$ and $M_2$ are related by $i_{d1} = -i_{d2}$. By assuming equal drain load, both the gain and the output noise per unit bandwidth are doubled compared to the conventional CG-TIA. As a result, the input-referred noise is reduced by $\sqrt{2}$, improving the circuit sensitivity by 3 dB. Note that in practice, this improvement may be lower because of the above-mentioned second-order effects. Furthermore, one should note that, the differential structure required for implementing the capacitor cross-coupling technique would not contribute to gain improvement since the input is single ended. Therefore, the above improvement is due to capacitor cross-coupling technique.

In optical receivers, dc coupling to PD is preferred to achieve near dc-extended frequency response. However, dc coupling deteriorates the whole system performance stability, since changing average optical power level at the input will change the dc level of produced photocurrent, significantly altering the dc-bias conditions of the circuit [10]. In Fig. 4(b), the left part of the circuit directly couples to the PD and faces such a problem. Hence, the dc level of signals at the output of the left part becomes unstable depending on the received optical signal, while the output of the right part remains unaffected. This problem causes many design issues for subsequent stages. A solution to this problem is floating biasing of CG-TIAs as shown in Fig. 5(a), where the dc-bias currents through $M_1$ is held constant by forming a floating current mirror with $M_0$, as described in [10]. In other words, dc part of the $i_{in}$ will be grounded through $R_s$, while its ac part will be directed toward $R_d$ of course when the gate of $M_1$ can be considered ac grounded by $C_B$ [10,11]. Fig. 5(b) exhibits the

![Fig. 2. Conventional CG-TIA.](image)

![Fig. 3. $g_m$-boosting scheme: (a) principle, (b) topology of $g_m$-boosted CG-TIA.](image)

![Fig. 4. (a) Differential implementation of $g_m$-boosting technique, (b) SDC by means of $g_m$-boosting technique.](image)
proposed differential TIA with its biasing circuitry. In this circuit, the cross-coupling capacitors also work as gate bypassing capacitor for floating biasing.

4. \(G_m\)-boosted differential TIA (DTIA)

Three factors affect the coupling efficiency in the circuit of Fig. 5(b): parasitic capacitors at the gates, \(C_p\); the impedance of gate biasing circuitry, \(R_g\); and the frequency of incoming signal, \(i_{in}\); as shown in Fig. 6 as an equivalent circuit for coupling mechanism by \(C_c\). The inverting amplification value, \(A\), in Fig. 5(b) is approximately given by

\[
A = \frac{v_{gs}}{i_{in}} = \left(1 + \frac{C_p}{C_c} + \frac{1}{R_g C_c^2}\right)^{-1}
\]

In order to have \(C_c\) working as a unity gain stage, the conditions \(C_c \gg C_p\) and \(\omega \gg 1/R_g C_c\) must be satisfied.

A wideband frequency response with a low cut-off frequency as close to dc as possible is needed for TIA circuits to operate free from baseline wander and intersymbol interference (ISI), and also to relax data coding requirement [10]. To achieve this by the architecture of Fig. 5(b) where coupling of signals takes place just for frequencies beyond \(1/R_g C_c\), we need a large \(R_g\). Called modified floating biasing, in Fig. 7(a) the resistor \(R_B\) is placed in series with gate to increase gate-biasing impedance [12]. In Fig. 7(b), \(R_B\) is implemented using a MOS transistor operating in subthreshold region [13].

Fig. 8 shows the modified version of the circuit of Fig. 5(b), obtained by capacitor cross-coupling of two modified floating-biased CG pairs. Although the floating biasing is only required for the left pair, it is used for the right pair to simply match the characteristics of the pairs.

Assuming \(g_{m1} = g_{m2} = g_m\) and \(g_{mb1} = g_{mb2} = g_{mb}\), and neglecting channel-length modulation, the drain current for \(M_1\) and \(M_2\) (\(i_{d1}\) and \(i_{d2}\)) can be obtained similar to (B.2) and (B.5), respectively:

\[
\frac{i_{d1}}{i_{in}} = \frac{-R_{S1}}{1 + (g_m + g_{mb})R_{S1}} \frac{g_m + g_{mb} + 2g_m g_{mb} R_{S2} + g_{mb}^2 R_{S2}}{1 + (g_m + g_{mb})R_{S2}}
\]

This relation reveals that the value of \(i_{d2}\) is less than the value of \(i_{d1}\). When the body effects in \(M_1\) and \(M_2\) are suppressed, \(g_{mb} = 0\) and \(i_{d1} = -i_{d2}\). However, this may bring some technological limitations in an n-well technology since the transistors should be placed in a p-well. An alternative way is to minimize \(R_{S2}\) in (8) as follows.
Assuming \( R_{D1} = R_{D2} = R_h \), the differential gain of the circuit, as shown in (B.8), becomes:

\[
Z_{T_{\text{DTIA}}} = \frac{g_{m2} (1 + g_{mb} R_{S2}) + (g_{m1} + g_{mb1}) (1 + g_{mb2} R_{S2}) R_{S1} R_0}{1 + (g_{m1} + g_{mb1}) R_{S1} (1 + g_{mb2} R_{S2})}
\]  

(9)

Ratio of the transimpedance gain of a DTIA to a conventional

\[
Z_{T_{\text{DTIA}}} = \frac{1 + g_{mb} R_{S2}}{1 + (g_{m2} + g_{mb2}) R_{S2}} + \frac{g_{m2}}{g_{m1} + g_{mb1}} \frac{1 + g_{mb} R_{S2}}{1 + (g_{m2} + g_{mb2}) R_{S2}}
\]  

(10)

According to (1) and (8)–(10), when \( R_{S2} = 0 \) and \( g_{m1} = g_{m2} = g_m \), we have:

\[
\begin{align*}
I_{d1} & = - \left( 1 + \frac{g_{mb}}{g_m} \right) I_{d2} \\
Z_{T_{\text{DTIA}}} & = \left( 1 + \frac{g_m}{g_m + g_{mb}} \right) Z_{T_{\text{CG-TIA}}} = \frac{2g_m + g_{mb}}{g_m + g_{mb} + 1} R_0
\end{align*}
\]  

(11)

Eq. (11) reveals that, eliminating \( R_{S2} \) is sufficient for obtaining a nearly doubled differential gain and the difference between the drain currents is small. Note that eliminating \( R_{S2} \) will result in negligible dc imbalance at the output due to biasing with current mirror.

Fig. 9 illustrates the circuit of Fig. 8 for \( R_{S2} = 0 \), where \( M_2 \) has a common-source configuration. The input-referred noise current spectral density of the circuit, as shown in (C.11), is approximated by:

\[
\frac{I_{n,m}}{I_{n,m}} \approx 4kT \left\{ R_{S1}^{-1} + \frac{g_m}{(2g_m + g_{mb})^2} \left[ \frac{g_m}{g_m + g_{mb}} \right]^2 + 1 \right\}
\]

\[
+ \frac{(g_m + g_{mb})^2 + (\omega C_{in}^2 + R_{S2}^{-2})}{(2g_m + g_{mb})^2} \times \left\{ \left( \frac{g_m}{g_m + g_{mb}} \right)^2 + 2 \right\} R_0^{-1} + \gamma g_m \}
\]

(12)

In deriving this equation the noise contributions of \( M_0 \) and \( M_3 \) are neglected, since they have smaller dimensions compared to \( M_1 \) and \( M_2 \) [10]. In addition, the total current noise per unit bandwidth generated by a subthreshold MOS transistor is proportional to its current [14]. Since this is small in transistors implementing \( R_n \), the noise contribution of these transistors can be neglected.

5. Simulation results

The circuits in Figs. 2 and 9 are simulated with Hspice(RF) in a 130 nm CMOS process, with threshold voltage of 0.326 and

\(-0.324 \text{V for nMOS and pMOS, respectively. The circuit parameters for simulation are given in Table 1. The performance plots for typical process parameters are shown in Figs. 10–14. A PD capacitance of 300 fF and a bondwire inductance of 500 pH have
been used for all simulations. Fig. 10 shows the dependency of the outputs $d$ levels to the $d$ content of the input photocurrent for CG-TIA and DTIA. While $V_{od-}$ remains unaffected, the slope of $V_{od+}$ is about one-eleventh comparing to the slope of $v_{out}$ in CG-TIA in response to a 0–500 mA variation in input dc level.

Fig. 11 shows the frequency response of the circuits for $C_C = 1 \, \text{pF}$. The value of $C_p$ is about 40 fF. The differential gain is 48.9 dB, which is boosted by a factor of 1.82. The transimpedance gain for the left pair is 43.7 dB, which is equal to that of the CG-TIA, while for the right pair is 42.1 dB. A $-3$ dB frequency of 10.04 and 10.12 GHz can be seen for DTIA and CG-TIA, respectively. Although one of the cross-coupling capacitors is directly connected to the input node, the high-frequency corner is slightly deteriorated, since an extremely high-value resistor follows this capacitor. Further, the parasitic capacitors add a negligible extra capacitive load to the input node.

The transient simulations for a 10-GB/s random bit pattern in Fig. 12 reveal a completely open eye for two different-level inputs with extinction ratio of $r_e = 5$. The input average current level is approximately 30 and 300 mA for Fig. 12(a) and (b), respectively. A small dc difference at differential outputs can be seen in the transient responses, which are due to both the dc content of input current and the drain current mismatches of $M_1$ and $M_2$.

The noise current spectral density of the DTIA is shown in Fig. 13. It is observed that the noise current spectral density slowly increases at high frequencies. According to (12), at high frequencies $\omega C_n$ increases, thus the noise contribution of $M_1$ and $M_2$ and load resistors, $R_n$, to the input will increase. Fig. 14 demonstrates the BER graphs of the CG-TIA and DTIA. The optical sensitivity for CG-TIA and DTIA is obtained as $-14.8$ and $-15.7 \, \text{dBm}$, respectively, using a PD responsivity of $0.9 \, \text{A/W}$ for a BER of $10^{-12}$ from following relation [15]:

$$P_{ave}(\text{dBm}) = 10 \log \left( \frac{i_n \text{SNR} r_e + 1}{2 \rho r_e - 1} \times 1000 \right)$$

Fig. 13. Noise-current spectral density of CG-TIA and DTIA.

One should note that it is possible to achieve a better gain and noise performance in expense of a high-power consumption. However, the sensitivity of $-15.7 \, \text{dBm}$ is sufficient for short haul applications, which requires $-12 \, \text{dBm}$, according to SONET OC192 standard. The DTIA is employed in a 10-GB/s optical receiver with limiting amplifier (LA) and clock-recovery circuit.
Table 2
Performance comparison of recent CMOS TIAs for 10-Gb/s operation

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<thead>
<tr>
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<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>Technology (nm)</td>
<td>120</td>
<td>250</td>
<td>180</td>
<td>130</td>
</tr>
<tr>
<td>Power consumption (mW)</td>
<td>3</td>
<td>1.6</td>
<td>34</td>
<td>0.69</td>
</tr>
<tr>
<td>Transimpedance gain</td>
<td>50 dBΩ</td>
<td>42.2 dBΩ</td>
<td>52 dBΩ</td>
<td>43.7 dBΩ</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>N/A</td>
<td>N/A</td>
<td>7.5 GHz</td>
<td>10.12 GHz</td>
</tr>
<tr>
<td>Optical sensitivity for BER = 10⁻¹² (dBm W)</td>
<td>-13.1</td>
<td>-13.6</td>
<td>-19</td>
<td>-14.8</td>
</tr>
<tr>
<td>Power consumption (mW)</td>
<td>N/A</td>
<td>N/A</td>
<td>2.8 μAmps</td>
<td>2.3 μAmps</td>
</tr>
<tr>
<td>Technology (nm)</td>
<td>120</td>
<td>250</td>
<td>180</td>
<td>130</td>
</tr>
<tr>
<td>Photodiode parasitic capacitance</td>
<td>N/A</td>
<td>N/A</td>
<td>340 ff</td>
<td>300 ff</td>
</tr>
<tr>
<td>RMS input noise</td>
<td>N/A</td>
<td>N/A</td>
<td>28 μAmps</td>
<td>23 μAmps</td>
</tr>
<tr>
<td>Technology (nm)</td>
<td>120</td>
<td>250</td>
<td>180</td>
<td>130</td>
</tr>
<tr>
<td>Power consumption (mW)</td>
<td>N/A</td>
<td>N/A</td>
<td>340 ff</td>
<td>300 ff</td>
</tr>
<tr>
<td>Transimpedance gain</td>
<td>50 dBΩ</td>
<td>42.2 dBΩ</td>
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</tr>
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</tr>
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<td>N/A</td>
<td>N/A</td>
<td>2.8 μAmps</td>
<td>2.3 μAmps</td>
</tr>
</tbody>
</table>

Fig. A1. High-frequency noise model of CG-TIA.

The optical sensitivity of the TIA followed by LA was reduced to 
−14.1 dBm W.

The performance parameters of CG-TIA and DTIA along with 
other recently published TIA data are given in Table 2. The power 
dissipation of DTIA is twice than that of CG-TIA, while its input
referred noise current is reduced by a factor of 0.82, which 
illustrates 1.7 dB improvement in the circuit sensitivity.

6. Conclusions

The capacitor cross-coupled g_{m}-boosted differential TIA is 
implemented using two modified floating-biased CG stage. This 
novel approach can advantageously replace other differential 
design methods regarding to its simplicity, higher gain and better 
sensitivity. Simulation results with HSpice(RF) show that, despite 
the conventional methods for SDC that doubles the power and 
the noise for the same gain, the new DTIA gives a higher gain and 
and hence reduces the input-referred noise power. Design of the DTIA 
circuit using 0.13 μm CMOS technology illustrates near 1.7 dB 
 improvement in the circuit sensitivity and 5.2 dB enhancement in 
transimpedance gain compared to its single-ended counterpart.

Acknowledgement

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Appendix A. Noise analysis of the CG-TIA

Fig. A1 shows the high-frequency small-signal noise model of 
CG-TIA. Since the noise current of R_S, denoted by I_{n,RS}, is directly 
added to the input, it is ignored in the analysis and finally will 
be added to the results. Neglecting channel-length modulation, we have

\[ V_S = (I_{n,M1} + g_m V_S + g_{mb} V_S)(C_{in} S + 1/R_S)^{-1} \]  \hfill (A.1)

\[ -V_S = [-V_{n, out}(C_{out} S + 1/R_D) + I_{n, RD}](C_{in} S + 1/R_S)^{-1} \] \hfill (A.2)

From (A.1) and (A.2), we have

\[ V_{n, out} = \frac{I_{n, RD}}{C_{out}^{2} + 1/R_D} + \left( C_{in} S + 1/R_S \right) I_{n, M1} \] \hfill (A.3)

The transimpedance gain of the CG-TIA given in (1) can be 
rewritten as

\[ T_Z = \frac{(g_m + g_{mb})}{(g_m + g_{mb} + C_{in} S + 1/R_S)(C_{out} S + 1/R_D)} \] \hfill (A.4)

Dividing (A.3) by (A.4) yields

\[ I_{n, in} = \frac{C_{ps} S + 1/R_S}{g_m + g_{mb}} \left( I_{n, M1} + I_{n, RD} \right) + I_{n, R0} \] \hfill (A.5)

By adding the noise of R_S to (A.5), we obtain

\[ I_{n, in} = C_{ps} S + 1/R_S \left( I_{n, M1} + I_{n, RD} \right) + I_{n, R0} + I_{n, RS} \] \hfill (A.6)

Assuming all noise sources are uncorrelated, the equivalent 
input noise current spectral density of the CG-TIA is given by

\[ \overline{I_{n, in}^2} = \frac{(\sigma^2 c_{in}^2 + 1/R_S^2)(g_m + g_{mb})^2}{(g_m + g_{mb})^2 + (\sigma^2 c_{in}^2 + 1/R_S^2)(g_m + g_{mb})^2} \] \hfill (A.7)

Substituting the equivalent thermal noise for each noise source, we get

\[ \overline{I_{n, in}^2} = \frac{4kT}{R_S} + \frac{4kT}{R_D} + \frac{4kT}{g_m + g_{mb}} \left( \sigma^2 c_{in}^2 + 1/R_S^2 \right) \] \hfill (A.8)

Appendix B. Transimpedance gain of the DTIA

Fig. B1 shows the main core of the DTIA, which is the circuit 
of Fig. 8 without its biasing circuitry. Due to capacitor cross-
coupling, V_{S1} ≈ V_{g2} and V_{S2} ≈ V_{g1}, where V_{S1} and V_{S1} are source and 
gate voltages of M_1 and V_{g2} and V_{g2} are source and gate voltages
of $M_2$, respectively. From the small-signal analysis of the circuit

$$v_{s1} = \frac{i_{in}}{R_{s1}} \left[ \frac{1}{(g_{m1} + g_{mb1})} \right] = \frac{R_{s1}}{1 + (g_{m1} + g_{mb1})} i_{in}$$  \hspace{1cm} (B.1)$$

since $v_{s2} \approx v_{s1}$, we have Eq. (7) as follows:

$$i_{d2} = \frac{g_{m2}}{1 + (g_{m2} + g_{mb2} R_{s2})} v_{s2} = \frac{g_{m2}}{1 + (g_{m1} + g_{mb1})} R_{s1} i_{in} \times \frac{1}{1 + (g_{m2} + g_{mb2}) R_{s2}}$$  \hspace{1cm} (B.2)$$

also

$$v_{s1} \approx v_{s2} = \frac{g_{m2} R_{s2}}{1 + (g_{m2} + g_{mb2} R_{s2})} v_{s2} = \frac{g_{m2} R_{s2}}{1 + (g_{m1} + g_{mb1})} R_{s1} i_{in} \times \frac{1}{1 + (g_{m2} + g_{mb2}) R_{s2}} \quad \text{(B.3)}$$

The drain current of $M_2$, $i_{d2}$, can be found as follows:

$$i_{d2} = -(g_{m1} + g_{mb}) v_{s1} + g_{m1} v_{s1} \quad \text{(B.4)}$$

substituting $v_{s1}$ and $v_{s1}$ from (B.1) and (B.3) into (B.4) yields

$$\frac{i_{d2}}{i_{in}} = -R_{s1} \times \left[ \frac{g_{m1} + g_{mb} R_{s2}}{1 + (g_{m2} + g_{mb}) R_{s2}} \right]$$  \hspace{1cm} (B.5)$$

Assuming $g_{m1} = g_{m2} = g_m$ and $g_{mb1} = g_{mb2} = g_{mb}$, we obtain

$$\frac{i_{d2}}{i_{in}} = -\frac{g_{m1} + g_{mb}}{1 + (g_{m1} + g_{mb}) R_{s2}} \quad \text{(B.6)}$$

The transimpedance gain of DTIA can be obtained as

$$Z_{I_{s}}|_{\text{DTIA}} = \frac{i_{d2} - i_{d1}}{i_{in}} R_{D0}$$  \hspace{1cm} (B.7)$$

substituting $i_{d1}$ and $i_{d2}$ from (B.5) and (B.2) into (B.7) yields

$$Z_{I_{s}}|_{\text{DTIA}} = \frac{g_{m2} (1 + g_{mb} R_{s2}) + (g_{m1} + g_{mb}) (1 + g_{mb} R_{s2})}{1 + (g_{m1} + g_{mb})} R_{s1} R_{s2} \quad \text{(B.8)}$$

The dc transimpedance gain of CG-TIA is given by

$$Z_{I_{s}}|_{\text{CG-TIA}} = \frac{g_{m1} + g_{mb}}{1 + (g_{m1} + g_{mb})} R_{s1} R_{D0}$$  \hspace{1cm} (B.9)$$

Dividing (B.8) by (B.9) yields

$$\frac{Z_{I_{s}}|_{\text{DTIA}}}{Z_{I_{s}}|_{\text{CG-TIA}}} = \frac{1 + g_{mb} R_{s2}}{1 + (g_{m2} + g_{mb}) R_{s2}} \times \frac{1 + g_{m1} + g_{mb}}{1 + (g_{m1} + g_{mb})} R_{s1} R_{s2}$$  \hspace{1cm} (B.10)$$

Appendix C. Noise analysis of the DTIA

Fig. C1 depicts the core of the DTIA, i.e. the circuit in Fig. 9, at high frequencies. $M_1$ has a CG configuration while $M_2$ is a common-source stage. The contribution in differential transimpedance gain is as follows:

$$T_{ZM1} = \frac{v_{od+}}{i_{in}} = \frac{(g_{m1} + g_{mb1})}{(g_{m1} + g_{mb1} + C_{in} S + 1/R_{D1})}$$  \hspace{1cm} (C.1)$$

$$T_{ZM2} = \frac{v_{od-}}{i_{in}} = \frac{-g_{m2}}{(g_{m1} + g_{mb1} + C_{in} S + 1/R_{D2})}$$  \hspace{1cm} (C.2)$$

where $C_{in}$ is the parasitic input capacitance and $C_{out1}$ and $C_{out2}$ are parasitic output capacitances at the drain of $M_1$ and $M_2$, respectively. Using (C.1) and (C.2) and assuming $g_{m1} = g_{m2} = g_m$, $C_{in} = g_{mb}$ and $R_{D1} = R_{D2} = R_D$, differential transimpedance gain is obtained by

$$V_{od} = \frac{i_{in}}{i_{in}} = \frac{(2g_m + g_{mb})}{(g_{m} + g_{mb} + C_{in} S + 1/R_{D})}$$  \hspace{1cm} (C.3)$$

From Appendix A, contribution of the left pair of the circuit (Fig. C1) at output noise is

$$V_{n,od+} = \frac{i_{n, R_D}}{C_{out} S + 1/R_{D}}$$  \hspace{1cm} (C.4)$$

$$+ \frac{(C_{in} S + 1/R_{D}) I_{n,M1}}{g_m}$$

Contribution of the right pair of the circuit at the output noise is

$$V_{n,od-} = \frac{1}{C_{out} S + 1/R_{D}} \left( I_{n, R_D} + I_{n, M_2} + g_{m} V_{n,od+} Z_{in} \right) \quad \text{(C.5)}$$

where $Z_{in}$ is the input impedance given by

$$Z_{in} = \frac{1}{g_m + g_{mb} + C_{in} S + 1/R_{D}}$$  \hspace{1cm} (C.6)$$

From (C.3)–(C.5), we have

$$V_{n,od} = V_{n,od+} + V_{n,od-} = \frac{(2i_{n, R_D} + I_{n,M1})}{C_{out} S + 1/R_{D}} R_D \left[ \frac{C_{in} S + 1/R_{D}}{g_m} \right] I_{n,M1}$$

$$+ \frac{(C_{in} S + 1/R_{D}) I_{n,M1}}{g_m + g_{mb} + C_{in} S + 1/R_{D}}$$  \hspace{1cm} (C.7)$$

Dividing (C.7) by (C.3) yields

$$I_{n,in} = \frac{g_m + g_{mb} + C_{in} S + 1/R_{D}}{2g_m + g_{mb}} \left( \frac{g_m}{g_m + g_{mb}} + 2 \right) I_{n,R_D} + I_{n,M1}$$

$$+ \left( \frac{g_m}{g_m + g_{mb}} + 1 \right) \left( \frac{C_{in} S + 1/R_{D}}{2g_m + g_{mb}} \right) I_{n,M1}$$  \hspace{1cm} (C.8)$$
Including the noise contribution from $R_s$, (C.8), becomes

\[
I_{n,\text{in}} = \frac{g_m + g_{mb} + C_{in}S + 1/R_s}{2g_m + g_{mb}} \left( \frac{g_m + g_{mb} + 2}{g_m + g_{mb}} \right) I_{n,R_0} + I_{n,M_2}
\]

\[
+ \left( \frac{g_m + g_{mb}}{2g_m + g_{mb}} + 1 \right) \left( \frac{C_{in}S + 1/R_s}{2g_m + g_{mb}} \right) I_{n,R_1} + I_{n,M_1}
\]

\[= \text{ } (C.9)\]

Assuming all noise sources are uncorrelated, the equivalent input noise current spectral density of the DTIA becomes

\[
\frac{I_{n,\text{in}}^2}{I_{n,\text{in}}^2} \approx \left( \frac{R_s^{-1} + 78s}{2g_m + g_{mb}} \right) \left( \frac{g_m + g_{mb}}{g_m + g_{mb}} \right)^2 + 1
\]

\[
+ \left( \frac{g_m + g_{mb}}{2g_m + g_{mb}} \right)^2 \left( \frac{C_{in}S + 1/R_s}{2g_m + g_{mb}} \right)^2
\]

\[
\times \left\{ \left( \frac{g_m + g_{mb}}{g_m + g_{mb}} \right)^2 + 2 \right\} \frac{I_{n,R_0} + I_{n,M_2}}{g_m + g_{mb}}
\]

\[= \text{ } (C.10)\]

Substituting the equivalent thermal noise for each noise source, we get

\[
\frac{I_{n,\text{in}}^2}{I_{n,\text{in}}^2} \approx 4kT \left( \frac{R_s^{-1} + 78s}{2g_m + g_{mb}} \right) \left( \frac{g_m + g_{mb}}{g_m + g_{mb}} \right)^2 + 1
\]

\[
+ \left( \frac{g_m + g_{mb}}{2g_m + g_{mb}} \right)^2 \left( \frac{C_{in}S + 1/R_s}{2g_m + g_{mb}} \right)^2 \left( \frac{g_m + g_{mb}}{g_m + g_{mb}} \right)^2 + 2 \right\} \frac{R_s^{-1} + 78s}{g_m + g_{mb}}
\]

\[= \text{ } (C.11)\]

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