New RTD-Based General Threshold Gate Topologies and Application to Three-Input XOR Logic Gates

S. M. Mirhoseini, 1 M. J. Sharifi, 2 and D. Bahrepour 1

1 Science and Research Branch, Islamic Azad University, Tehran, Iran
2 Electrical and Computer Faculty, Shahid Beheshti University, Tehran, Iran

Correspondence should be addressed to M. J. Sharifi, m.j.sharifi@sbu.ac.ir

Received 4 August 2009; Accepted 10 November 2009

Academic Editor: Paul D. Franzon

Copyright © 2010 S. M. Mirhoseini et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

This paper presents two new general threshold gate (GTG) structures which are based on the monostable-bistable element (MOBILE) as their main part. These new GTGs eliminate an RTD from the structure compared to old structures and lead to less elements count and better performance in terms of power consumption, maximum frequency, and power-delay product (PDP). In the paper also two new single gate three-input XOR logic gates based on the old GTGs and two ones based on the new GTGs are presented and simulated in HSPICE simulator.

1. Introduction

One of the most promising nanoscale devices expected to augment CMOS technology in future is the resonant-tunneling diode (RTD) that is the most mature technology of quantum nanoelectronics [1]. RTDs are very fast nonlinear circuit elements which exhibit a negative differential resistance (NDR) region in their current-voltage characteristics, because of these features it uses in different applications [2, 3]. The most important topologies, among all RTD based topologies, are those that use the monostable-bistable logic element (MOBILE) as their main part. The MOBILE consists of two RTDs connected in series, driven by a switching bias voltage ($V_{bias}$) [1].

Threshold gate (TG) topology [1], multithreshold threshold gate (MTTG) topology [4], and more recently generalized threshold gate (GTG) topology [5–7] are three well-known topologies for implementing logic functions that are based on MOBILE.

Implementing three-input XOR function in a single gate structure by old MOBILE topologies, such as TG and MTTG, were not practical [4] and the presented three-input XOR gate in TG and MTTG topologies utilized cascading of two two-input XOR gates. Fewer element counts and operating in only one clock cycle are the advantages of single gate structures.

In this letter for the first time, to the best of author’s knowledge, two modified versions for general threshold gate (GTG) topology, which is the newest member of MOBILE based topologies, are presented in order to implement logic functions. Then we introduce two three-input XOR gates in single gate structure based on generic GTG and two other ones based on our new modified versions of GTG.

2. New GTG Structures and New XOR Gates

The new designs are based on GTG topology. The input-output relationship for a generic GTG is shown in (1) called general threshold function:

$$y = \text{sign}\left[ w_{11} f_1(x_1,\ldots,x_k) \cdots + w_{1n} f_n(x_1,\ldots,x_k) - w_{21} g_1(x_1,\ldots,x_k) \cdots - w_{2m} g_m(x_1,\ldots,x_k) - T \right],$$

(1)

where $T$ is the threshold, $w_{ij}$ ($i = 1,\ldots,n$) are positive weights, $w_{ij}$ ($j = 1,\ldots,m$) are negative weights, $y$ is the output, and $x_1 \cdots x_k$ are the boolean inputs. In this paper, following [6, 7], we utilize only $-2$ and $+2$ values for RTD weights and $-1$ and $+1$ values for the thresholds. Three different structures for GTG were introduced in 2005 and 2008 [5–7]. The work in [7] named these structures as
GTG-1, GTG-2, and GTG-3. The GTG-1 is an extension of TG topology in which, according to the above equation, f and g functions incorporate only AND boolean function [3]. In the GTG2, f and g functions may contains AND and/or OR boolean functions [6]. In the GTG-3 structure f function is equal to zero and g function implements the main boolean function with AND, OR, and NOT functions [7]. In other words, in GTG-3 structure, there is not any input branch in parallel with load RTD and the driver RTD has a parallel branch that implements the complement function.

In this letter we introduce two new GTG structures that are the modifications for GTG-2 and GTG-3 and therefore we call them GTG-4 and GTG-5, respectively. In the modified structures we focus on the weights, such that some weights are chosen to be infinity (see (1)). In other words, some RTDs are eliminated from the structure because RTDs with infinity area are actually equal to short circuits. In this letter we have also introduced two three-input XOR gates based on GTG-2 and GTG-3 and two others based on GTG-4 and GTG-5.

2.1. Designing Three-Input XOR Gates Based on GTG-2 and GTG-3. Equation (2) shows the boolean function for a three-input XOR gate. Equation (3) shows the implementation of (2) by general threshold function based on GTG-2. In the relations, ∨ and ∧ are the boolean OR and AND functions, respectively, and the – sign and + sign are arithmetic subtraction and addition functions, respectively. The sign is the sign function which is equal to 1 if its arguments are greater than or equal to zero and is equal to 0 if its arguments are negative:

\[ x_1 \oplus x_2 \oplus x_3 = (x_1 \land \overline{x_2} \land \overline{x_3}) \lor (\overline{x_1} \land x_2 \land \overline{x_3}) \lor (\overline{x_1} \land \overline{x_2} \land x_3), \]

\[ y = \text{sign} \left\{ [2(x_1 \land x_3) + 2(x_1 \lor x_2 \lor x_3)] \lor (x_1 \land x_2 \land x_3) \right\} - 1. \]

Figure 1(a) depicts the proposed three-input XOR gate based on GTG-2. The NDR0 implements the positive terms: \( [2(x_1 \land x_3) + 2(x_1 \lor x_2 \lor x_3)] \), NDR1 implements the negative term: \( [2(x_1 \land x_2) \lor (x_1 \land x_3) \lor (x_2 \land x_3)] \), and \( w_2A \) is used for adjusting the threshold value. For achieving XOR function the threshold value is equal to 1.
Equation (4) shows our general threshold function for three-input XOR gate based on GTG-3 and Figure 1(b) shows its implementation:

\[
    y = \text{sign}\{ -2 \left[ (\overline{x_1} \land x_2 \land x_3) \lor (\overline{x_1} \lor x_2 \lor x_3) \right. \\
    \left. \lor (x_1 \lor x_2 \lor x_3)] + 1 \right\}.
\]  

(4)

In Figure 1(b) the complement of the XOR function is implemented in NDR1 and \(w_1A\) is for adjusting the threshold value. For achieving XOR function the threshold value is equal to \(-1\).

2.2. Designing Three-Input XOR Gates Based on GTG-4 and GTG-5. As stated before, eliminating RTD(s) from GTG-based circuits would present new structures that we call them GTG-4 and GTG-5 which correspond to the modified GTG-2 and GTG-3, respectively (Figure 1). In this section, two new three-input XOR gates are presented. Considering (3) we realized that the coefficient of the \((x_1 \land x_2 \land x_3)\) term in (3) can be adjusted toward infinity without changing the output value. Note the brief explanation as follows.

Selecting any higher value for the coefficient of this term does not change the result of the mentioned function and this coefficient is the only one that has this feature. Hence, if the inputs adjust to (111), the output would be equal to 1. Meanwhile, in the implemented circuit the drive RTD should be switched [1]. While all the inputs are equal to 1, all the transistors are on; therefore the prerequisite for switching the drive RTD when all the inputs are equal to 1 is the correctness of the following relation (see Figure 1(a)) [1]:

\[
    (w_1A + w_2A + w_4A)(w_2A + w_3A).
\]  

(5)

That \(w_i\) is the coefficient for the boolean terms in (1) and also it adjusts the threshold value, \(A\) is a constant value and corresponds to the RTD fabrication technology (in the simulations \(A\) is adjusted to \(1 \mu m^2\)). By increasing the \(w_1\) toward the infinity (2) will remain correct; hence, the dotted RTD in the Figure 1(a) can be eliminated.

This method is repeated for (3) and the dotted RTD in the Figure 1(b) is removed resulting another implementation of three-input XOR gate.
Table 1: Comparison between single gates and cascaded gates of three-input XOR logic based on MOBILE structure. The results are normalized based on GTG-2 result except second column (PDP = (Power at Fmax)/Fmax).

<table>
<thead>
<tr>
<th>THREE-INPUT XOR TYPE</th>
<th>Device counts = RTD + Transistor</th>
<th>Fmax</th>
<th>PDP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cascaded GTG-3 [5]</td>
<td>25 (13 + 12)</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>GTG-2</td>
<td>17 (12 + 5)</td>
<td>0.66</td>
<td>0.85</td>
</tr>
<tr>
<td>GTG-3</td>
<td>21 (15 + 6)</td>
<td>1.33</td>
<td>0.35</td>
</tr>
<tr>
<td>GTG-4</td>
<td>16 (12 + 4)</td>
<td>0.92</td>
<td>0.53</td>
</tr>
<tr>
<td>GTG-5</td>
<td>20 (15 + 5)</td>
<td>1.71</td>
<td>0.26</td>
</tr>
</tbody>
</table>

For the MOBILE-based circuits the RTD areas should be adjusted to appropriate values for correct operation; moreover, the transistors width may be tuned for better performance [4–7]. In these designs, before and after removing the RTDs in both presented circuits, the transistors widths have been tuned in order to obtain better performance and fortunately; after eliminating RTDs, the modified transistors widths were less than before resulting another benefit from. In Figure 1 the transistors widths after modification are shown in parenthesis.

3. Simulation and Comparisons

Figure 2 shows the simulation results for four proposed XOR logic circuits. The simulations are done in HSPICE simulator. In all simulations LOCOM model for RTDs is used [4–7] and a 130 nm HSPICE transistor model is used to model transistors. For correct evaluation each output is loaded with four MOBILE inverters. The comparison between four proposed circuits in terms of device counts, maximum frequency, and power-delay product is shown in Table 1. In addition, we have simulated a different three-input XOR logic gate that consists of two cascaded two-input XOR gate based on GTG-3 that has been introduced before [7] for comparison. The used two-input GTG-3 XOR gate [7] was the best previously introduced gate, in terms of maximum frequency and PDP, and so the results that shown in Table 1 for maximum frequency and PDP are normalized based on results of this gate (the first row in the table).

The table shows that GTG-4 and GTG-5 designs have better performance in comparison with GTG-2 and GTG-3 in all aspects especially in PDP and all new designs have better performance in terms of device count.

4. Conclusion

In this paper we have introduced two modified structures for general threshold gate topology based on MOBILE. These two new structures eliminate RTDs and lead to lower power consumption, better speed, and PDP. Then we proposed two three-input XOR logic gates based on old GTG topologies and two based on new GTG topologies. Our designs also were compared with a different three-input XOR logic gate that consists of two cascaded, previously introduced, two-input XOR gates. The HSPICE simulation results showed that the three-input XOR based on GTG-5 is the best one according to maximum frequency and PDP and that one that is based on GTG-4 is the best in terms of device count.

References