A cross coupled low phase noise oscillator using an output swing enhancement technique

Mohammad Bagheri a,*, Ahmad Ghanaatian a, Adib Abrishamifar a, Mahmoud Kamarei b

a Department of Electrical Engineering, University of Science and Technology, Tehran, Iran
b Department of Electrical and Computer Engineering, University of Tehran, Tehran, Iran

ABSTRACT

A new voltage controlled oscillator (VCO) in a 0.18 μm CMOS process is offered in this paper. This paper’s argument is to provide an innovative approach to improve the phase noise which is one of the most controversial issues in VCOs. Contrary to most ideas that have been put forward to decrease phase noise which are based on higher current dissipation to increase output voltage swing, this new method offers better specifications with respect to traditional solutions. The presented circuit is capable of extra oscillation amplitude without increasing the current level, taking advantages of tail current elimination and topology optimization. Analysis of the presented peak voltage amplitude can verify the optimum performance of the proposed. Post-layout simulation results at 2.3 GHz with an offset frequency of 1 MHz and 3 MHz show a phase noise of about $-125 \text{ dBc/Hz}$ and $-136.5 \text{ dBc/Hz}$, respectively, with the current of 1.3 mA from 1.8 V supply. Also, Monte Carlo simulation is used to ensure the sensitivity of the proposed circuit to process and frequency variations are very promising.

1. Introduction

Local oscillators or crystals in traditional ways were often used for various applications which cannot meet nowadays dominant criteria, like low cost, small size, and low power consumption. As it seems impossible to put the frequency crystal on-chip, designing a crystal-less oscillator with an appropriate phase noise is attractive for future RF technology. Some different techniques have been used to overcome the inaccuracy issue of crystal-less oscillators. In order to achieve an acceptable phase noise performance in a VCO, some key factors such as temperature, supply voltage, and process variation should be considered. In 2009, Mcorquodale et al. [1] used a complementary structure for the oscillator. Using advantage of a feedback from a frequency divider, a novel compensator circuit, and a band gap reference circuit with the 2nd order temperature-coefficient compensation, Mcorquodale et al. [1] could achieve a brilliant phase noise as well as a jitter level just like crystal oscillators. With this innovating feedback and complex structure which improve the phase noise and jitter as well, high dissipating power and current are inevitable.

In theory, increasing quality factor can be mentioned as one of the effective ways to gain the proper phase noise in LC oscillators. But, the technology properties limit the improvement of Q in the tank [2–4]. Therefore, it could not be regarded as a certain way in all technologies. Another possible method to decrease the phase noise in crystal-less oscillators is eliminating the tail current as a main factor in the oscillators final phase noise [5]. Also, a capacitor and an inductor should be placed in the tail part of the circuit. These passive elements work as a filter of the 2nd tail current harmonic which mainly affects the output phase noise. However, these components will make the final circuit somewhere big in size. In 2011, Brown et al. [6] replaced the tail current source with a couple of inductors to omit the source of the phase noise in the output. A proper phase noise level was achieved with an extremely high dissipating current of around 6 mA from 0.5 V of supply.

It could be recognized that the most recent researches are derived from an innovative change in the Colpitts structure. Obviously, the Colpitts oscillation startup current is much larger than that of cross-coupled structures. Thus, most of works on the Colpitts structure could not present an impressive improvement from the side of dissipating power consumption. Consequently, Colpitts has smaller oscillation start up condition compared to the cross-coupled structures which present lower phase noise level as well as higher oscillating amplitude. In this paper, a cross-coupled...
circuitry is used as the rudimentary structure. In order to decrease the phase noise, two solutions based on amplitude enlargement are opted. First, a technique to enhance the signal amplitude after the cross-coupled transistors is used to boost the oscillating level. Second, a tail current source is eliminated to improve the phase noise level at the output. The rest of the paper is arranged as follows: Section 2 presents the mentioned technique. Complete circuitry and schematics are demonstrated in Section 3. Simulation and post-layout simulation results are placed in Section 4 and Section 5 concludes the paper finally.

2. Proposed architecture

Fig. 1(a) presents a cross-coupled structure in which the phase noise is relatively high due to the direct injection of the phase noise from the switching transistors into the tank. The main idea of this paper arises from Fig. 1(b) with a k-block above the cross-coupled transistors so that their phase noise can be rejected before injecting to the tank. Supposing that the phase noise of the mentioned block is not contributed to the circuit, it can be stated that the phase noise rejections as well as the oscillating amplitude enlargement are the benefits of this block. In addition, the dc voltage level can be increased by omitting the tail current source. As the tail current source directly acts as a noise source in the output, its elimination would be beneficial to the final phase noise level improvement, too. Fig. 1(c) presents the exact idea mentioned above.

3. Suggested circuitry

3.1. Suggested VCO circuitry

Fig. 2 presents the schematic of proposed VCO along with the bias circuitry. $M_1$ and $M_2$ are switching transistors. The amplifying stage, k-block, is replaced with $M_3$, $M_4$, $M_5$, $M_6$, $C_1$ and $C_2$. Large capacitance of $C_2$ can eliminate high frequency noise of the bias circuit. The circuit current is determined with $M_1$ and $M_2$ while their drain voltage is fixed with $M_5$ and $M_6$, respectively. So, the circuit current is controllable.

3.2. k-Block

Fig. 3 prepares a precise presentation of k-block. $C_1$, $C_2$ and assisting transistors ($M_3$ and $M_4$) can reduce the phase noise while increasing the swing level of the output voltage. The signal first meets the node M of switching transistor. As shown in Fig. 3, three paths of active and passive elements are now encountered. Active signal paths through $M_3$ (Common-Gate) and $M_5$ (Common-Drain) are a couple of those. The third path is through $C_1$ which prepares a direct way to the node M. Finally, the estimated output signal would be the summation of three signals with the same phase, resulting in an amplified output swing. Meanwhile, the large capacitance of $C_2$ will lead to a better filtering behavior in the circuit, but the oscillating frequency will be decreased. On the other hand, $C_2$ is not a good noise blocker if it has a small value. Therefore, its value is a challenge and should be optimized by the simulation. The role of $C_1$ in the circuit is blocking the injected noise of $M_3$ and $M_5$. Thus, the k-block can be considered low phase noise due to the enhanced final output and added noise filter ($C_1$).

In another analyze, it might be safe to say that the current noise of transistors will create the maximum phase noise when the output voltage crosses zero [7]. On the other hand, the k-block operates as an amplifier in this region and intensifies the signal amplitude. It means closing the signal angle to degree 90 around zero crossing region as shown in Fig. 4. Why this swing enhancement occurs is related to when the transistors enter the nonlinear

Fig. 1. Cross-coupled structure (a) with its noise sources, (b) with k-blocks, (c) without tail current source.

Fig. 2. Proposed VCO with its bias circuitry.

Fig. 3. k-Block circuitry.
region. The more the key transistor is near to their nonlinear region (the region between small signal trans-conductance and large signal one), the more swing will be achieved. Finally, it can be stated that the swing enhancement in the same current will improve the phase noise behavior.

3.3. Output voltage swing

In order to find the output voltage of the tank in Fig. 5, the large signal trans-conductance must be calculated [8]:

\[ G_m = \frac{2I_B}{V_{gs}} \]  

(1)

In (1), \( I_B \) is the bias current and \( V_{gs} \) is the gate-source voltage of the transistor. In order to find the voltage amplitude of the tank, the large signal model (half-circuit model) is predicted in Fig. 6 [7]. \( I_1, C_{in}, R_{tank}, C_{var}, R_\text{tankb}, \) and \( L \) are the amplitude of the first harmonic of drain current, the capacitance shown in Fig. 7, the impedance seen via the tank, the varactor of the tank, the series resistance of output inductance and the output inductance, respectively.

\( C_m \) can be found from Fig. 7. Where \( C_{1,T} \) and \( C_{2,T} \) are as follows:

\[ C_{2,T} = C_2 + C_{gr1} \]  

(2)

\[ C_{1,T} = C_1 + C_{gr6} \]  

(3)

\( C_{gr1} \) and \( C_{gr6} \) are negligible compared to \( C_1 \) and \( C_2 \). Thus (2) and (3) roughly can be simplified as

\[ C_{2,T} \approx C_2 \]  

(4)

Table 1

<table>
<thead>
<tr>
<th>Reference</th>
<th>Name</th>
<th>Output oscillation amplitude</th>
</tr>
</thead>
<tbody>
<tr>
<td>[9]</td>
<td>Cross-coupled</td>
<td>( \frac{2\pi}{\omega R_\text{ds}} )</td>
</tr>
<tr>
<td>[9]</td>
<td>DS-VCO</td>
<td>( \frac{4\pi}{\omega R_\text{ds}} )</td>
</tr>
<tr>
<td>[8]</td>
<td>Colpitts</td>
<td>( 4I_B R_{\text{tank}}(1-n) )</td>
</tr>
<tr>
<td>[10]</td>
<td>( G_m )-Boosted Differential G-S</td>
<td>( 4I_B R_{\text{tank}}(1-n) )</td>
</tr>
<tr>
<td>[11]</td>
<td>( G_m )-Boosted Differential D-S</td>
<td>( 4I_B R_{\text{tank}}[1-(1/2)] )</td>
</tr>
<tr>
<td>This work</td>
<td>Proposed VCO</td>
<td>( 4I_B R_{\text{tank}}[1-(1/2)] )</td>
</tr>
</tbody>
</table>

**Fig. 4.** A comparison between initial and boosted signal.

**Fig. 5.** Final schematic of proposed VCO without bias circuitry.

**Fig. 6.** Equivalent large signal model to find resonance amplitude signal.

**Fig. 7.** A circuit showing how to find \( C \).

**Fig. 8.** Suitable model to find \( R_x \).
Eventually, $C_{in}$ can be presented [7] as (6)

$$C_{in} = C_1/(C_1 + C_2)$$  \hspace{1cm} (6)

Fig. 8 is used to find $R_{in}$ [7], where $Z_1$ roles as an equivalent impedance at the source node of $M_6$. Considering Fig. 8, $i_1$ is approximately closed to zero and $R_x$ can be shown as

$$R_x = [(1/j\omega C_{gds}) + (1/j\omega C_{gds}/r_{o4})]/(1 + [G_{md}(1/j\omega C_{gd})/r_{o4}])$$  \hspace{1cm} (7)

For $r_{o4} \approx \infty$ (7) is simplified to (8):

$$R_x = [(1/j\omega C_{gds}) + (1/j\omega C_{gds})]/[G_{md}(1/j\omega C_{gd})]$$  \hspace{1cm} (8)

Obviously, $C_{gds} \approx C_{gd}$ and $R_x$ can be simplified to (9):

$$R_x \approx 2/G_{md}$$  \hspace{1cm} (9)

So, $R_{in}$ can be found as below [7]:

$$R_{in} = R_x/n^2$$  \hspace{1cm} (10)

where $n$ is $C_1/(C_1 + C_2)$. $V_{out}^+$ can be calculated:

$$V_{out}^+ = I_1[R_{tank}/(2/(n^2 G_{md}))]$$  \hspace{1cm} (11)

$G_{md}$ can be replaced by $I_1/(nV_{out}^+)$ [7], then (11) results to:

$$V_{out} = I_1 R_{tank}[1 - (n/2)]$$  \hspace{1cm} (12)
Finally, in the differential mode, the output signal amplitude can be shown as below:

\[ V_{out} = V_{out} - V_{out} = 4I_{B}R_{tank}[1 - (n/2)] \quad (13) \]

Table 1 is provided in order to compare some of the presented output amplitudes with (13). In [9], the output oscillation amplitudes of cross-coupled and double switch (DS) VCO were shown. The related structures are shown in Fig. 9. It is obvious that both structures have a lower output oscillation amplitude compared to the proposed VCO. Given that in the mentioned structures \( C_1 \) and \( C_2 \) are not used, factor \( n \) does not appear in their output oscillation amplitudes. As the noise of switching transistors is directly injected into the tank, both structures approximately have the same current and \( \frac{1}{C_0} \) factor is 7.5 and the output current is 1.3 mA. Fig. 12 shows the post-layout simulation result of the phase noise. As it is demonstrated, the phase noises at the offset frequency of 1 MHz and 3 MHz are \(-125 \text{ dBC/Hz}\) and \(-136.5 \text{ dBC/Hz}\), respectively. It could be stated that output voltage level increment can improve the phase noise behavior of the circuit [8]. Also, Fig. 13 shows the layout schematic of the proposed circuit.

A comparison among recently published CMOS-based VCOs is provided in Table 2. Also, a figure-of-merit (FoM) is considered as [6].

\[ \text{FoM} = 20 \log \left( \frac{f_o}{\Delta f} \right) - 10 \log (P_{DC}/1 \text{ mW}) + \frac{1}{2}\left| \Delta f \right| \quad (14) \]

where \( f_o \) is the resonance frequency, \( \Delta f \) is the offset frequency, \( P_{DC} \) is the power dissipation and \( l/\Delta f \) is the phase noise (dBC/Hz). Although the comparisons are presented in this table are the measurement results, the amplitude results have been obtained from simulation. It should be mentioned that the reported amplitude result of [11] is obtained from simulation using 1.8 V power supply.

To verify that the proposed VCO is promising through PVT variations, Table 3 is provided to show the post-layout simulation results. It is clear that FoM of the proposed VCO remains relatively constant throughout the PVT variations.

### 4. Simulation and post-layout simulation results

The proposed VCO is designed in 0.18 \( \mu \)m TSMC CMOS technology with 1.8 V power supply. Fig. 11 shows the simulation result of the output voltage swing in which the output signal peak to peak is about 4.7 V, the center frequency is 2.3 GHz, the tank quality factor is 7.5 and the output current is 1.3 mA. Fig. 12 shows the post-layout simulation result of the phase noise. As it is demonstrated, the phase noises at the offset frequency of 1 MHz and 3 MHz are \(-125 \text{ dBC/Hz}\) and \(-136.5 \text{ dBC/Hz}\), respectively. It could be stated that output voltage level increment can improve the phase noise behavior of the circuit [8]. Also, Fig. 13 shows the layout schematic of the proposed circuit.

A comparison among recently published CMOS-based VCOs is provided in Table 2. Also, a figure-of-merit (FoM) is considered as [6].

\[ \text{FoM} = 20 \log \left( \frac{f_o}{\Delta f} \right) - 10 \log (P_{DC}/1 \text{ mW}) + \frac{1}{2}\left| \Delta f \right| \quad (14) \]

where \( f_o \) is the resonance frequency, \( \Delta f \) is the offset frequency, \( P_{DC} \) is the power dissipation and \( l/\Delta f \) is the phase noise (dBC/Hz). Although the comparisons are presented in this table are the measurement results, the amplitude results have been obtained from simulation. It should be mentioned that the reported amplitude result of [11] is obtained from simulation using 1.8 V power supply.

To verify that the proposed VCO is promising through PVT variations, Table 3 is provided to show the post-layout simulation results. It is clear that FoM of the proposed VCO remains relatively constant throughout the PVT variations.

### 4.1. Monte Carlo simulation result

The transistors \( W, L \) and also process variation were examined taking advantage of Monte Carlo simulation. The results show that the proposed design is very promising and confirm the performance of the circuit. In 100 times of simulation, the phase noise variation is less than 1 dBC/Hz and the frequency variation is less than 290 kHz over the center frequency of 2.5 GHz. Fig. 14 depicts the mentioned simulation results.

![Fig. 13. The layout schematic of the proposed VCO.](image)

### Table 2

Comparison of proposed VCO with newly published counterparts.

<table>
<thead>
<tr>
<th>VCO</th>
<th>Frequency (GHz)</th>
<th>Supply (V)</th>
<th>( P_{DC} ) (mW)</th>
<th>Phase noise (dBC/Hz)</th>
<th>FoM (dBC/Hz)</th>
<th>Amplitude (V)</th>
<th>Process (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[11]</td>
<td>1.84</td>
<td>0.9</td>
<td>1.35</td>
<td>(-126@1 \text{ MHz})</td>
<td>(-190)</td>
<td>(= 2.6)</td>
<td>180</td>
</tr>
<tr>
<td>[12]</td>
<td>1.8</td>
<td>2</td>
<td>7.2</td>
<td>(-128@1 \text{ MHz})</td>
<td>184.5</td>
<td>N.A</td>
<td>180</td>
</tr>
<tr>
<td>[13]</td>
<td>1.8</td>
<td>1.4</td>
<td>15.8</td>
<td>(-145.5@3 \text{ MHz})</td>
<td>(-189.1)</td>
<td>N.A</td>
<td>180</td>
</tr>
<tr>
<td>[14]</td>
<td>4.84</td>
<td>1.2</td>
<td>3.4</td>
<td>(-123@1 \text{ MHz})</td>
<td>(-193)</td>
<td>(= 2.5)</td>
<td>180</td>
</tr>
<tr>
<td>[15]</td>
<td>(\approx 6)</td>
<td>1.8</td>
<td>(\approx 2.16)</td>
<td>(-123@2 \text{ MHz})</td>
<td>(-189)</td>
<td>0.9</td>
<td>180</td>
</tr>
<tr>
<td>[16]</td>
<td>3.1</td>
<td>1</td>
<td>1.57</td>
<td>(-123@1 \text{ MHz})</td>
<td>(-191.2)</td>
<td>N.A</td>
<td>180</td>
</tr>
<tr>
<td>[17]</td>
<td>3.4</td>
<td>1.2</td>
<td>6.6</td>
<td>(-147@10 \text{ MHz})</td>
<td>(-191)</td>
<td>(= 2)</td>
<td>90</td>
</tr>
<tr>
<td>[18]</td>
<td>1.96</td>
<td>1.8</td>
<td>14.4</td>
<td>(-118.5@1 \text{ MHz})</td>
<td>(-172.9)</td>
<td>N.A</td>
<td>180</td>
</tr>
<tr>
<td>[19]</td>
<td>13.15</td>
<td>0.75</td>
<td>2.4</td>
<td>(-101.4@1 \text{ MHz})</td>
<td>(-180)</td>
<td>(= 2.2)</td>
<td>180</td>
</tr>
<tr>
<td>This work</td>
<td>2.3</td>
<td>1.8</td>
<td>2.3</td>
<td>(-125@1 \text{ MHz})</td>
<td>(-189)</td>
<td>4.7</td>
<td>180</td>
</tr>
</tbody>
</table>

![Table 2](image)
Large signal analysis is used to prove the voltage swing amplitude without increasing the circuit current and power as mentioned is achieved through intensifying the output oscillating compared to the recently published counterparts. This improvement of this new structure is the improvement in output voltage swing behavior in conventional VCOs is presented. The dominant feature of the other works published recently.

5. Conclusion

In this paper a basic idea of how to improve the phase noise behavior in conventional VCOs is presented. The dominant feature of this new structure is the improvement in output voltage swing compared to the recently published counterparts. This improvement is achieved through intensifying the output oscillating amplitude without increasing the circuit current and power as well. Large signal analysis is used to prove the voltage swing enhancement. The post-layout simulation in 0.18 μm CMOS technology with oscillation frequency of 2.3 GHz, shows the offset frequency of 1 MHz and the phase noise of –125 dBc/Hz with the power supply of 1.8 V and a total current of 1.3 mA. Based on the mentioned results and the Monte Carlo simulation, the proposed idea shows a promising and improved performance compared to the other works published recently.

Table 3

<table>
<thead>
<tr>
<th>Process Corner</th>
<th>Frequency (GHz)</th>
<th>Current (mA)</th>
<th>Phase noise (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TT [27 °C]</td>
<td>2.3</td>
<td>1.3</td>
<td>–125.91 MHz</td>
</tr>
<tr>
<td>FF [–40 °C]</td>
<td>2.5</td>
<td>1.3</td>
<td>–126.291 MHz</td>
</tr>
<tr>
<td>SS [125 °C]</td>
<td>2.1</td>
<td>1.2</td>
<td>–123.41 MHz</td>
</tr>
</tbody>
</table>

Fig. 14. Monte Carlo simulation results (a) phase noise, (b) frequency variation.

References

[17] L. Fanori, P. Andreani, Highly efficient class-C CMOS VCOs, including a comparison with class-B VCOs, IEEE J. Solid State Circuits 48 (July (7)) (2013) 1730–1740.