Characterization of High $Q$ Transmission Line Structure for Advanced CMOS Processes

Ivan Chee Hong LAI $^{a}$, Student Member, Hideyuki TANIMOTO $^{†}$, Nonmember, and Minoru FUJISHIMA $^{†}$, $^{† †}$, Member

SUMMARY A new transmission line structure is presented in this work for advanced CMOS processes. This structure has a high quality factor and low attenuation. It allows slow-waves to propagate which results in low dispersion for a given characteristic impedance. It is also designed to satisfy the stringent density requirements of advanced CMOS processes. A model is developed to characterize this structure by analyzing the physical current flowing in the substrate and the shield structure. Test structures were fabricated using CMOS 90 nm process technology with measurements made up to 110 GHz using a transmission-reflection module on a network analyzer. The results correspond well to the proposed model.

key words: transmission line, slow-waves, quality-factor, attenuation, CMOS

1. Introduction

With the scaling of the CMOS to sub-100 nm nodes in recent years, silicon technology has become a possibility to operate at tens of gigahertz. $f_T$ and $f_{\text{max}}$ of the MOS transistor are now well beyond 100 GHz for advanced CMOS processes [1]. The possibility is further augmented by the need for low-cost electronics to work at the 60 GHz license-free band [2]. It is therefore necessary to develop high-performance devices and models to work under stringent process requirements. To effectively exploit CMOS at high frequency, transmission lines with high quality factor ($Q$-factor) are required. High $Q$ lines are characterized by a low attenuation that can reduce power consumption in a circuit. It is also desirable to have lines with high phase constant, $\beta$, to reduce the phase velocity of the waves in the lines. The resulting slow wave has low dispersion as described in [3]. An implementation of the slow-wave transmission line in the form of the coplanar waveguide has been reported [4] by using a floating shield. This method of reducing losses is very useful because it requires no additional processing steps. It is therefore useful to further develop new and better transmission line structures with slow-wave characteristics though layout innovations.

Currently, there are several issues that need to be addressed regarding on-chip transmission lines.

- Less lossy lines with superior performance at high frequency are required. Specifically, lines with high $Q$ for low loss, high $\beta$ for lower phase velocity of the wave, and high obtainable impedance for easy matching are required.
- Proper characterization is necessary for accurate circuit simulations. Accurate models that can explain the physical phenomenon of the structure are required. The attenuation, phase constant as well as characteristic impedance of the line should be correctly predicted.
- In advanced CMOS processes, stringent design rules require minimum metal densities and limited distances between planar metals. Therefore, the loop inductance of a coplanar waveguide (CPW) cannot be large, thus resulting in low impedance lines. This makes it difficult to use transmission line matching at high frequency.

We present a new slow-wave transmission line (SWTL) structure that satisfies the above requirements. The lines are fabricated using a six-metal 90 nm CMOS process. Figure 1 shows the basic structure of the transmission line. The features and physics of this structure are explained in detail in the following sections.

2. Slow-Wave Transmission Line (SWTL)

2.1 Structure

Figure 2 describes the structure which includes ground metals at both sides of the signal line. Each of the ground metal structure consists of extended metal fingers orthogonal to the direction of current flow and they are connected together.
Fig. 2 Structure of the slow-wave transmission line with the currents flowing through it.

Fig. 3 Simplified cross-section of the slow-wave transmission line. The electric field from the signal line will terminate at the side grounds and the bottom shield located 2.9 $\mu$m below it. No return current flows along these finger structures but will flow at a farther distance $w_g$ from the signal conductor at where the fingers join. In this way, the return ground current flows at a distance farther away in order to increase the inductance while satisfying the density rules. The typical density requirement for advanced CMOS processes is between 20% and 60% within the given size of a checking area, depending on the metal layer. This checking area is stepped through the layout. Hence, the required condition in the design of the finger structures is to fulfill these requirements by determining the most appropriate distance between the fingers and the signal line. This region will not contain any metal and will, therefore, reduce the total metal density of the checking area. The most stringent requirements can be considered with more than one CPW in the same checking area, which can be satisfied by the proposed method while maintaining proper characterization of the complete structure. In this structure, the effects of extended metal fingers can be considered as a minor reduction in the inductance of the signal lines due to eddy current in the fingers. However, due to the narrow width of each finger, the eddy current in the extended metal fingers is small and can be reasonably neglected.

The ground conductors extend towards the silicon substrate and are connected to a slotted ground shield laid underneath the signal conductor. The ground shield prevents the electric field from entering the substrate while its slotted structure minimizes return current from flowing thereby allowing $w_g$ to be the principal parameter to determine the inductance. Figure 4 demonstrates how the inductance, $L$, can be affected by $w_g$.

The proximity of the shield, further, reduces the distance of the signal line to ground potential and this result in a larger capacitance. The approximate lossless relationship between the phase velocity, $v_p$, and the unit inductance, $L$, and capacitance, $C$, is shown as

$$v_p = \frac{1}{\sqrt{LC}}.$$  

(1)

It can be deduced that a lower phase velocity can be achieved when the unit inductance and capacitance are high. In general, the propagation constant $\gamma$ is related to $L$ and $C$ by

$$\gamma = \alpha + j\beta = \sqrt{(G + j\omega C)(R + j\omega L)}.$$  

(2)

The real part of $\gamma$, $\alpha$ corresponds to the attenuation of the line, and the imaginary part, $\beta$ is the phase constant. $G$ and $R$ is the unit leakage conductance from signal to ground and the unit series resistance of the signal line respectively. Consequently, the extended metal fingers and slotted ground shields changes $\alpha$ and $\beta$. This is verified by the measurement results given in the next section.

2.2 Measurement of Fabricated Structures

Test structures are fabricated with line length, $l=900 \mu$m and different values of $w_g$. Large values of $w_g$ are included to characterize its effect on the performance of the SWTL. Table 1 summarizes the dimensions of the fabricated test structures. Table 2 list the dimensions of the common parameters.

$w_{\text{finger}}$ and $L_{\text{finger}}$ are the width and length of the metal


Table 1  Summary of dimensions of fabricated SWTL structures.

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<tbody>
<tr>
<td></td>
<td>$w_y$ [µm]</td>
<td>$s_{finger}$ [µm]</td>
<td>$L_{finger}$ [µm]</td>
<td>$s_{slot}$ [µm]</td>
</tr>
<tr>
<td>#1</td>
<td>14.0</td>
<td>4.0</td>
<td>0.0</td>
<td>8.125</td>
</tr>
<tr>
<td>#2</td>
<td>24.0</td>
<td>4.0</td>
<td>10.0</td>
<td>8.125</td>
</tr>
<tr>
<td>#3</td>
<td>34.0</td>
<td>4.0</td>
<td>20.0</td>
<td>8.125</td>
</tr>
<tr>
<td>#4</td>
<td>44.0</td>
<td>4.0</td>
<td>30.0</td>
<td>8.125</td>
</tr>
<tr>
<td>#5</td>
<td>84.0</td>
<td>4.0</td>
<td>70.0</td>
<td>8.125</td>
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</tbody>
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Table 2  Dimensions of other common parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tr>
<td>Signal conductor width, $w$</td>
<td>12.0µm</td>
</tr>
<tr>
<td>Signal conductor to finger distance</td>
<td>14.0µm</td>
</tr>
<tr>
<td>Signal conductor to shield distance</td>
<td>2.9µm</td>
</tr>
<tr>
<td>Shield metal thickness, $t_{metal}$</td>
<td>0.25µm</td>
</tr>
<tr>
<td>Shield slot spacing, $s_{slot}$</td>
<td>0.25µm</td>
</tr>
<tr>
<td>Shield slot width, $w_{slot}$</td>
<td>0.25µm</td>
</tr>
</tbody>
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Figure 5  Cross-section of the reference CPW structure.

Figure 6  Micrograph of the fabricated structure.

fingers at the top metal layers, $s_{finger}$ is the space between the fingers. For comparison, a coplanar waveguide (CPW) structure of Fig. 5 with signal-to-ground gap of 14 µm is also fabricated on the same chip.

For measurements, an Anritsu ME7808 vector network analyzer with Anritsu 3742A-EW Transmission-Reflection modules is used on an on-wafer probe station. The Transmission-Reflection modules extend the measurement frequency from 65 GHz to 110 GHz.

Figure 6 is a micrograph of a fabricated transmission line for $w_y=44$ µm. The lines are measured with G-S-G probes on the pads at the two ends of the lines and de-embedded. De-embedding employs the open-short-through method. From the de-embedded $S$-parameters obtained from measurements, Eqs. (3) and (4) are then used to obtain the propagation constant, $\gamma$ [5].

$$e^{-\gamma l} = \left\{ \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right\}^{-1},$$  \hspace{1cm} (3)

where

$$K = \left\{ \left( S_{11}^2 + S_{21}^2 + 1 \right) \right\} \frac{2S_{21}^2}{(2S_{21})^2},$$  \hspace{1cm} (4)

and $l$ is the length of the fabricated SWTL.

Figure 7 plots the measured values of $\alpha$ for three of the representative SWTL as well as the conventional CPW. The results show that lower attenuations are achieved for the SWTL when compared to the CPW. Up to 60 GHz, the attenuations of these lines are approximately only 50% of the reference CPW line. The higher attenuations of some lines at 65 GHz are a result of measurement errors due to employing the Transmission-Reflection modules at the switch-over frequency of 65 GHz.

Comparing the SWTL of different $w_y$, there is relatively small variations at low frequency. However, at high frequencies, lines with smaller $w_y$ perform significantly better with lower $\alpha$ with up to 20% reduction in attenuation at 100 GHz between the narrowest ($w_y=14$ µm) and the widest structure ($w_y=84$ µm). Lines with large $w_y$ have stronger magnetic field penetrating the substrate underneath the shield at high frequency that induces a current to flow. Further increasing $w_y$ results in attenuations which approaches that of a CPW. The high frequency effect of the signals on the CPW is manifested through the substrate parasitic as the signal line of the CPW is exposed to the silicon underneath. Some of the electric field lines terminates on the semi-conducting substrate and can induce a weak return current to flow.
Fig. 8  Imaginary ($\beta$) component of the propagation constant for structures of different $w_g$. $\beta$ is the phase constant of the lines. The plot for CPW is included for reference.

Fig. 9  Quality factors of the measured new transmission lines have higher values as compared to the $Q$-factor of the measured CPW fabricated under the same process conditions.

The plot of Fig. 8 shows that the slow-wave transmission lines have high phase constants $\beta$. The phase velocity of the wave is related to the phase constant by

$$v_p = \frac{\omega}{\beta}. \quad (5)$$

Slow-wave transmission lines have high $\beta$ that result in the lowest phase velocity. Figure 8 also shows that reducing $w_g$ will result in a value of $\beta$ closer to that of the CPW. This variation with $w_g$ is different from that of $\alpha$ as described earlier.

For transmission line resonators that are commonly used in filters, oscillators and tuned amplifiers, the resonant cavity $Q$ is derived [6] to be

$$Q = \frac{\beta}{2\alpha}. \quad (6)$$

This definition takes into account of the average energy stored, including both magnetic energy and electric energy. Figure 9 plots the values of $Q$ obtained using Eq. (6). From Fig. 9, the $Q$-factors of all the slow-wave transmission lines are higher than the conventional CPW. The definition of $Q$ in Eq. (6) can also be understood as the inverse relationship of the phase constant of attenuation per phase constant. In contrast to the attenuation per physical length, given simply by $\alpha$ as in Fig. 7, $Q$ describes the power loss in a given phase. Since the length of a transmission line is determined by the required number of wavelengths in a RF design, it is meaningful to consider the loss in a given phase. To understand the mechanism of the $Q$-factor variation, it is useful to consider the inductive and capacitive quality factors [7] which limit the attainable value of $Q$. In the case of SWTL, it is the low inductive quality factor that prevents the structures from high values of $Q$. For the CPW which has a larger signal-to-ground distance, the capacitive quality factor is lower and the value of $Q$ is affected by both types of quality factor. It can be seen that all SWTL have higher $Q$-factors when compared with the CPW.

The characteristic impedances of the lines are obtained from the de-embedded S-parameters according to

$$Z_C = \frac{Z_0 (1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2}. \quad (7)$$

Results are shown in Fig. 10 with values in the range of 30–50 Ohm. It can be seen that lines with larger $w_g$ has higher impedances. For the simplified lossless case approximation,

$$Z_C = \sqrt{\frac{L}{C}}. \quad (8)$$

Since lines with larger $w_g$ have a higher $L$, lines with larger $w_g$ will result in higher $Z_C$.

3. Modeling

3.1 Equivalent Circuit Model

To employ the new transmission line structure in circuit designs, an accurate model for circuit simulations is required. The proposed model of Fig. 11 considers the physics of the
A magnetic field loops around the current-carrying conductor and penetrates the closely located silicon substrate. Hence, substrate current is induced that results in parasitic inductance and resistance. As the operating frequency increases, this substrate effect increases and becomes substantial. The electric field that originates from the signal line terminates at ground potential located at the same metal plane and at the slotted ground shield underneath the signal line. Therefore, the return current due to the electric field in the silicon substrate is significantly reduced. The electric field lines also terminate at sidewalls of the ground metals. In this structure, the return current flows primarily along the coplanar metals at a distance $w_g$ from the signal line, which also develops an inductance and resistance along its path. The return current cannot effectively flow through the slotted ground shield dividing the signal line and the substrate because of the slot spaces that prevent the flow of the return current. However, due to capacitive coupling between the slotted metals of the shield, a small current exists at high frequency. With a description of the physical processes in the structure, an equivalent distributed circuit model is developed.

The model of Fig. 11 takes into account the important effects of the substrate and ground parasitic by using simple lumped equivalent circuit elements.

In the model, the series inductance and resistance are represented by $L_s$ and $R_s$, respectively. The parasitic components include the substrate resistance $R_{sub}$, substrate inductance $L_{sub}$, resistance of the ground metal along the return current path $R_{gnd}$, the associated inductance in the ground metal $L_{gnd}$, as well as the capacitance of the slot spaces in the shield metal $C_{gnd}$. The substrate and ground inductances are coupled to the line inductance. In addition, the capacitance between the signal line and the ground metals is considered with the capacitor $C$. $R_{sh}$ represents the resistance of the metal slots of the shield structure.

This model is transformed into an equivalent model of Fig. 12. This model has fewer components and it explicitly demonstrates the effect of the substrate parasitic on a shielded transmission line. The resonance loop models the increasing effects of the substrate at higher frequency. In addition, this equivalent-circuit model has kept its simplicity for the purpose of practical implementation. The proposed elements $R_{ext}$, $L_{ext}$, $M$, $C_{gnd}$, and $R_{sh}$ in this equivalent circuit are described. Equations (9)–(13) provides guidance to the value of the parameters used in the model. For Eqs. (9)–(11), fitting is made to the numerical parameters of $k_1$, $k_2$, $k_3$ and $k_4$. Approximations of the other parameters can be obtained by conventional analysis of the Telegrapher’s RLGC model. $R_{ext}$ is approximated to the substrate resistance through which the substrate current flows.

$$R_{ext} = k_1 \frac{R_{ss, Si}}{w} \quad (9)$$

$R_{ss, Si}$ is the sheet resistance of the silicon underneath the signal line and $w$ represents the width of the signal line. $L_{ext}$ is a result of the magnetic field generated by the signal line and is approximated by a fraction of $L_s$.

$$L_{ext} = k_2 \cdot L_s \quad (10)$$

The magnetic coupling coefficient is approximated by the parametric equation

$$M = 1 - e^{-k_3 \left( \epsilon_{Si}/\epsilon \right)^{k_4}} \quad (11)$$

$C_{gnd}$ and $R_{sh}$ are small due to the low values of the series capacitances linking the gaps between the slotted metals in the shield and the parallel resistances of the slotted metal, respectively. The values can be approximated by

$$C_{gnd} = \frac{\varepsilon_{ext} L_{shield} w}{m \cdot s_{slot}} \quad (12)$$

$$R_{sh} = R_{ss, slot} \cdot \frac{2w_g + w}{2m \cdot w_{slot}} \quad (13)$$

$\varepsilon_{ext}$ is the effective dielectric permittivity, $m$ is the number of metal slots per meter in the shield and $R_{ss, slot}$ is the sheet resistance of the slot metal in the shield. This model of Fig. 12 has been simulated in 80-stage cascade to evaluate the performance. To ensure the distributed characteristics of the model, the elemental stage is ensured to have a length significantly less than a wavelength of the maximum measurement frequency. Results of the modeling are explained in the next section.

### 3.2 Modeling Results

Table 3 shows the fitted parameters used in Eqs. (9)–(11).
The new parameters of the distributed model of Fig. 12 are calculated by the Eqs. (9)–(13). Tables 4(a) and 4(b) provide a summary of all the parameters used in the SWTL model.

Since all the test structures have the same length, the values of \( R_s \), \( C \), \( C_{\text{end}} \) and \( R_{\text{ext}} \) do not change, according to the physical equations that describe them. \( L_{\text{ext}} \) which is a result of the coupled inductance from the signal line is shown to have a value that is only a fraction of \( L_s \) with slight increases in the coupling coefficient \( M \). A larger \( M \) results from a larger area being coupled with increasing \( w_g \).

The model characteristics, using the calculated values, are then verified with the measured results in this frequency range. The objective is to show that the proposed model can be used to represent the fabricated structures. Figures 13 and 14 show the comparison of the attenuation and the phase constant of the fitted model and measured sample transmission line with \( w_g = 14 \mu m \).

The simulated results of the distributed model generally agree well with the measured results, especially at low frequency. However, excessive attenuation is not accounted for by the model at 65 GHz due to the switching-over of the Transmission-Reflection modules of the measurement setup as described earlier. Figure 13 shows the results of the fitted model with a sample line \( w_g = 14 \mu m \), which has the worst-case 65 GHz peaking among the results of Fig. 7. Figure 14, however, shows the excellent agreement of the phase constant of the model and measured results.

Figure 15 shows the simulated impedance of the lines using the proposed model and the measured results. The peaks and troughs are not due to measurement problems but are simply caused by the length of the line which reaches half a wavelength at this frequency [8]. This can be seen by the \( S_{11} \) of the measured SWTL showing minimum return losses and zero phases at frequencies corresponding to the half-wavelength in Fig. 16 and Fig. 17 respectively. Alternatively, this effect can be modeled by lumped circuit elements at the two ports. This results in a good fit as shown in Fig. 15 as well. The proposed model can be used in simulations to characterize the high-\( Q \) transmission lines.

The peak occurrences of the characteristic impedance
where the half-wavelength, \( \lambda/2=900\mu m \). According to Fig. 8 and Eq. (5), an equivalent value can be obtained for the sample line \( w_g=14\mu m \).

4. Conclusion

A new slow-wave transmission line structure for improving the \( Q \)-factor has been fabricated and characterized. This structure uses slotted ground shields for preventing the electric field from entering the substrate. The extended ground metal fingers of the transmission line allow higher inductions to be achieved while enabling the design to satisfy the stringent density requirements of advanced CMOS processes. The current induced in the silicon substrate by the magnetic field is modeled by the proposed distributed circuit model. This model also accounts for the leakage return current along the reverse signal path in the ground shield. The model can be employed in circuit simulators for design use.

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References


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