Low-Power Multiple-Valued Reconfigurable VLSI Based on Superposition of Bit-Serial Data and Current-Source Control Signals

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Abstract

A bit-serial multiple-valued reconfigurable VLSI using current-mode logic circuits has been proposed. A Differential-Pair Circuit (DPC) is used as a basic component of a cell, so that the static power is dissipated even in the nonactive cells. To solve the problem, autonomous ON/OFF control of the current sources is presented based on superposition of bit-serial data and current-source control signals. In the proposed switched current control technique, the static power dissipation can be greatly reduced because current sources in nonactive circuit blocks are turned off. The superposition of data and control signals in a single interconnection is effectively utilized to reduce complexity of switches and interconnections, and to eliminate skew between data and control signals. It is evaluated that the reduction of the power dissipation is remarkable, if the operating ratio is less than 75%.

1 Introduction

Reconfigurable VLSIs such as FPGAs are widely used for implementing special-purpose processors in a short time and at a low cost. This consists of an array of processing units or cells whose functions and interconnections can be programmed after fabrication [1][2]. However, there are problems of delay, area and power consumption in the conventional coarse-grain FPGA due to low utilization of a logic block in the cell and complexity of a switch block.

On the other hand, fine-grain bit-serial reconfigurable architecture has potential advantages in that fine-grain pipelining and high utilization of a cell make the performance and parallelism high, respectively [3][4]. We have proposed a fine-grain multiple-valued reconfigurable VLSI, where localized data transfer architecture and Multiple-Valued Current-Mode Logic (MVCML) are effectively employed for reduction of the complexity of switch blocks and interconnections [5]. Also, reduction of the cell area can be achieved by using a series-gating differential-pair circuit and superposition of data and start signals [6].

A threshold logic operation is done in a Differential-Pair Circuit (DPC) with one or two current sources [7]. Lower power consumption at high frequency in comparison with CMOS implementation can be achieved because power consumption of MVCML is independent of the clock frequency. However, the power of the cell in which any operation with valid data is not done is dissipated because steady currents flow in DPCs.

To solve the problem, we introduce valid signal information transfer between cells together with data transfer. The valid signal information is equivalent to the ON/OFF control signal, and its information is represented by "1" during the clock cycle when the valid data is available. The representation makes the ON/OFF control circuit very simple. Moreover, the superposition of data and control signals in a single interconnection is effectively utilized to reduce complexity of switches and interconnections, and to eliminate skew between data and control signals. The separation of the data and ON/OFF control signals can be easily done by a threshold logic operation, so that the hardware overhead is small. The prototype of the reconfigurable VLSI is designed and implemented based on 65nm CMOS design rule. A special I-V converter is proposed to make the voltage differences between logic values uniform. Using the proposed switched current control technique, the static power dissipation can be greatly reduced because current sources in nonactive circuit blocks are turned off. It is evaluated that the reduction of the power dissipation is remarkable, if the operating ratio is less than 75%.

2 Review of architecture of the multiple-valued reconfigurable VLSI

As shown in Fig. 1, the multiple-valued reconfigurable VLSI consists of many identical cells, where each cell can be connected to its 8-neiborhood cells. The cell consists of
a logic block and a switch block. A one-bit storage circuit is provided which is used to make a bit-serial fine-grain operation and a temporal storage of an intermediate result. As shown in Fig. 2, the direct allocation of Control/Data Flow Graph (CDFG) is introduced, where each node in the CDFG corresponds to a macro-block in the multiple-valued reconfigurable VLSI and each edge corresponds to data transfer between macro-blocks. A macro-block consists of a cell or multiple cells. Such architecture for the localized data transfer can be effectively employed to reduce the complexity of interconnections and delay due to data transfer between cells.

As shown in Fig. 3, a fine-grain multiple-valued cell has been proposed to realize bit-serial operations. The cell consists of a Universal Literal (UL) module, a D-flipflop (D-FF) and an Output circuit (DO), a start control module, and a switch block. The UL module consists of a UL/FA circuit, an I-V converters, and an AND /NOT circuit provided for a multiplication and a subtraction. Any 2-variable binary logic functions can be realized by the UL. Therefore, any n-variable binary logic functions can be implemented by programming the UL modules. Also, a bit-serial adder composed of a Full Adder (FA) can be programmed by the UL module. In a bit-serial operation, start signal which indicates a head of one-word data is required to initialize a D-FF used for state memory. Superposition of data and start signals is introduced to reduce the complexity of a switch block.

The steady currents always flow in DPCs and the power is consumed even if the cell does not operate for valid data inputs. To reduce power consumption of nonactive cells, we introduce autonomous current-source control in each cell.

3 Current-source control for low-power operation

3.1 Principle of current-source control

In the current-mode logic circuit, the cut-off of the current sources can be easily achieved by the ON/OFF control signal. As shown in Fig. 4, Vref is selected in the multiplexer if the valid signal is "1". Then, the current source turns ON, and the threshold logic operation is started. On the other hand, the voltage 0V is selected if the valid signal is "0". Then, the current source turns OFF, and the wasted
current is saved. In the conventional cell, the start signal is required to initialize a D-FF used for state memory. However, it is not necessary if the valid signal "0" is inserted between words and initializes a D-FF.

Figure 5 shows a principle of current source ON/OFF control in the cellular array of the reconfigurable VLSI. Let us consider the scheduled DFG of Fig. 5(a) as an example, where 2-bit serial additions are successively performed. The corresponding mapping on the cellular array is shown in Fig. 5(b), where each cell consists of the UL module and DO module of Fig. 3. In clock1, only cell1 is controlled to be active and the other cells remain nonactive. In clock2, cell1 performs the second bit operation and cell2 is controlled to be active and the other cells remain nonactive. In clock3, U1 of the cell1 turns off and O1 of the cell1 remains ON. The similar control is done in clock4 and clock5.

### 3.2 Superposition of bit-serial data and current-source control signals

To make the autonomous ON/OFF control of current sources, valid signal information is transferred between...
cells together with data transfer. Figure 6 shows an example of the valid signal representation. When the valid signal is "1" the valid data is available, otherwise the data is invalid. The representation corresponds to the clock cycle of a valid data, and it is used as the ON/OFF control signal. Therefore, it is not necessary to provide an additional circuit to generate the ON/OFF control signal. To reduce complexity of switches and interconnections, and to eliminate skew between data and control signals, we introduce superposition of data and control signals in a single interconnection as shown in Fig. 7. In Fig. 7(a), data1, data2 and the valid signal are separately transferred from 8-neighborhood cells. Accordingly, a $8 \times 3$ switch matrix is essential. On the other hand, data2 and the valid signal are superposed in Fig. 7(b). Therefore, a $8 \times 2$ switch matrix is sufficient to construct a switch block. Table 1 indicates definition of the superposed signal. If the valid signal is "0", the superposed signal is always "0" irrespective of the data value. If the valid signal is "1", the superposed signal is equal to the data value +1 which can be linear summation of the valid signal and the data as shown in Fig. 7.

4 Design of the cell and evaluation

Figure 8(a) shows the structure of the proposed cell. The cell consists of a UL module, a current-source control module, a DO module and a switch block. The UL module is same as that of the cell without ON/OFF control of Fig. 3. The current-source control module consists of the valid signal detector of Fig. 8(b), two multiplexers, a D-FF and an OR gate. The superposed signal enters the I-V converter from In2, and the valid signal is separated by the valid signal detector, where the threshold logic operation is done.
with the threshold value "0.5" as shown in Fig. 8(b). The multiplexer is used as a voltage-level converter, so that an appropriate gate voltage can be applied to make the current sources turn ON. In the current-source control of Fig. 5, it is often required to make only a DO module of a cell active. For example, only the DO module O1 is active in Cell1 at clock3. Such a control mode can be realized using the same current-source control module of Fig. 8(a), because D-FF2 and the OR gate makes the one-clock delay of the valid signal Vs. The overhead of the current-source control module is very small, because hardware complexity of the current-source control module of Fig. 8(a) is almost same as that of the start control module of Fig. 3. D-FF1 in the DO module stores the output of the UL module. The Output circuit of Fig. 9 controls superposition of a valid signal and D-FF1 output according to a configuration memory data C as shown in Fig. 9. When the configuration memory data C is "0", the left side transistors of the DPC2 turns OFF. Then, the valid signal is not superposed on the output. When both of the configuration memory data C and the valid signal are "1", the left side transistors of the DPC2 turns ON. When the configuration memory data C is "1" and the valid signal is "0", the current source of DPC2 is controlled to be "0".

The performance and power consumption of the cell are evaluated based on HSPICE simulation using a 65nm CMOS design rule. Figure 10 shows the power consumption versus the ratio of the number of valid data signals to that of total data signals which corresponds to the utilized ratio of the cell. Compared to the cell without ON/OFF control, the power reduction is remarkable if the utilized ratio is small. In fact, the cross point is 75%.

The number of transistors in the cell and the clock cycle are evaluated as shown in Table 2. Compared to the cell without ON/OFF control, the number of transistors is increased by 7%. This means that the hardware overhead is very small in the ON/OFF control scheme. However, the clock cycle is increased by 65%, because the wake-up time is required to make DPCs turned ON.

The prototype of the reconfigurable VLSI is designed based on 65nm CMOS design rule as shown in Fig. 11. The 16 × 32 cellular array is constructed in the prototype chip, where the current-source control module is provided for each cell. In the 65nm CMOS design rule, nonlinearity of a pMOS resistor cannot be neglected, so a special pMOS resistor circuit using two pMOS transistors is introduced. The resistor is utilized to make the voltage differences between logic values uniform in the I-V converter.

5 Conclusion

A new technique of the autonomous ON/OFF control of the current sources is proposed based on superposition of bit-serial data and current-source control signals. We can confirm that the static power dissipation can be greatly reduced to 54.6% in the case of 25% utilized ratio of the cells. This is achieved by design of the simple ON/OFF control circuit. The superposition of bit-serial data and current-
source control signals is effectively employed for reducing complexity of the switch block and eliminating skew between data and control signals in nano-scale device era.

As a future problem, it is important to improve the clock cycle in the proposed ON/OFF control scheme. One solution is to set the valid signal information one clock earlier than the valid data arrival. Also, we need to consider the granularity of the ON/OFF control of the current sources for the total power minimization.

References


