Computer Architecture & Technology: some thoughts on the road ahead

M. J. Flynn

FCRC 2003
San Diego
June, 2003
Outline

• The technology road ahead
• Time: Performance and tradeoffs
• Power
• Area
• Beyond Time x Power x Area: computational integrity, design time and interconnections
• The shape of the “new” system
## Semiconductor Industry Roadmap

### Semiconductor Technology Roadmap (2001/02)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology generation (nm)</td>
<td>90</td>
<td>65</td>
<td>32</td>
<td>22</td>
</tr>
<tr>
<td>Wafer size (mm)</td>
<td>300</td>
<td>300</td>
<td>450</td>
<td>450</td>
</tr>
<tr>
<td>Defect density (per m²)</td>
<td>1356</td>
<td>1356</td>
<td>1116</td>
<td>1116</td>
</tr>
<tr>
<td>iP die size (mm²)</td>
<td>310</td>
<td>310</td>
<td>310</td>
<td>310</td>
</tr>
<tr>
<td>Chip Frequency (GHz)</td>
<td>4</td>
<td>6.7</td>
<td>19.4</td>
<td>29</td>
</tr>
<tr>
<td>MTx per Chip (Microprocessor)</td>
<td>552</td>
<td>1204</td>
<td>3424</td>
<td>6200</td>
</tr>
<tr>
<td>MaxPwr(W) High Performance</td>
<td>160</td>
<td>190</td>
<td>251</td>
<td>290</td>
</tr>
</tbody>
</table>
What this means to Computer Architecture

Tradeoffs in time (performance), power and area (cost). (TPA product)
Time (Performance), Area and Power Tradeoffs
Performance lesson: wires not gates determine delay.
High Speed Clocking

Fast clocks are not primarily the result of technology scaling, but rather of architecture/logic techniques:

- Smaller pipeline segments, less clock overhead

- Modern microprocessors are increasing clock speed more rapidly than anyone (SIA) predicted…fast clocks or *hyperclocking*. (really short pipe segments)

- But fast clocks do not by themselves increase system performance
CMOS processor clock frequency

![Graph showing the CMOS processor clock frequency over the years from 1967 to 2003. The x-axis represents the year (1967, 1973, 1983, 1993, 2003) and the y-axis represents the frequency in MHz (1, 10, 100, 1000, 10000). The graph illustrates an increasing trend in frequency over time.]
Bipolar and CMOS clock frequency

![Graph showing the frequency of Bipolar and CMOS over the years 1967 to 2003. The x-axis represents the years 1967 to 2003, and the y-axis represents frequency in power limits.]
Bipolar cooling technology (ca ’93)

Hitachi 880: 500 MHz; one processor/module, 40 die sealed in helium then cooled by a water jacket. Power consumed: about 700 watts per 10x10 cm module
SIA clock rates

![Graph showing the trend of SIA clock rates from 1998 to 2016. The x-axis represents the years (1998, 2001, 2007, 2013, 2016), and the y-axis represents frequency in cycles per second (100, 1000, 10000, 100000). The graph illustrates a significant increase in clock rates over time, with hyper frequency indicated.]
Lower clock overhead enables more pipe segments & higher freq.

- Let the total instruction execution without pipelining and associated clock overhead be $T$
- Let $S$ be the number of segments and $S - k$ be the number of cycles lost due to a pipeline break ($S > k$)
- Let $b = \text{prob of break/instr.}, C = \text{clock o’head incl skew}$

![Diagram]

- $T$ is the total execution time without pipelining.
- $T/S$ is the time for each segment.
- $C$ is the clock overhead per cycle.
- $T + CS$ is the total execution time with pipelining.
- $b$ is the probability of a pipeline break per instruction.
- $S - k$ is the number of cycles lost due to a pipeline break.
Performance, issue rate and frequency

Performance is largely determined by cycle time, issue rate and \(b\), the disruption rate.

Optimum \(S\) (and max freq.) is additionally determined by \(C\).

\[
S_{opt} = \sqrt{\frac{f(k) T}{b C}}
\]

Dubey and Flynn’90
Optimum Pipelining and ILP

Optimum pipe segment size is determined by clock overhead, C

Optimum issue rate, m, is determined by issue overhead, o
Architecturally (ignoring technology), what’s happened to T, b and C?

- T has increased, probably 25-50%, due to added processor complexity
- b has decreased significantly, probably from .20 to closer to .05, due to better compilers, prediction and cache management.
- C has at least halved due to better clocking.
- So S has increased by more than 4-6x decreasing the number of F04s/cycle
Change in pipe segment size

![Graph showing the change in FO4 delays per clock from 1996 to 2006. The delays decrease significantly over the years.]

- **1996**: 120 delays per clock
- **1999**: 40 delays per clock
- **2003**: 10 delays per clock
- **2006**: 0 delays per clock

*FO4 gate delays*
Performance: where’s the memory “wall”? 

- **The memory “wall”:** performance is limited by the predictability & supply of data from memory. This depends on the access time to memory and thus on wire delay which remains constant with scaling.

- But (so far) significant hardware support (area, fast dynamic logic) has enabled designers to manage cache misses, branches, etc reducing access to memory requirements and avoiding the wall.

- It may be better to think of a *frequency* (minimum segment size) “wall” and how to improve performance without changing the segment size.
Power: the real price of performance

$$P_{\text{total}} = \frac{C \cdot V^2 \cdot \text{freq}}{2} + I_{\text{leakage}} \cdot V + I_{\text{sc}} \cdot V$$

While $V_{\text{dd}}$ and $C$ (capacity) decrease, frequency increases at an accelerating rate thereby increasing power density.

As $V_{\text{dd}}$ decreases so does $V_{\text{th}}$; this increases $I_{\text{leakage}}$ and static power.

Net: while increasing frequency may or may not increase performance - it certainly does increase power.
Power: a new frontier

- Cooled high power: >70w/die
- High power: 10-50w/die ... plug in supply
- Low power: 0.1-2w/die.. rechargeable battery
- Very low power: 1-100mw/die..AA size batteries
- Extremely low power: 1-100 microwatt/die and below (nano watts) .. button batteries
# Battery Energy & use

<table>
<thead>
<tr>
<th>type</th>
<th>energy capacity</th>
<th>time</th>
<th>power</th>
</tr>
</thead>
<tbody>
<tr>
<td>rechargeable</td>
<td>10,000 mAh</td>
<td>50 hours (10-20% duty)</td>
<td>400 mw-4w</td>
</tr>
<tr>
<td>2xAA</td>
<td>4000 mAh</td>
<td>_ year (10-20% duty)</td>
<td>1-10 mw</td>
</tr>
<tr>
<td>button</td>
<td>40mAh</td>
<td>5 years (always on)</td>
<td>1uw</td>
</tr>
</tbody>
</table>
Power is important!

By $V_{dd}$ and device scaling

$$\frac{\text{freq}_2}{\text{freq}_1} = \sqrt[3]{\frac{P_2}{P_1}}$$

- By scaling alone a 1000x slower implementation may need only $10^{-9}$ as much power.
- Gating power to functional units and other techniques should enable 100MHz processors to operate at $O(10^{-3})$ watts.
- Goal: $O(10^{-6})$ watts…. Implies about 10 MHz
Extremely Low Power

System: suppose low power was the metric, rather than cycle time.
Very Low power ($\mu$W) can be achieved:
- Perhaps sub threshold circuits
- Clock rate may be limited to 10 MHz (?)
- Achieve 1 to 5 year battery life
- Lots of area, BUT how to get performance
  - Very efficient architecture and segmented powering.
  - Very efficient software & operating system
  - Very efficient arithmetic & signal processing
  - Very effective parallel processing

- Once again the frequency “wall”: challenge use area not frequency to achieve performance
Area: the basics of wafer and die size

- Wafers, 30 cm in diameter produce $(\pi d^2/4)/A$ dice, about 700 1cm$^2$ dice per wafer.
- Yield (% of good die) is $e^{-\frac{\rho A}{2}}$ where $\rho$ is the defect density, $\rho A = .2$; Yield is 80%
The basics of wafer fab

• A 30 cm, state of the art (\( \square = 0.2 \)) wafer fab facility might cost $3B and require $5B/year sales to be profitable…that’s at least 5M wafer starts and almost 5B 1cm die /per year. A die (\( f=90\text{nm} \)) has 100-200 M tx /cm\(^2\).

• At O($1000) per wafer that’s $1/die or 100M tx. So how to use them?
Area and Cost

Is efficient use of die area important?
Is processor cost important?
NO, to a point — server processors (cost dominated by memory, power/cooling, etc.)
YES – “client”, everything in the middle.
NO – small, embedded die which are package limited. (10-100Mtx/die)
Area

Indeed, looking ahead how to use from 0.2 to 2+ billion transistors/cm$^2$ die?

– With performance limited by power, memory & program behavior servers use multiple processors per die, limited by memory.
– For client systems either “system on a chip” or hybrid system are attractive.
– Low cost embedded systems need imaginative packaging and enhanced function.
Hybrid system: a possibility

- Core, *very low power* units comprise limited storage, limited processing, *crypto* and *wireless*: “watch” type package
- Multi user displays, keyboards, voice entry and network access can be implemented with higher power.
- Wireless, secure interconnects complete the system, but with major power management implications.
Beyond T x A x P …other design dimensions

- Computational integrity and RAS
- Design time and FPL
- Configure ability / system connections and wireless technology.
Computational Integrity

Design for

- Reliability
- Testability
- Serviceability
- Process recoverability
- Fail-safe computation
Design time: CAD productivity limitations favor FPL

Source: S. Malik, orig. SEMATECH
Computer Architecture & Arithmetic Group

**Logic Transistors per Chip (K)**

<table>
<thead>
<tr>
<th>Year</th>
<th>Transistors/Staff - Month</th>
</tr>
</thead>
<tbody>
<tr>
<td>1981</td>
<td>10</td>
</tr>
<tr>
<td>1983</td>
<td>100</td>
</tr>
<tr>
<td>1985</td>
<td>1,000</td>
</tr>
<tr>
<td>1987</td>
<td>10,000</td>
</tr>
<tr>
<td>1989</td>
<td>100,000</td>
</tr>
<tr>
<td>1991</td>
<td>1,000,000</td>
</tr>
<tr>
<td>1993</td>
<td>10,000,000</td>
</tr>
<tr>
<td>1995</td>
<td>100,000,000</td>
</tr>
<tr>
<td>1997</td>
<td>1,000,000,000</td>
</tr>
<tr>
<td>1999</td>
<td>10,000,000,000</td>
</tr>
<tr>
<td>2001</td>
<td>100,000,000,000</td>
</tr>
<tr>
<td>2003</td>
<td>1,000,000,000,000</td>
</tr>
<tr>
<td>2005</td>
<td>10,000,000,000,000</td>
</tr>
<tr>
<td>2007</td>
<td>100,000,000,000,000</td>
</tr>
<tr>
<td>2009</td>
<td>1,000,000,000,000,000</td>
</tr>
</tbody>
</table>

**58%/Yr. compound Complexity growth rate**

**21%/Yr. compound Productivity growth rate**

Source: S. Malik, orig. SEMATECH
Computer Architecture & Arithmetic Group
Interconnects: optical and wireless technologies

- Essential to realizing efficient client and package limited systems
- RF can be power consumptive, requires very efficient channel management.
  - Focused, adaptive radiation patterns
  - Digital management of RF
  - Probably better suited to MHz rather than GHz RF… in conflict with antenna goals
  - Many issues: security, multi signal formats, etc.
  - Distance between tx and rx is key to power mgmt.
The “New” Server System

Server Processor

– Cost insensitive
– Fast (but power limited) cycle time
– Multiple (order of 10’s to 100) processors on single die, together with portion of memory space
– MIMD extensions via network
– Base processor using ILP with SIMD extensions
– Very high integrity
Client System

- Invisible core... integrated into
  - Appliances
  - Communications devices
  - Notebooks
  - “Watches”, wearable cores

- Always secure and available
- Very low power
- Integrated wireless/networked
The “New” Client System

Client

– “System on a chip,” integrated, hybrid or embedded
– Many frequency-power design points from 100 mW with cycle time 1 ns to 1 mW with cycle of 100 ns
– Several base processors
  • Core and signal processors
– High integrity
– Signal processors VLIW/SIMD
The System Design Challenge

• Performance in more important than ever.
  - But use area (concurrency) not frequency to achieve performance with lower power.

• IP’s – not IC’s. Amalgamate existing designs from multiple sources
  – Validate, test, scale, implement

• Buses and Wires
  – Placement and coupling, wire length, delay modules… some role for optics?

• Effective floorplanning
System Design: Other Challenges

• Really good power management
• Low power wireless interconnections
• Integrity – Security
• Scene/ pattern recognition
• Software efficiency: Op Systems, compilers
• Software productivity: rules based, analysis, heuristic, etc.
Summary

• Processor design with deep sub-micron (f < 90nm) technology offers **major advantages:** 10x speed or $10^{-6}$ power and 100x circuit density. Indeed, SIA projections have consistently underestimated the future.

• *But the real challenge is in system design: new system products and concepts, interconnect technologies, ip management and design tools.*