Prospects of 3D Inductors on Through Silicon Vias Processes for 3D ICs

Yiorgos I. Bontzios, Michael G. Dimopoulos, Alkis A. Hatzopoulos
Department of Electrical & Computer Eng., Aristotle Univ. of Thessaloniki, Thessaloniki, Greece
E-mail: gmpontzi@auth.gr, mdimop@ieee.org, alkis@eng.auth.gr

Abstract—Three dimensional (3D) integration attempts to keep Moore’s Law effectively in the years to come. Through-silicon-vias (TSV) processes offer a step towards 3D integration. In this work, the aspects of inductors in the TSV technologies are studied. Various TSV inductor topologies are examined both theoretically and by means of numerical simulations. As results show, true 3D vertical inductor designs offer improvements in inductance and quality factor over the planar ones.

Keywords-component: Through silicon vias; Integrated inductor; Inductance; CMOS; 3D ICs.

I. INTRODUCTION

The rising demand for portable/wireless devices is driving the full integration of wireless and RF systems towards system-on chip (SoC) solutions. As devices have scaled down according to Moore’s law, the complexity of both the circuit design but also the demands on its interconnects have increased.

TSV has emerged as the most promising solution to alleviate all the limiting factors that pose a serious impediment to Moore’s law by reducing line length and minimizing parasitic impedance, especially inductance [1]. Some early 3D oriented chips have been already fabricated [2]-[4]. First order models have been reported also, based primarily on fitting simulation data [5]-[8].

TSVs have been proposed to be used in many applications such as high performance capacitors or Faraday cages for isolation purposes [2]. However, their use has not been studied on the integrated inductors. A recent study has been performed only in transformers [9] by means of simulation. Integrated inductors constitute a key component to RF systems on chip. For this reason, the need for integrated inductors with reasonable characteristics has become urgent. However, inductors remain still one of the most difficult parts to integrate due to the multiple loss mechanisms they suffer from. Thus, it is considered challenging to investigate the prospects of the integrated inductors in the new 3D era.

This work is organized as follows. A brief review of the current inductor design is presented in section II followed by a theoretical analysis of the TSV inductors. Simulation results comparing the current 2D-inductor design with the foreseen 3D inductor design are presented in section III. This paper is concluded in section IV.

II. TSV INDUCTORS INVESTIGATION AND PROGNOSTICS

In this section, the design of the integrated inductors in the framework of the new 3D process is theoretically investigated. In the next section the conclusions derived by this analysis will be validated with a commercial simulator.

An accurate characterization of the inductor component (as for any component) may be accomplished only by fabrication and measurement. But the resulting model is not predictive and cannot be used for prognostics [10]. This is also supported by the fact that the parameters of the emerging TSV processes have not been standardized yet, but different dimensions are proposed by various foundries [2]-[4]. In Table I the dimensions of various parameters of current and TSV processes are presented. In this work the TSV inductors are investigated in terms of the typical value ranges that have been proposed.

Before, proceeding to the TSV inductor study, it is constructive to briefly review the planar inductor design and present its weaknesses.

A. Planar Inductors

The most common integrated inductor shape in modern technologies is the planar spiral square inductor shown in Fig. 1. Other inductors shapes that are also used are the octagonal and the circular inductor [10]. The square inductor exhibits the highest inductance and the lowest quality factor among other shapes for a given area, whereas the circular inductor offers the highest quality factor in the expense of the lowest inductance value for a given area.

The quality factor $Q$ of the planar inductors is poor, ranging typically from 10 to 20. Furthermore, the useful frequency range is limited to about 20 GHz for inductance values of a few nH. Larger frequencies can be achieved for lower inductances.
The behavior of a TSV inductor will be studied next. For the sake of distinction, variables referring to planar inductors will be denoted with a “~”, e.g. $R_{DC}$. The numerical values for the presented parameters on Table I, are taken as the mean average of the corresponding ranges.

1) DC Resistance

The track resistance $R_{DC}$ of the inductor can be computed with the common formula of resistance:

$$R_{DC} = \frac{\rho \cdot l}{w}$$  \hspace{1cm} \text{(1)}$$

In TSV process, the series resistance of the inductor can be reduced in comparison to the current process, since the cross section of the inductor track may be much larger. In particular, assuming that the inductor is ideally designed by using only TSVs (the contribution of horizontal tracks is negligible), while the conventional inductor is design in top metal (as it is the usual case) and substituting the typical values from Table I, the succeeded improvement would be:

$$\alpha_{DC} = \frac{R_{DC}}{R_{DC}} = \left(\frac{\rho \cdot \frac{L}{w}}{\rho \cdot \frac{L}{w}}\right) \left(\frac{\rho \cdot \frac{L}{w}}{\rho \cdot \frac{L}{w}}\right) = \frac{w}{0.5 \cdot d^2} = \frac{10}{0.5 \cdot 10^{-2}} = \frac{1}{5}$$  \hspace{1cm} \text{(2)}$$

or 5 times better. This implies that $Q$ can be ideally increased by 500%, which is a tremendous increase considering that a typical increase in planar processes ranges approximately between 20-30%. It is obvious, that this is an ideal situation. In practice horizontal metal is always necessary for the connection of the TSVs thus the overall improvement will be less. But with clever design the contribution of the horizontal resistance may be kept limited to small values without significantly affecting the above result.
2) AC Resistance; Skin effect

As frequency increases, the current crowds at the edges of the conductor and flows in a thin layer around its outer edges. Obviously, the AC resistance $R_{AC}$ of the inductor will depend on the perimeter $P$ of the conductor. The larger the perimeter the lower will be the resistance. Thus, a lower $R_{AC}$ is expected in TSV inductors.

For the most common metal used, copper, which has resistivity value $\rho = 1.68 \times 10^{-4}$ $\Omega$m at 20$^\circ$C and relative permeability $\mu_r = 1$, the skin depth at frequency $f = 1$GHz is:

$$\delta = \sqrt{2\rho f/\mu_r} = 2 \mu m$$  (3)

Thus, for tracks of width equal to 2 $\mu m$ or more and for frequencies over a few GHz, the $R_{AC}$ becomes dominant, with respect to the DC resistance.

According to [11] the skin effect may be modeled with an effective thickness $t_{eff} = \delta(1 - e^{-\delta/t})$ inside which the current is assumed to flow. Then $R_{AC}$ may be written in terms of the effective thickness and the perimeter of the conductor as:

$$R_{AC} = \rho \cdot \ell / (Pt_{eff})$$  (4)

The ratio $a_{AC}$ of the AC resistance of the TSV inductor to the AC resistance of the planar inductor, by substituting the values of Table I, will be:

$$a_{AC} = \frac{R_{AC}}{R_{DC}} \Rightarrow a_{AC} = \frac{\delta}{P} = \frac{(2 \cdot 10 + 2 \cdot 2) \times 10^{-6}}{(2 \cdot 10 + 2 \cdot 10) \times 10^{-6}} = \frac{3}{5}$$  (5)

and the ratio $a_{AC}$ becomes:

$$a_{AC} = \frac{2 \times 10 + 2 \times 1.5}{3.14 \times 10} = 0.7 = \frac{3.5}{5}$$  (6)

It is clear, that $a_{AC}$ is now reduced in comparison with $a_{DC}$ but the succeeded improvement still remains high, over 40%.

The TSV inductor, when compared to the planar one, offers better performance due to the generally lower $R_{DC}$ and $R_{AC}$ resistance values. In fact, performance increases by minimizing the length of the horizontal metal tracks.

3) Capacitance

The capacitance to the substrate (Fig. 4) is expected to be increased in TSV conductors since the effective area of the tracks would be larger while the effective separation distance to the substrate and backplane would be closer.

In the TSV process the track of the inductor is perpendicular to the substrate backplane. A first-order closed-form expression for this capacitance [6] is:

$$C = \varepsilon_0 f t / \ln[1 + (r_0 / r)]$$  (7)

where $r$ is the radius of a cylinder approximating the TSV and $\beta, \gamma$ are constants that are determined by fitting with data.

For the planar inductor the capacitance of a track to the substrate may be approximated to first order with the problem of a cylinder above infinite ground plane. This can be analytically solved using the method of images, resulting to the following expression for the capacitance:

$$\tilde{C} = 2\pi f \ell / (\cosh^{-1}(h / r))$$  (8)

Therefore, the ratio of the capacitance values between tracks of the same length is, in general:

$$\frac{C_2}{C_1} = \frac{\beta \cosh^{-1}(h / r)}{2\pi \ln(1 + \gamma / h / r)}$$  (9)

For relatively small substrate heights (and thus TSV heights), the capacitance to substrate is higher in TSV inductors and is increased with the aspect ratio. For aspect ratios of one order of magnitude or more, which is the typical case, the ratio $a_c$ saturates to a specific value.

III. SIMULATION RESULTS

Simulations have been performed by utilizing a simulator which employs the Boundary Element Method (BEM). All the comparison results were performed between inductors with the same inductance value $L$, since this is the parameter to be considered regarding design. The particular dimensions of the planar inductors have been chosen by taking into account the typical dimensions encountered in practice and as an average tradeoff between $Q$ and area. It has been shown [10] that the occupied area of planar inductors is proportional to $Q$. Thus, a higher $Q$ value than the one illustrated in the presented experiments may be succeeded but with an area overhead.

The TSV process considered here, consists of two wafers connected as F2B. For the comparison to be fair, the TSV inductors have been compared with simple square planar inductors without any additional enhancements like PGS.

In the first experiment, the substrate height and thus the length of the TSVs are set to 200$\mu$m. Fig. 5 shows the results for four different inductors. A planar inductor (classic) of 2.5 turns, two TSV inductors (TSV1, TSV2) of toroidal design with different width of TSVs and a TSV inductor (TSV3) of vertical design. The particular parameters for the inductors are given in Table II. It must be mentioned, that the diameter of the planar inductor is measured horizontally and that of the TSVs is measured vertically, whereas the surface area is measured for both inductors horizontally.

The quality factor for all three TSV inductors is superior over the planar one. In fact, the quality factor of the TSVs with greater width is almost 4 times the value of the classic inductor supporting the theoretical analysis discussed before.
The frequency range of the TSV inductors is decreased as a result of the larger capacitance to the substrate.

In the second experiment, the substrate height is set to 50 μm. Three different inductors have been studied. A planar inductor (classic) of 1.5 turns and two TSV inductors (TSV1, TSV2) of toroidal design with different width of TSVs. The particular parameters for the inductors are given in Table III. For the diameter and the surface area the same are valid with the first experiment. The results are depicted in Fig. 6.

Here the effect of the TSVs is reduced. The quality factor is only slightly better than the planar one. This is attributed to the shorter length of the thick TSVs. The frequency range is again lower due to the larger effective area of TSVs in comparison with the horizontal layers.

IV. CONCLUSION

The potential of the inductor design in the emerging 3D ICs with TSVs is examined in this work. Two different inductor topologies have been investigated theoretically and by means of numerical simulations. Comparative results with planar inductors of current technology are presented. The comparison reveals a superior quality factor of the TSV inductors in the expense of a small decrement in the frequency range for substrate heights higher than 50 μm. For substrate heights lower than 50 μm the TSV inductor performance becomes inferior and it may be chosen when the area overhead is of critical concern.

REFERENCES


TABLE II. INDUCTOR PARAMETERS USED IN THE FIRST EXAMINED CASE OF SUBSTRATE HEIGHT EQUAL TO 200 um.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Classic</th>
<th>TSV1</th>
<th>TSV2</th>
<th>TSV3</th>
</tr>
</thead>
<tbody>
<tr>
<td>metal width (μm)</td>
<td>10</td>
<td>10</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>metal thickness (μm)</td>
<td>2</td>
<td>10</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>total length (μm)</td>
<td>650</td>
<td>1200</td>
<td>1200</td>
<td>1100</td>
</tr>
<tr>
<td>diameter (μm)</td>
<td>120 (h)</td>
<td>200 (v)</td>
<td>200 (v)</td>
<td>200 (v)</td>
</tr>
<tr>
<td>horizontal area (μm²)</td>
<td>(120x120)</td>
<td>(100x50)</td>
<td>(100x50)</td>
<td>(100x50)</td>
</tr>
</tbody>
</table>

Figure 5 Inductance (a) and quality factor (b) of three TSV inductors in comparison with a planar inductor

TABLE III. INDUCTOR PARAMETERS USED IN THE SECOND EXAMINED CASE OF SUBSTRATE HEIGHT EQUAL TO 50 um.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Classic</th>
<th>TSV1</th>
<th>TSV2</th>
</tr>
</thead>
<tbody>
<tr>
<td>metal width (μm)</td>
<td>10</td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>metal thickness (μm)</td>
<td>2</td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>total length (μm)</td>
<td>200</td>
<td>600</td>
<td>600</td>
</tr>
<tr>
<td>diameter (μm)</td>
<td>80 (h)</td>
<td>50 (v)</td>
<td>50 (v)</td>
</tr>
<tr>
<td>horizontal area (μm²)</td>
<td>(80x80)</td>
<td>(100x50)</td>
<td>(100x50)</td>
</tr>
</tbody>
</table>

Figure 6 Inductance (a) and quality factor (b) of two TSV inductors in comparison with a temporary