A Low-Power, Small-Size 10-Bit Successive-Approximation ADC

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SUMMARY A new Successive-Approximation ADC (Analog-to-Digital Converter) was designed which not only consumes little power, but also requires a small chip area. To achieve those goals, both comparator and internal DAC (Digital-to-Analog Converter) have been improved. The ADC was designed in a 1.2 μm CMOS double-poly double-metal n-well process. It performs 10-bit conversion with 67 dB SFDR. Power consumption and die area are 0.6 mW and 0.95 mm², respectively. ADC was extensively simulated using Hspice to verify the desired performance.

1. Introduction

New systems have large digital parts with analog blocks such as ADCs in one chip. To minimize the digital noise interference to analog parts and reduce power, differential and low power structures must be used. Successive-approximation ADCs are good candidates for such applications, due to the minimal amount of analog hardware and power required [1]. However, conventional differential capacitor based successive-approximation ADCs suffer from large total capacitance, too many switches, large chip area and extra power consumption. The new successive approximation ADC described here has improved both challenging parameters. Moreover, the new design achieves a small area and a low power consumption.

2. Architecture

Figure 1 shows block diagram of a conventional Successive-Approximation ADC. For internal DACs there are three main structures:

1. Resistive division of the reference voltage
2. Charge redistribution by a capacitor array
3. Combination of charge redistribution and resistive voltage division techniques (two-stage DAC).

The first method is not a good choice for CMOS processes because of high output resistance of resistor string. Furthermore, for an m-bit converter 2ᵐ resistors and 2ᵐ + 1 switches are needed. Thus, this method requires a complex switch driving logic circuitry, which is not suitable at all for high resolution (more than 6 bits) applications. In the second method, S/H and subtraction blocks are merged in DAC, but it requires 2ᵐ unit capacitors that consume a large die area for a high-resolution conversion. By combining the two methods and use of an n-bit resistor string and a k-bit binary weighted capacitor array, we can design an m = n + k bit DAC. The method offers the advantages of the charge redistribution method, combining S/H, DAC, and subtraction blocks, which hereon we will call SDS block.

3. SDS Block

Figure 2 shows a fully differential SDS that has 66 switches, 128 resistors, and only 20 unit capacitors. Main advantage of this structure is its very low loss, which is critical in low voltage circuits. It is

\[ A_{SDS} = \frac{C}{C + C + C + C} \]  

(1)

In the above equation, \(A_{SDS}\) is the gain (loss) of the voltage division from the ADC’s input to the input of the comparator, \(C\) is the sampling capacitor and \(C_r\) is the parasitic capacitor at the comparator’s input nodes. \(C_r\) is estimated 60fF and \(C\) was chosen 1.6 pF. Another advantage of this configuration is that by opening \(S_A\) a little before \(S_B\), and \(S_B\) before other switches of the DAC, we have equal charge injection at two sides of capacitor array (the charge injection mismatch is eliminated). In Fig. 2 \(V_{in} + V_{ref}/2\) is the common mode of DAC. In order to minimize voltage change in the input common-mode potential of the comparator, \(V_{in} + V_{ref}/2\) is set near the common-mode voltage of the input signal. \(V_{ref}\) is half of maximum differential input swing. In sampling mode, switches \(S_4, S_6, S_7, S_{17}\) and \(S_{33}\) are closed and the others are opened (note that all switches are dual). In this
Fig. 2  A fully differential SDS with 20 unit capacitors.

mode input signal is sampled in the sampling capacitors, $C$. In conversion mode, switches $S_A$, $S_B$, and $S_1$ are opened and switches $S_5$ are closed. Change in voltage of node $x_1$ is
Fig. 3 The proposed SDS with 20 unit capacitors, 45 switches, and 64 unit resistors.

\[ V_x + \frac{V_{ref}}{2} - V_i^+ \]  

and for node \( x_2 \) is

\[ V_x + \frac{V_{ref}}{2} - V_i^- \]  

hence the change in differential input of comparator is

\[
V_{inc} = A_{SDS} \begin{bmatrix} (V_x + \frac{3V_{ref}}{4} - V_i^+ - V_i^-) \\
(V_x + \frac{V_{ref}}{4} - V_i^+ - V_i^-) \end{bmatrix} 
= A_{SDS} (V_i^+ - V_i^-) \] (4)

As Eq. (4) shows, the first bit is the sign bit. To determine the second bit, switches \( S_5 \) are opened. If the sign bit is 1, switches \( S_3 \) are closed to determine the second bit. In this case input of comparator becomes

\[
V_{inc} = A_{SDS} \begin{bmatrix} (V_x + \frac{3V_{ref}}{4} - V_i^+) \\
(V_x + \frac{V_{ref}}{4} - V_i^-) \end{bmatrix} 
= A_{SDS} \left[ \frac{V_{ref}}{2} - (V_i^+ - V_i^-) \right] \] (5)

and when the sign bit is 0, switches \( S_7 \) are closed and input of comparator becomes

\[
V_{inc} = A_{SDS} \begin{bmatrix} (V_x + \frac{3V_{ref}}{4} - V_i^-) \\
(V_x + \frac{V_{ref}}{4} - V_i^+) \end{bmatrix} 
= A_{SDS} \left[ -\frac{V_{ref}}{2} - (V_i^+ - V_i^-) \right] \] (6)

This process is continued until the last bit is determined.

To reduce the number of switches and resistors, we
can use an asymmetric method to resolve the last three bits (this method with two more unit capacitors was used in [3]), shown in Fig. 3. In this method, to determine B7 (seventh bit) switches S23 and S28 are opened and S21 and S26 are closed. Hence, the input voltage of the comparator changes as much as

$$\frac{C}{8} + \frac{C}{s} \times \frac{8}{64} V_{\text{ref}} = A_{S_{DS}} \times \frac{V_{\text{ref}}}{64}$$  \hspace{1cm} (7)$$

To resolve B8, only switches of the left side of SDS are changed. Depending on whether B7 is 1 or 0, S29 or S23 are closed and S21 is opened. The change of the comparator input becomes

$$\frac{C}{8} + \frac{C}{s} \times \frac{4}{64} V_{\text{ref}} = A_{S_{DS}} \times \frac{V_{\text{ref}}}{128}$$  \hspace{1cm} (8)$$

Next, to determine B9, switches of the right hand side are changed. In this case, S26 is opened and S25 or S27 is closed depending on whether B8 is 1 or 0. Thus, the change in the input voltage of the comparator becomes:

$$\frac{C}{8} + \frac{C}{s} \times \frac{2}{64} V_{\text{ref}} = A_{S_{DS}} \times \frac{V_{\text{ref}}}{256}$$  \hspace{1cm} (9)$$

At last to detect the 10th bit, switches of the left side are changed. In this case, state of switches depends on both B8 and B9. Variation of the comparator input becomes

$$\frac{C}{8} + \frac{C}{s} \times \frac{1}{64} V_{\text{ref}} = A_{S_{DS}} \times \frac{V_{\text{ref}}}{512}$$  \hspace{1cm} (10)$$

In the proposed architecture, the maximum common mode variation of the comparator input, due to asymmetric switching for the three LSBs is

$$\frac{1}{2} \left[ \frac{5}{64} V_{\text{ref}} + \frac{2}{64} V_{\text{ref}} \right] \times \frac{C}{8} + \frac{C}{s} \times \frac{1}{1024} V_{\text{ref}} \approx 2.7 \text{ mV}$$  \hspace{1cm} (11)$$

This small variation doesn’t cause any problem for the ADC’s performance. (Notice that any common-mode variation injection to differential signal is dramatically attenuated by CMRR of the comparator which is more than 30 dB in the worst case. Hence any possible error due to that is less than 0.1 LSB and is completely negligible). Therefore, this architecture not only improves DAC loss, but also requires only 45 switches, 64 resistors, and 20 unit capacitors for a fully differential version. In this architecture the same capacitor C is used to detect the first three bits (MSBs). Since there are seven remaining bits to be detected by other capacitors (C/8s), thus capacitor matching required is seven bits (in the order of 0.8%). Hence the unit poly-poly capacitor size (C/8) was determined to be 0.2 pF, which has a standard deviation of $\sigma = 0.5%$ [4]. Table 1 shows gain and number of unit capacitors, unit resistors, and switches in this work and two other works.

### Table 1. Table of comparison of fully differential 10-bit SDS.

<table>
<thead>
<tr>
<th></th>
<th>Gain</th>
<th>Unit C</th>
<th>Unit R.</th>
<th>Switches</th>
</tr>
</thead>
<tbody>
<tr>
<td>This Work</td>
<td>0.78</td>
<td>20</td>
<td>64</td>
<td>45</td>
</tr>
<tr>
<td>[2]</td>
<td>0.35</td>
<td>26</td>
<td>128</td>
<td>42</td>
</tr>
<tr>
<td>[3]</td>
<td>0.65</td>
<td>22</td>
<td>64</td>
<td>41</td>
</tr>
</tbody>
</table>

The resistor string is made up of a one-piece long silicon, with contacts equally spaced on it to create resistor pieces. The poly width is 9 $\mu$m to achieve 10-bit linearity. The length of each piece is 17.4 $\mu$m, set by 50 Ohm/piece resistance, for low power consumption. Notice that polysilicon resistors do not suffer from the nonlinearity of otherwise diffusion resistors. The method is quite effective and we have achieved better than 11-bit linearity in many different processes.

### 4. Comparator Design

The maximum input swing of the ADC is 1 V, so LSB is 1 mV. The designed comparator should detect:

$$1/2 \text{LSB} \times A_{S_{DS}} = 0.5 \text{ m} \times 0.78 = 390 \mu\text{V}$$  \hspace{1cm} (12)$$

Thus, the comparator should have an input referred offset less than 390 $\mu$V. A good choice to achieve this low input referred offset is shown in Fig. 4 [5]. Here, offsets of all stages, preamplifier and latch, are cancelled.

The drawback of it, however, is that in preamplification mode the latch (Gm2) stays idle and consumes power. In order to save power consumption of the latch in preamplification mode and use this power to increase speed, a new method was developed [6]. Figure 5 shows the new comparator. By reducing the output resistance/gain of the preamplifier stage, the comparator was speeded up. This became possible since the second stage helps overall gain in the preamplification mode. In Fig. 5(a) comparator is in offset cancellation mode. In the proposed architecture offset cancellation is applied to preamplifier (first gain stage), buffers and the latch (second gain stage), hence, a small input referred offset was achieved. In this architecture the first
The gain stage and the buffers use Output Offset Storage method [5], while the second gain stage, with a relatively high gain, employs Input Offset Storage method. For accurate offset cancellation Input Offset Storage method requires a high gain. The comparator in preamplification and latch modes are shown in Figs. 5(b) and 5(c), respectively. As these figures show, $G_{m2}$ is used for amplification in the preamplification mode, and as a positive feedback loop in latch mode.

The difference of the two comparators is that in Fig. 4 the gain stage of latch is outside of the signal path (input to output) in the preamplification mode (inputs of $G_{m2}$ are grounded), while in Fig. 5(b) it is part of signal path and enhances comparator gain.

Fig. 5 Proposed comparator in (a) offset cancellation mode, (b) preamplification mode, and (c) latch mode.

The second stage amplifier, $A_2$, is implemented by $M_5$ and $M_6$ differential pair with active loads $M_7$ and $M_8$. $M_9$ and $M_{10}$ set output common mode, and at the same time reset $A_2$ before the beginning of each amplification mode (these switches are ON by narrow reset pulses at the end of each latch mode). Use of $M_9$ and $M_{10}$ in this manner maintains high gain of the stage during amplification, and increases speed by fast recovery from the previous large output differential levels, while eliminates parasitic capacitances due to extra reset switch. $M_{12}$ creates a DC shift down from $V_{dd}$, which lets output common mode be set at a lower voltage (about $V_{dd}/2$). Due to the reduced output common mode voltage, ON resistance of NMOS switches are reduced and speed is enhanced.

Since offset cancellation is applied to all stages, residual offset is primarily due to the low gain of the second stage and mismatch of $S_{5c}$ and $S_{6c}$. Mismatch of $S_{7c}$–$S_{10c}$ is not important because when $S_{7c}$ ($S_{9c}$) is opened $S_{5c}$ ($S_{10c}$) is closed. Hence charge injection of one ($S_{7c}$, $S_{9c}$) is absorbed by the other ($S_{8c}$, $S_{10c}$). Moreover, effect of any residue from this charge injection, due to large signal levels at the inputs of $M_3$, $M_4$, is completely negligible. Residual offset at nodes A and B is:

$$V_{osAB} = \frac{\Delta Q}{C_{of}} + \frac{V_{os2}}{1 + A_2} \tag{13}$$

where $\Delta Q$ is the channel charge mismatch of $S_{5c}$ and $S_{6c}$ when they are ON, $C_{of}$ represents the offset storage capacitors, and $V_{os2}$ and $A_2$ are the input offset and gain of the second stage respectively. So input referred offset is:

$$V_{oin} = \frac{V_{osAB}}{G_{m1}R_{L12}} \tag{14}$$

where $G_{m1}R_{L12}$ is the gain of the first stage. In simulations, 10 mV offsets are applied intentionally to the input of the second stage, input of the first stage, and input of transistors $M_3$ and $M_4$. In this design $A_2$ is 40. As Eq. (13) shows, in order to reduce the residual offset at nodes A and B, $A_2$ should be as large as possible. Higher gain requires either higher output impedance by reducing the bias current (a lower speed), or higher input transconductance by enlarging input transistors (higher input capacitance). Note that switches $S_{c1}$–$S_{c4}$ are used only to test the comparator and they are not used in the comparator blocks of Figs. 2 and 3.

5. Simulation Results of Comparator

After extraction of SPICE file from layout, worst-case operation of the comparator has been tested. In the first cycle, Fig. 7, a large positive input (200 mV) and in the second cycle a very small negative input ($-350 \mu V$), and inversely in
Fig. 6  Transistor-level circuit of the used comparator.

Fig. 7  Waveforms of (a) $\phi_1$, (b) $\phi_2$, (c) reset, (d) input of the comparator, outputs of the comparator (e) before the inverters, (f) after the inverters.
the third cycle a −200 mV and in the fourth cycle a 350 µV have been applied to the input of comparator.

In order to cause a real channel charge mismatch, ∆Q, a 0.05 µm mismatch has been applied to W of switches S_5 and S_6, intentionally. In this design A_1 is 2. Transistors M_3 and M_4 are larger than minimum size to reduce their mismatch. Using Eq. (13) and Eq. (14) and due to limited gain, C_{of} was chosen 0.55 pF to minimize offset. Device sizes in the comparator are given in Table 2.

As mentioned before, 10 mV offsets and 0.05 µm mismatch are applied intentionally in the SS (worst parameter set) simulations. Figures 7(a) and 7(b) depict \( \phi_{1c} \) and \( \phi_{2c} \). Figure 7(c) shows the reset signal. Input and output waveforms are given in Fig. 7(d) and Fig. 7(e) respectively. To bring the outputs to full CMOS levels two inverters have been used at the comparator outputs, Fig. 10. Figure 7(f) shows the inverters’ outputs. The same test with the same conditions in 100°C has been done. The resulted outputs of the comparator are given in Fig. 8.

### 6. Setting of ADC

The designed ADC has three modes from time constant point of view, sampling mode, preamplification mode while detecting the first three bits, and preamplification mode while detecting the last seven bits. In the sampling mode we have the largest time constant for both DAC and comparator. Since the respective transients occur simultaneously, the transient times are none aggregate. Settling times of DAC and comparator in the sampling mode are 7 nSec and 24 nSec, respectively. Since two clock periods have been dedicated for sampling mode (320 nsec), this ensures better than 10-bit settling. During clock cycles in which the first three bits are detected, half circuit model of SDS is as shown...
in Fig. 9. The three poles’ time constants can be calculated as

\[ \tau_{2-SDS} = (16R + R_s) \left( C_{p1} + \frac{C}{\frac{1}{2}C + C_x} \right) \]  
\[ \tau_{2-comp1} \approx \left( \frac{1}{g_{m3}} \right) \left( C_d + C_s + C_{BS} + \frac{C_{of} \times C_{in2}}{C_{of} + C_{in2}} \right) \]  
\[ \tau_{2-comp2} = \left( \frac{R_s}{R_s + R_{S5}} \right) \left( C_{d5} + C_{d7} + C_{ds} + C_{d-50} \right) \]

Here, \( C_{p1} \) is the total parasitic capacitance at node x, including wiring, diffusion and bottom plate capacitance of C. It amounts to 630 fF. \( R_s \), the DAC switch’s resistance is 2.8 kΩ. Time constants obtained from the above equations are 3.5 nSec, 2.1 nSec, and 14.3 nSec, respectively. And the total time constant, which determines settling, dominated by \( \tau_{2-comp2} \) becomes 15 nSec. Similarly, to detect the last seven bits, time constants of Eq. (16) and Eq. (17) remain the same, while time constant of Eq. (15) changes to Eq. (18).
Table 3  Boolean expressions of switches gate signals.

| S_1 | ϕ_1 + ϕ_2 | S_15 | b_3 (ϕ_7 + b_3b_4ϕ_{14}) |
| S_2 | b_1b_2 (ϕ_5 + b_3ϕ_{16}) | S_16 | b_3b_5 (ϕ_5 + b_3ϕ_{16}) |
| S_3 | b_1 (ϕ_4 + b_2b_5ϕ_{16}) | S_17 | b_3b_5b_6ϕ_{14} + ϕ_{14} |
| S_4 | b_1b_2 (ϕ_5 + b_3ϕ_{16}) | S_18 | b_3b_5b_{12} |
| S_5 | b_4 + b_3b_5ϕ_{16} | S_19 | b_1 (ϕ_{10} + ϕ_{11}) |
| S_6 | b_1b_2 (ϕ_5 + b_3ϕ_{16}) | S_20 | b_3b_5b_{12} |
| S_7 | b_1 (ϕ_4 + b_2b_5ϕ_{16}) | S_21 | ϕ_9 |
| S_8 | b_1b_2 (ϕ_5 + b_3ϕ_{16}) | S_22 | b_3b_5b_{12} |
| S_9 | b_1b_2b_5ϕ_{16} | S_23 | b_3 (ϕ_{10} + ϕ_{11}) + ϕ_{11} |
| S_{10} | b_3b_5 (ϕ_5 + b_3ϕ_{16}) | S_24 | b_3b_5b_{12} |
| S_{11} | b_4 (ϕ_7 + b_3b_4ϕ_{14}) | S_25 | b_4 (ϕ_7 + ϕ_{12}) |
| S_{12} | b_3b_5 (ϕ_5 + b_3ϕ_{16}) | S_26 | ϕ_9 + ϕ_{10} |
| S_{13} | b_4b_5b_6ϕ_{14} | S_27 | b_4 (ϕ_{11} + ϕ_{12}) |
| S_{14} | b_3b_5 (ϕ_5 + b_3ϕ_{16}) | S_28 | ϕ_{11} |

\[ \tau_{3-SDS} = (16R + R_{r13,21,26}) \times \left[ C_p2 + \frac{C}{8}(C + \frac{C}{8} + C_s) \right] \times \left[ \frac{C}{8} + \left( \frac{C}{8} + C_s \right) \right] \]  

(18)

Hence, the total time constant is slightly reduced to 14.6 nSec. In Eq. (18) \( C_p2 \) is the total parasitic capacitance at bottom plate of C/8. Notice that to detect each bit one clock cycle (160 nsec) has been allocated for comparator operation. of which 120 nSec is for preamplification, which ensures 11-bit accuracy. The remaining 40 nSec is for latch. Figure 11 shows the simulation results of ADC, for three complete conversion cycles and for three different input signal levels. In this simulation extracted parasitic capacitances at bottom plate of capacitors have been used in the netlist. The differential signal at bottom plate of capacitors C and C/8 are shown in Fig. 11(a)–(c). The differential input and single ended output of comparator are given in Fig. 11(d) and (e) respectively. Notice Fig. 11(d) clearly shows that there are two clock cycles, for offset cancellation and for input sampling, at the beginning of each conversion cycle where the comparator input is zero. Then when detection of bits starts in the third clock cycle, for the first bit there is the largest comparator input. As successive-approximation proceeds, the comparator input approaches zero indicating bits and feeding them back to the internal DAC. Figure 11(f) shows only control signals of S_1–S_9 to reduce the figure’s complexity.

### 7. Control Logic

Figure 10 shows registers of ADC and required clock signals. Outputs of registers have been used to control switches of SDS. Boolean expressions for the control signals of SDS switches are given in Table 3.

Since this ADC is a low speed one, in order to reduce the power consumption and switching activity of the digital circuits, complex CMOS logic, instead of many two input gates (NAND or NOR) were used to realize the Boolean functions.

### 8. Floor Plan and Power Consumption

The floor plan of the chip is shown in Fig. 12. Area of ADC is estimated by subtracting the area of the switched capacitor amplifier, another block required for the larger system which includes ADC, from the whole die area.

The unit resistors are laid out as one piece long string. For better matching, the unit capacitors that make C are laid out around the two unit capacitors. To isolate the capacitors from the substrate noise, they are put over a well, connected to V_{dd}. The power consumption of the resistor string, the comparator, and the digital circuitry are given in Table 4. High value of the unit resistors and the efficient use of power in the comparator are the main factors for low power consumption of this ADC. It should be mentioned that the power consumption required for the reference voltage generator is not considered in power consumption calculations.

### 9. Complete ADC Simulation

This ADC was aimed to operate at a sampling rate of 500 KHz. However, for ease of simulations, we chose a clock period of 160 nSec (less than 167 nSec for 500 KHz sampling). To avoid long simulations, while accurately estimating output spectrum, we selected a full input range signal at a frequency of

\[ f_{in} = \frac{3f_i}{32} = \frac{3}{12 \times 160n} = 48.828125 \text{ KHz} \]  

(19)

This allowed the input signal to land exactly on the third bin of a 32-bit output spectrum. Hence only 32 samples taken.
from 3 complete sinusoidal input signal cycles were used for a 32-point FFT. Notice that this exact relation between clock frequency and input signal frequency is only possible in simulations (not in measurements), which drastically reduces FFT points and simulation time. In Eq. (19) the factor 3 indicates the bin number of the input signal. In order to prevent possible folding of high frequency harmonics on each other or the main component, the input signal bin number should be an odd one. Figure 13 shows the result of FFT. It shows the largest harmonic (3rd) is about $-67$ dB below the main component, which satisfies the requirement for a 10-bit ADC.

To determine $\text{INL}_{\text{max}}$, a ramp was applied to the input of ADC. Moreover, an offset of $10$ mV was applied to the input differential pair of comparator. The INL diagram, Fig. 14, reflects the worst combination of all adverse effects by mismatches which is less than $\pm 1$ LSB. The results were obtained using HSPICE and MATLAB.

### 10. Comparison with Other Works

The aim of this work was to design a reduced power and chip area successive-approximation ADC. Table 5 shows the results and comparison with three other works. In all aspects the designed ADC shows improvement, specially when it is considered that a much slower process was used than those of previously reported works.

### 11. Conclusions

In the designed ADC both the internal DAC and the comparator have been improved. Partially asymmetric operation of DAC switches not only has reduced the loss of DAC, but also has lowered the number of unit capacitors and resistors. In order to reduce the input referred offset of the comparator, offset cancellation was applied to not only the preamplifier, but also to the latch. The improvements caused effective reduction of chip area and power consumption. The layout of ADC, drawn by MAGIC, takes on effective die area of ADC only $0.95$ mm$^2$. The HSPICE transient simulations showed that the power consumption of the complete ADC is only $0.6$ mW. Hence a much less power and area was required while a much slower process was used, without compromising speed, compared to other reported works.

### References

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