A low power, reconfigurable IR-UWB system

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Abstract—Impulse-Radio-UWB is the ideal air interface for low power wireless applications especially when they require ranging capabilities. This paper presents a complete UWB transceiver system, including acquisition and ranging protocols. The system is fully reconfigurable in terms of bandwidth, data rate, processing gain, acquisition protocol and ranging accuracy, in order to fulfill the needs of the application with minimal energy consumption. The complete system is demonstrated by measurements on an IR-UWB transceiver platform built around 3 fully integrated CMOS chips. The transceiver system achieves a data rate up to 50Mbps and a ranging error with a root mean squared error of less than 10cm while consuming 31.7mW. The IC implementation allows to fully validate the power/flexibility trade-off that can be achieved with integrated solutions.

I. INTRODUCTION

Low power, low-data-rate wireless communication is the key enabling technology for a wide range of sensor network applications [1]. This growing market continuously stimulates the research for energy-efficient radio systems. An interesting air interface candidate is Impulse Radio Ultra WideBand (IR-UWB) [2], [3]) communication, where data is modulated on short, wideband pulses. This wideband communication technique offers many benefits in comparison to classical narrow-band systems. The duty-cycled nature of the pulses can be exploited in the design of an ultra-low power transceiver frontend [4]. Also the large robustness of UWB against multipath environments and multi-user interference is an advantage for sensor network applications. Finally the short duration of the pulses allows very accurate time-of-arrival (TOA) estimation [5]. This enables accurate ranging, often required in the targeted application domains.

This paper presents a complete energy-efficient IR-UWB transceiver system, including acquisition and ranging protocols (Section II). The system is made reconfigurable to avoid a conservative, worst-case design, while still covering the wide range of possible data rates, distances and channel conditions. This flexibility allows the system to minimize the energy consumption, while adapting to the requirements of the application and the environment.

The performance of the complete system is finally demonstrated by real life measurements on a complete IR-UWB transceiver platform, built around 3 fully integrated CMOS chips (Section III). The measurements presented in Section IV illustrate the possible power vs. performance trade-offs that can be achieved on a real system when data rate, ranging accuracy, processing gain and choice of acquisition protocol are varied. Measured power figures are given.

Section V discusses the system’s compatibility with the latest IEEE802.15.4a standard and Section VI concludes the paper.

II. BPSK IR-UWB SYSTEM

A. IR-UWB air interface

Data can be modulated onto a stream of IR-UWB pulses by on-off keying (OOK), pulse position modulation (PPM) or phase shift keying (PSK). Among those, PSK is known to offer better theoretical SNR performances ([6]). Moreover PSK also allows to track clock-offset between receiver and transmitter, by scanning the rotation of the incoming quadrature signals in the constellation diagram. This clock-offset compensation loop eliminates the need for a power-hungry early-late detection circuit. Binary phase shift keying (BPSK) is therefore selected as modulation scheme.

To increase the link budget of the communication, multiple pulses per bit are used. Each data is correlated with a pseudo noise (PN) spreading code of length Np in the transmitter. The spread Np pulses are then decorrelated in the receiver. The Federal Communication Commission (FCC) approved commercial UWB operation in the 3.1-10.6GHz band [2]. To avoid the strong WLAN interference at 5GHz the proposed system will however be restricted to the 3.1-5GHz band.

B. Quadrature analog correlating receiver

Over the last decade, many different UWB receiver architectures were presented in literature. They mainly differ by the position of the ADCs and in the generation of the pulse correlation template. A recent study [7] has compared the five most promising architectures in terms of their energy consumption per useful received bit (EPUB). The Quadrature Analog Correlating (QAC) receiver [8] appeared as the optimum in terms of power/performance trade-off.
The very low power consumption of the QAC architecture is obtained by performing the pulse correlation in the analog domain such as to reduce the speed requirements of the ADC and the digital front-end [8]. Figure 1 shows the QAC receiver topology. The analog pulse correlation is realized by a quadrature downconversion followed by a windowed integration. The window length is typically around $2/BW$, $BW$ being the pulse bandwidth. The ADC samples the correlation value once every pulse period and the result is processed in the digital domain. The direct-downconversion must be performed in 2 quadrature paths in order to collect all received pulse energy and to allow clock offset tracking. The despreading of the pulse sequence with the PN code and the clock-offset compensation are done in the digital domain.

**C. Data acquisition**

An acquisition phase precedes the data detection. Based on a train of known preamble pulses, the receiver has to find the best analog integration window position and align the locally generated PN spreading code in the digital domain with the incoming data samples. In the remainder of this paragraph two different acquisition protocols will be analyzed. The most straightforward acquisition protocol, the PN-based acquisition, scans all possible combinations of window position and code alignment. The protocol is depicted in figure 2(a). For every possible position of the analog integration window, $N_s$ code alignments will have to be checked by a correlation between the incoming data and the locally generated PN code (=PN correlation). The number of required PN correlations, $N_{PN}(PN)$, can however become very large for longer code lengths or pulse periods:

$$N_{PN}(PN) = N_s \cdot \left[ \frac{T_p}{T_w/2} \right] \text{ PN corr. of length } N_s, \quad (1)$$

where $T_p$ is the pulse period and $T_w$ the window length and assuming that the window is shifted in steps of $T_w/2$. The number of PN correlations that can be executed in parallel is limited by the number, $C_{PN}$, of parallel correlators present in the digital back-end. As a result, the time, $T_{acq}(PN)$ necessary for one PN-based acquisition is:

$$T_{acq}(PN) = \left( \frac{T_p}{T_w/2} \right) \cdot \left[ \frac{N_s}{C_{PN}} \right] \cdot N_s \cdot T_p \quad (2)$$

The second acquisition protocol, the AC-based acquisition uses, in a first step, energy detection based on autocorrelations to find the correct window position with a minimum of operations. One autocorrelation is done for every possible window position. Next, the window is fixed to the best position and $N_s$ PN correlations are executed to find the correct code alignment. As represented in figure 2(b), the required number of operations will be lower than for the PN-based acquisition:

$$N_{AC}(AC) = \left[ \frac{T_p}{T_w/2} \right] \text{ AC corr. of length } N_s, \quad (3)$$

$$N_{PN}(AC) = N_s \quad \text{ PN corr. of length } N_s, \quad (4)$$

The total acquisition time for one AC-based acquisition equals:

$$T_{acq}(AC) = \left( 2 \cdot \left[ \frac{T_p}{T_w/2} \right] \right) + \left[ \frac{N_s}{C_{PN}} \right] \cdot N_s \cdot T_p \quad (5)$$

The total receiver energy consumption during acquisition, $E_{acqRx}$, is a function of the acquisition time and the necessary number of correlations:

$$E_{acqRx} = \alpha \cdot T_{acq} + \beta \cdot N_{AC} \cdot N_s + \gamma \cdot N_{PN} \cdot N_s \quad (6)$$

from which the parameter values $\alpha$, $\beta$ and $\gamma$ can easily be derived from measurements (see section III-C and III-D). Formulae (1) to (6) prove that a significant acquisition energy saving can be achieved by selecting the right acquisition algorithm depending on the system parameters. This will also be proved in the measurements of Section IV. The acquisition protocol should hence be kept flexible in the receiver design. The performance of the AC-based acquisition will however be worse than the PN-based acquisition. While a PN correlation of length $N_s$ realizes a processing gain with a factor $N_s$, an autocorrelation of length $N_s$ on the other hand results in an output signal-to-noise ($SNR_{out}$) ratio of:

$$SNR_{out}(AC) = \frac{S_{out}}{N_{out}} = N_s \cdot \frac{S_{in}^2}{2 \cdot S_{in}^2 \cdot N_{in} + N_{in}^2} \quad (7)$$

with $S_{in}$ and $N_{in}$ the signal power and noise power at the correlator entrance respectively. This loss in comparison to the
PN-based acquisition can be large in low SNR environments, and should be taken into account in the selection of the acquisition protocol.

D. Synchronization and CO tracking

Clock offset (CO) between transmitter and receiver can largely degrade the system performance and cause loss of data. The quadrature incoming data samples of the digital back-end will be affected by a rotation in the constellation diagram due to clock offset. Secondly clock frequency mismatch between transmitter and receiver will cause the data pulses to shift gradually out of the receiver’s correlation window. As a result, it is very important to estimate the clock offset and compensate for it. Therefore a digital tracking loop continuously tracks the clock offset [8]. This offset monitoring allows to cancel the rotation of the data in the constellation diagram and shift the integration window. The tracking loop is initialized with a first estimation of the clock offset, computed at the end of the acquisition phase [8].

E. Ranging

In many sensor network applications the exact physical location of the transmitter is crucial information. In IR-UWB locationing comes almost for free via a time-of-arrival (TOA) measurement. After acquisition, the position of the analog integration window, gives the TOA information of the pulse with an accuracy of $T_w/2$. Depending on the ranging accuracy requirement, the coarse window positioning during acquisition will have to be followed by a finer granularity search. The ranging protocol used during this search is depicted in figure 2(c). It reduces the window size to $T_w/X$ and scans $X$ window positions around the optimal position determined during acquisition. A finer accuracy can be obtained at the expense of power consumption (increased signal bandwidth) or acquisition time (increased $X$).

F. Required flexibility

Previous discussions revealed the need for flexibility knobs in an IR-UWB system. These allow to dynamically trade the systems performance for power consumption, acquisition time or data rate. Reconfigurability then allows the transceiver to operate over a wide range of application requirements, channel conditions and application domains. It is however of crucial importance to keep the power penalty due to the introduction of flexibility as low as possible.

To be flexible in terms of data rate, communication distance, channel conditions, processing gain and ranging accuracy, the system should have the flexibility knobs listed in table I. The table also mentions the range over which the parameters can vary in the transceiver platform presented in this paper.

III. COMMUNICATION PLATFORM USING FULLY INTEGRATED CHIPS IN CMOS

The system proposed in Section II has been implemented in different CMOS ICs that together form a complete communication platform. It consists of three fully integrated CMOS chips: a transmitter (Tx), a receiver front-end (Rx-FE) and a receiver back-end (Rx-BE). Two FPGAs connect the transmitter and the receiver respectively with a PC to steer the measurement and process the results. The complete setup can be seen in figure 3. The following paragraphs briefly describe the different ICs of the platform.

A. Duty cycled IR-UWB transmitter

The transmitter has been realized in a 90nm CMOS process and presented in [4]. It consists of two main parts: an RF modulator and a local oscillator (LO) generator. In order to duty-cycle the system at the pulse repetition rate, a novel PLL concept, the phase-aligned frequency-locked loop, has been used. It allows the LO generator to operate only during the pulse transmission period and therefore save power between two pulse transmissions. The modulator is a digital multiplier that modulates the LO with a predefined pulse shape whose phase depends on the data value. The digital approach in the design of the modulator results in a fully dynamic system with no static bias current. Pulses with a center frequency from 3.1GHz up to 10GHz can be created. The power consumption of the transmitter is below 1mW from a 1V supply.

B. QAC receiver front-end

The QAC receiver front-end has been realized in a 180nm CMOS process and presented in [9]. It is based on a classical direct-downconversion architecture (LNA and quadrature mixer) for the RF part. The two quadrature analog baseband sections are built from a cascade of a 3rd order active filter with variable gain and bandwidth, a windowed integrator for the analog correlation and a fully dynamic 4 bits flash ADC. The various clock signals for the integration window and ADC sampling are created on-chip with a timing generator.
A delay line has also been implemented on-chip to align the clock signal to the received pulse stream. This delay-line is steered by the synchronization algorithm. The receiver can downconvert pulses in the 3.1GHz-5GHz band with different bandwidths from 500MHz to 2GHz thanks to a variable bandwidth baseband filter. The integration window length can also be adapted to the pulse bandwidth, between 700ps up to 4.2ns. The power consumption of the receiver is 28.8mW from a 1.8V supply.

C. Reconfigurable receiver back-end

The main tasks of the receiver back-end are threefold: 1. Control the analog front-end, by setting window start and stop times and the AGC value; 2. Execute an acquisition protocol to find the optimum window placement and code alignment, possibly followed by a ranging protocol; 3. Decorrelate the incoming samples during data detect and track and compensate for clock offset. The back-end was made reconfigurable to meet the flexibility requirements of table I. The energy overhead due to this flexibility is kept low by using distributed programmable controllers, allowing to gate clocks and power supplies with a very fine granularity. The chip is implemented in 130nm standard cell CMOS technology and consumes 1.4mW during data detect and less than 3.5mW during acquisition [10]. It contains 33 parallel PN correlators, consuming 4.7pJ/pulse ($\gamma$), while an autocorrelation consumes 12pJ/pulse ($\beta$).

D. Power consumption partitioning

Table II gives the distribution of the measured power consumption of the system. It is clear that almost all the power goes to the receiver front-end. The power consumption of this block can however be reduced drastically by duty-cycling the front-end. This principle has already been successfully applied in the transmitter implementation and proves to reduce the power consumption with at least a factor of 6 [4].

| Table II POWER DISTRIBUTION

<table>
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<th></th>
<th>technology</th>
<th>av. power cons.</th>
<th>power fraction</th>
</tr>
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<tbody>
<tr>
<td>transmitter</td>
<td>90nm CMOS</td>
<td>1.0mW</td>
<td>3.2%</td>
</tr>
<tr>
<td>receiver front-end</td>
<td>180nm CMOS</td>
<td>28.8mW</td>
<td>90.8%</td>
</tr>
<tr>
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</tr>
<tr>
<td>total</td>
<td></td>
<td>31.7mW</td>
<td>100%</td>
</tr>
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</table>

IV. MEASUREMENT RESULTS

This section demonstrates the performance of the proposed IR-UWB system using the transceiver platform. The possible energy-performance trade-offs are explored by tuning the introduced performance knobs. Since UWB communication makes use of already allocated frequency bands, narrowband interferers are usually the main noise source, dominating over thermal Gaussian noise. All measurements will hence be plotted in function of the signal to interference ratio (SIR) measured at the receiver entrance. The measurement results are expressed in terms of the packet acceptance ratio (PAR) of the communication link. Packets with a length of 500 bits are used, preceded by a preamble of known (all “1”-) bits. The length of the preamble depends on the acquisition algorithm used and is computed using formulae (2) and (5). A packet is accepted, when the acquisition is successful and all payload bits are received correctly. The wireless link between transmitter and receiver is emulated by a wire followed by an attenuator. The interferer is injected in the link via a wideband coupler. The pulse power at the receiver entrance was fixed to -55dBm. 600MHz bandwidth pulses are used. The pulse repetition rate is flexible, but fixed in these measurements to 33MHz. An analog integration window length of 3.2nsec is used, except for the ranging measurements, where this parameter is varied.

A. Performance measurements

Figure 4 shows the system performance in the presence of an in-band (at 50 and 150MHz offset of the center frequency) and an out-of-band interferer (at 350MHz offset). As can be seen, the performance of the receiver is very sensitive to the interferer frequency. This again justifies the need for a band switching flexibility when a strong interferer is detected.

B. Flexibility measurements

Moving the communication band away from strong interferers is not the only way to improve the system performance. Increasing $N_s$, the number of pulses per bit, results in a larger processing gain and hence larger resistance against interferers, as can be seen in figure 5(a). This is however at the cost of an increased energy consumption per bit in the transmitter and receiver (figure 5(b)).
is limited by the pulse duration to 25 cm for a 600 MHz and be applied on a standard compliant system. It would simply is not designed towards the new IEEE 802.15.4a [11] standard.

As described in section II-C, the acquisition energy consumption can be minimized by selecting the right acquisition algorithm. Figure 6(b), which shows the measured energy consumption during one acquisition, demonstrates that power savings up to 70% can be achieved by tuning the acquisition algorithm flexibility knob. The performance of AC-based acquisition algorithm is however worse then for the PN-based protocol. The amount of loss depends on the SNR at the back-end entrance as can be seen in formula (7). Figure 6(a) shows the measured performance result for 31 pulses per bit. The loss is 6 dB as expected from formula (7) \( SNR_{\text{acq}} \approx -5 dB \). These figures show that AC-based outperforms PN-based acquisition in high SNR environments when \( N_s > 60 \).

Finally the flexibility of the chip can be exploited to adapt the ranging accuracy depending on the needs of the application. Parameters to adapt are the granularity of the window positioning during the search phase, the number of pulses per bit (processing gain) and the pulse bandwidth. Figure 7(a) shows the root mean squared error (rmse) of the measured ranging accuracy in function of the granularity of the window positioning step and the pulse bandwidth. As can be seen, the performance increases for larger \( N_s \) and smaller positioning steps. This comes with an increased energy consumption per ranging operation, as can be seen in figure 7(b). The accuracy is limited by the pulse duration to 25 cm for a 600 MHz and 10 cm for a 1600 MHz pulse.

V. FUTURE WORK ON STANDARD COMPLIANCE

The receiver of the IR-UWB system proposed in this paper is not designed towards the new IEEE 802.15.4a [11] standard. However, nothing prevents the above described concepts to be applied on a standard compliant system. It would simply require some small architectural modifications. The 802.15.4a preamble sequence uses equidistant pulses in time, which is identical to the air interface used in the current transceiver system and does not pose any problem. The payload however contains bursts of encoded pulses followed by a long silence period. They can be correctly detected by introducing an additional mixer before the windowed integrator in the analog front-end. This mixer multiplies the incoming burst with its spreading code in the analog domain. Next, an integration over the complete burst is done, and finally the result is sampled by the ADCs once every burst. The front-end power consumption will increase slightly due the additional baseband mixer, but the ADCs and digital back-end will be able to work at a lower rate.

VI. CONCLUSION

This paper presented a complete solution for low power communication and ranging. A QAC IR-UWB system is proposed together with the acquisition and ranging protocols. The system contains several flexibility knobs to optimally adapt to the needs from the environment and the application. The system is demonstrated by real measurements on a transceiver platform, built around 3 fully integrated CMOS ICs. The measurements prove the performance of the proposed system and show the possible trade-offs in terms of data rate, processing gain, acquisition protocols and ranging accuracy.

ACKNOWLEDGMENT

This work was partially supported by Imec-NL (Holst center).

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