Abstract—This paper is concerned with the time-domain simulation of circuits including noise sources. In general, when a circuit admits a steady-state solution, small signal analyses are used to determine noise effects. There is a class of circuits (e.g., fractional PLLs based on ΔΣ modulators and forced oscillators) not admitting a steady-state solution with a period reasonable low multiple of the characteristic time scales of the circuit. In commercial analog simulators, time domain noise analyses have been implemented by “extending” linear multi-step integration methods or by introducing sampled versions of noise generators. Through a set of basic benchmark circuits, we show that these extensions are often affected by a relevant numerical noise floor hiding the effects of noise sources and drastically limiting the applicability of time domain noise analysis.

I. INTRODUCTION

The numerical determination of effects due to noise sources in electronic circuits has received a large interest in the last years. The most widely diffused approaches can be roughly divided in two distinct classes. Those in the first class assume that circuits admitting a periodic steady-state solution are initially noiseless and working in their steady-state condition. The effects due to noise sources are assumed to be additive and sum to the large-signal noise-free solution. The circuit is thus linearised along this orbit, noise sources are turned on and their effects summed to the large signal solution. The analysis referred to in literature as periodic noise analysis belongs to this class; it “remaps” the nonlinear behaviour of the circuit along its orbit to a time-varying periodic linear model [1]–[4]. Approaches belonging to the second class are used to perform noise analyses of circuits that “do not admit” a periodic steady-state working condition or, better, whose periodic steady-state condition cannot be determined with a reasonable numerical effort or that do not admit a time-varying periodic linear model. For example, a fractional phase lock loop (PLL), where the dividing fraction of the voltage controlled oscillator (VCO) signal is determined by exploiting the output of a ΔΣ modulator, admits, in principle, a periodic steady-state behaviour, since the output of ΔΣ repeats after a very long sequence. This sequence, the period of the input signal of the PLL, and that of the VCO can lead to a steady-state behaviour characterized by a so large working period that the shooting (SH) or the harmonic balance (HB) methods are inapplicable. In these cases the designer need to resort to time domain noise analyses.

In this framework, there are two main approaches to model and solve a noisy nonlinear system. One approach describes the model through stochastic differential algebraic equations (SDAES), with noise sources modelled as Wiener processes. As far as we know, in literature this approach has been applied only to very simple circuits composed of a very limited number of elements to demonstrate some peculiar aspects [5], [6]. The second approach is related with methods that rely on and basically extend the conventional integration algorithms (often linear multi-step ones [7], [8]) to solve nonlinear circuits driven by equivalent models of noise sources. Noise sources are modelled by random number generators with suitable spectral properties or by a battery of equivalent noise sources with proper magnitude, frequency and random phase. In both approaches, due to the nonlinear nature of circuits, the solution is usually determined by exploiting iterative methods such as, for example, the Newton one [8]. This means that the iterative method is stopped when the error in estimating the solution becomes less than a given threshold. Furthermore, the linear multi-step integration method uses a variable-length time step. This “warps” time and introduces errors in the solution. All these effects lead to solutions affected by errors. We refer to these errors as the noise floor of the simulator [9]. In this paper we consider simple benchmark circuits and show how the noise floor can easily hide the effects due to external noise sources, thus making useless the application of time domain noise analysis. The effects of noise floor are evidenced by using also two commercial simulators, ELDO by MENTOR GRAPHICS™ and SPECTRE by CADENCE™, largely adopted in industrial environments.

II. BASIC CONCEPTS

Consider a circuit described through the modified nodal analysis (MNA) formulation and modeled by the equation

\[
\begin{align*}
\dot{q}(x(t)) + f(x(t), y(t)) + u(t) &= 0 \\
\dot{h}(x(t), y(t), t) &= 0
\end{align*}
\]

where \(q(x(t)) : \mathbb{R}^S \rightarrow \mathbb{R}^S\) represents charge (flux) of capacitors (inductors), \(f(x(t), y(t)) : \mathbb{R}^{S+L} \rightarrow \mathbb{R}^S\) represents current (voltage) through (across) capacitors (inductors),
\( h(x(t), y(t), t) : \mathbb{R}^{S+L+1} \rightarrow \mathbb{R}^L \) are algebraic relationships between electrical variables, \( x(t) \in \mathbb{R}^S \) and \( y(t) \in \mathbb{R}^L \) are the unknowns and \( t \) is time. By means of an implicit linear multi-step integration method that approximates, at the \( t_{n+1} \) discrete time instant, the \( \mathcal{Q}(x(t_{n+1})) \) derivative as the weighted linear combination of the \( \mathcal{Q}(x(t_k)) \) samples at the \( n+1-r, \ldots, n+1 \) previous time instants, Eq. (1) is recast as the following nonlinear algebraic equation

\[
\begin{align*}
\sum_{k=n+1-r}^{n+1} c_k(h_{n+1})q(x_k) + f(x_{n+1}, y_{n+1}) + u_{n+1} &= 0 \\
h(x_{n+1}, y_{n+1}, t_{n+1}) &= 0
\end{align*}
\]

(2)

where \( x_n \equiv x(t_n) \) (the same applies to the other symbols), \( h_{n+1} = t_{n+1} - t_n \) is the variable integration time step and \( c_k(h_{n+1}) \) are the coefficients defined by the selected integration method \([7], [8]. \) Equation (2) is solved, for example, with the Newton iterative method, which leads to the iterate

\[
\begin{align*}
J_{n+1}^j &= \frac{\partial q}{\partial x_{n+1}^j} + \frac{\partial f}{\partial x_{n+1}^j} \\
\frac{\partial q}{\partial x_{n+1}^j} &= \frac{\partial f}{\partial x_{n+1}^j} \\
\frac{\partial q}{\partial y_{n+1}^j} &= \frac{\partial f}{\partial y_{n+1}^j} \\
\frac{\partial q}{\partial h} &= \frac{\partial f}{\partial h}
\end{align*}
\]

\[
\begin{bmatrix}
\delta x_{n+1}^j \\
\delta y_{n+1}^j \\
\delta h
\end{bmatrix} =
\begin{bmatrix}
\frac{\partial q}{\partial x_{n+1}^j} \\
\frac{\partial q}{\partial y_{n+1}^j} \\
\frac{\partial q}{\partial h}
\end{bmatrix}
\begin{bmatrix}
\delta x_{n+1}^j \\
\delta y_{n+1}^j \\
\delta h
\end{bmatrix}
\]

(3)

where \( j \) is the iteration index, \( J_{n+1}^j \) is the Jacobian matrix, \( \delta x_{n+1} \) and \( \delta y_{n+1} \) updating vectors, i.e. \( x_{n+1} = x_{n+1} + \delta x_{n+1} \) (the same holds for \( y_{n+1} \)), and \( \mathcal{T}_{n+1}^j, \mathcal{T}_{n+1}^j \) represent the residuals of the first and second equations in Eq. (2). At each instant \( t_{n+1} \), the Newton algorithm is stopped when the solution derived by Eqs. (2) and (3) is affected by errors. In particular it depends on the parameter \( h_{n+1} \), this means that, given the simulation time interval \( T = [t_b, t_e] \), the \( x(t_b), y(t_b) \) solutions change if different (non uniform) time grids are used \([9]. \) At each \( t_{n+1} \), Eq. (2) is approximated solved by the Newton method (3), thus \( x(t_b), y(t_b) \) fall in balls with radius determined by the chosen accuracy. These inaccuracies determine the noise floor of the simulator: if we assume for example that Eq. (1) models a noiseless oscillator, we expect that the spectrum of a component of \( x(t) \) shows discrete spikes at the fundamental and its multiples. Instead, this spectrum is not discrete, looking like that of a noisy oscillator. The noise floor impacts on the accuracy of time domain nonlinear noise analysis since if the effects due to noise are below the noise floor of the simulator they cannot be identified.

### III. Test circuits

We used some very simple benchmark circuits to test time noise analysis capabilities of our simulator PAN \(^1\) and of the commercial circuit simulators ELDO \(^\text{T M}\), Mentor Graphics \(^\text{T M}\) and SPECTRE \(^\text{T M}\) by Cadence \(^\text{T M}\). Details about the algorithm to perform time noise analysis of these commercial simulators can be found in \([10], [11]. \) We remark that to determine the noise floor we used these algorithms without turning on noise sources. The only cases where noise sources were turned on refer to the solutions of SDAEs.

#### A. Linear RC circuit

The schematic of the first and very simple benchmark circuit (referred to as \( \text{Lin} \)) is shown in Fig. 1(a), with \( Rb \) replaced by a short circuit. It is constituted by the connection in parallel of the constant independent current generator \( Ao = 1 \mu A, \) of the sinusoidal generator \( As \) that generates a current waveform of 1 \( \mu A \) amplitude at 500 MHz and of the 100 kΩ linear resistor. Since this is linear, resistive and described by a scalar equation in the MNA formulation, we expect that it is accurately solved by the Newton iterative method. We simulated this circuit with PAN in the time domain in the interval \( 0 \leq t \leq 10^{-4} [s], \) i.e. for 50000 periods of the \( Ao \) driving signal. We calculated the modulus (in dB) of the Fourier integrals of the \( x(t) \) voltage at the \( \pi \) node shown in Fig. 1(a) at the two frequencies \( f_1 = 500 \text{ MHz} \) and \( f_2 = 500 \text{ MHz} - 10 \text{ kHz}, \) i.e. at 10 kHz offset from the fundamental. The use of Fourier integrals is justified since waveforms are deterministic and periodic, being the circuit noiseless. The results are summarised in Table I.

#### Table I

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Lin</th>
<th>HLin</th>
<th>PAN</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_1 )</td>
<td>acc</td>
<td>( \text{Lin} )</td>
<td>case 1</td>
</tr>
<tr>
<td>( f_2 )</td>
<td>acc</td>
<td>( \text{Lin} )</td>
<td>( \text{Lin} )</td>
</tr>
<tr>
<td>Ao</td>
<td>20</td>
<td>52</td>
<td>52</td>
</tr>
<tr>
<td>As</td>
<td>227</td>
<td>-102</td>
<td>-93</td>
</tr>
</tbody>
</table>

\(^1\)Simulator PAN is available at the URL: http://brambilla.ws.dei.polimi.it.

We point out that the noise floor of PAN is around 200 dB below the signal level. This is because \( @f_1 \) the expected magnitude of the Fourier integral coefficient is 100 kΩ \( \times Ao \rightarrow -20 \text{ dB} \) (perfectly coherent with the result reported in the Table) and \( @f_2 \) it should tend to \( -\infty \text{ dB}. \)

We repeated the same simulation with the modified version of \( \text{Lin}, \) where the \( Rb \) nonlinear resistor is modelled by the \( w = Ao \times y^2 \) characteristic. This simple modification (referred to as \( \text{HLin} \)) forces the simulator to perform several iterations of the Newton algorithm to find a solution. We performed three types of simulations once more with PAN, one (acc) with
tightly converged tolerances of the Newton method (10^{-6} relative and 10^{-12} absolute error introduced in satisfying the Kirchhoff equations), one (1.1b, 10^{-3} relative and 10^{-6} absolute error) with large tolerances, and one with the nonlinear resistor replaced by a linear one with conductance of 2.18 μS (1.1n) and tightened tolerances. This last case evidences that the insertion in series of a linear component does not increase the noise floor of the simulator. Results are reported in Table I and evidence that the insertion in series of the resistor does not substantially modify the noise floor in the 1.1n case (since the Newton method converges in one iteration) but largely affects the other two acc and 1.1b results. The noise floor of the simulator increases and depends also and obviously on the accuracy in computing the solution.

B. The Van der Pol oscillator

The schematic of the third circuit used as benchmark to test the noise floor of the simulator is shown in Fig. 1(b). It is the celebrated Van der Pol oscillator. In order to "force" the use of the Newton method also when an explicit integration method is employed, we have split the \( N \) nonlinear element in the series connection of two \( N1 \) and \( N2 \) nonlinear elements (not shown in the figure). We have thus introduced the \( y \) extra "algebraic" unknown and node. The SDAE modeling the circuit is

\[
\begin{align*}
C_2 \dot{z} + w + 27 (z - y)^3 - 3 (z - y) + \sqrt{\eta(t)} &= 0 \\
L_2 \dot{w} - z &= 0 \\
9 \left[ (z - y)^3 - \frac{1}{3} y^3 \right] - z + \frac{1}{3} y &= 0
\end{align*}
\]

(4)

where \( \eta(t) \) is a white noise process and the current flowing through the nonlinear resistor \( N \) is \( I_N(y,z) = 27 (z - y)^3 - 3 (z - y) \). The third algebraic equation in Eq. (4) implements balancing between the branch currents of \( N1 \) and \( N2 \), whose characteristics are \( i_N1(y,z) = I_N(y,z) \) and \( i_N2(y) = \frac{27}{3} y^3 - \frac{1}{3} y^3 \), respectively. Since this circuit is autonomous, in order to accurately determine the components of its spectrum by Fourier integrals, we have to accurately evaluate its working period. We determined a point belonging to the steady-state trajectory of this oscillator by means of the SH method of PAN and then started a time domain simulation along \( 10^4 \) periods of oscillations [12]–[14]. We determined the time instants at which the \( z(t) \) voltage crossed the \( 0 \) threshold with positive derivative. Threshold crossing was determined with an accuracy of \( 3 \cdot 10^{-18} \), i.e., for a time window of amplitude \( T \) and for any occurrence of the variable integration time step \( h \), threshold crossing was considered as acceptable if \( h < T^2 \). We simulated the circuit for 9905 threshold crossings and recorded each estimated period. The obtained results are reported in Table II; the meaning of the symbols are: \( T_{ave} \) is the average period, \( f_1 \) the corresponding average working frequency of the oscillator, \( \Delta J_{abs} \), the cycle jitter in the threshold crossing, that is the standard deviation of the computed working periods, \( dt_{max} \) is the maximum absolute value of the difference between \( T_{ave} \) and each computed period, \( dZ_{max} \) the maximum difference \( (z(T_{n+1}) - z(T_n)) \), i.e. the maximum difference between the values assumed by the solution \( z(t) \) at the beginning and at the end of the computed periods, \( z_{max} \) the maximum value assumed by \( z(t) \) along the considered periods. Note that we refer to cycle jitter and compute it as if the circuit were noisy but in fact it is noiseless, being noise sources turned off. This means also that known methods to relate cycle jitter to phase noise due to white Gaussian sources can not be applied.

### Table II

<table>
<thead>
<tr>
<th></th>
<th>case 1</th>
<th>case 2</th>
<th>case 3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( h_{max} : 3 ) ps (2)</td>
<td>( h_{max} : 30 ) ps (2)</td>
<td>( h_{max} : 30 ) ps (3)</td>
</tr>
<tr>
<td>( T_{ave} )</td>
<td>1.9990 ns</td>
<td>2.0004 ns</td>
<td>1.9988 ns</td>
</tr>
<tr>
<td>( f_1 )</td>
<td>500.25 MHz</td>
<td>499.91 MHz</td>
<td>500.29 MHz</td>
</tr>
<tr>
<td>( J_{abs} )</td>
<td>1.4986 ns</td>
<td>20.591 fs</td>
<td>6.115 fs</td>
</tr>
<tr>
<td>( dt_{max} )</td>
<td>1.379 fs</td>
<td>5.201 ps</td>
<td>1.319 ps</td>
</tr>
<tr>
<td>( dZ_{max} )</td>
<td>-1.18 nV</td>
<td>-4.53 nV</td>
<td>-5.35 nV</td>
</tr>
<tr>
<td>( z_{max} )</td>
<td>1.159 V</td>
<td>1.161 V</td>
<td>1.159 V</td>
</tr>
</tbody>
</table>

2The value of \( \tau \) has been determined by considering that the \( T \) working period of the oscillator is about 2 ns, that the \( \epsilon \) relative precision of the computer ALCU is about \( 10^{-16} \) (the IEEE floating point standard [15] sets relative precision at \( \epsilon = 2.22044605 	imes 10^{-16} \) and that we want to simulate the circuit for about \( 10^4 \) periods. At the end of the simulation the minimum allowed integration time step is \( h_{min} = 10^4 	imes 3nA \times \epsilon = 2 \times 10^{-21} \). This choice of \( \tau \), with \( \tau > h_{min} \), ensures that in determining \( \tau \) by means of threshold crossing there are at least 9 significant digits accurately computed.
effect. The attempt of reducing noise by lowering $h_{\text{max}}$ yields time consuming simulations; note that to compute for example the noise effects at a typical frequency offset of a few tens of kHz in an oscillator working at several GHz imposed the simulation for 10000 working periods. This in turn limits the minimum allowed integration time step $h_{\text{min}}$ due to the limited relative precision of the ALU.

The result of all these effects and limitations are synthesized by the levels of the noise floor reported in Table I. The best noise floor is obtained, as expected, in case 1. It is opinion of the authors that the $-116$ dB level limit the application of current time domain noise analyses to modern VCOs and as a consequence to PLLs. Indeed noise levels (mainly due to phase noise) of modern VCOs can be less than $-130$ dB.

Figure 2 shows two kinds of periodograms obtained by simulating the Van der Pol oscillator. The x-axis reports the offset frequency from the fundamental. The upper panel shows the results obtained with the circuit simulators ELDO (blue), SPECTRE (red), and PAN (green) in simulating the noiseless version of the oscillator. We performed a conventional TRAN analysis with ELDO and PAN and performed a time domain noise analysis with SPECTRE. In the latter case we would expect a very low noise floor. As it can be seen from Fig. 2, all simulators show relevant levels of noise floors.

The lower panels show the results obtained by solving the explicit form of system (4) through a SDAE approach. The system has been solved by using a second-order Runge-Kutta integration method for stochastic differential equations [16], [17]. The two panels correspond to different values of the integration step $h$ and the different curves in each panel are related to different values of the power level $\epsilon$ of the white noise: noiseless case (black), $-60$ dB (blue), $-50$ dB (cyan), $-40$ dB (yellow), $-30$ dB (red). The noise floor, which is roughly the average value of the power spectrum in the noiseless (i.e., with $\epsilon = 0$) case, raises as far as $h$ is increased. As a consequence, in the middle panel, the spectra corresponding to power levels of the white noise below the noise floor approach each other, since the dominant effect is due to the numerical noise introduced by the integration algorithm. The overall performance of the SDAE approach, even by resorting to very low (and thus time consuming) time steps, is not better than that of the circuit simulators. This can be interpreted as one of the main reasons (beyond complexity) for which this kind of approach did not spread in the circuit simulation framework.

IV. CONCLUDING REMARKS

In this paper, by means of simple benchmark circuits, we have shown how the numerical noise floor introduced by both circuit simulators and a specific SDAE solver easily hides the effects due to external noise sources, thus making useless the application of time domain noise analysis. Since this kind of analysis is extremely important to characterize the noise effects in circuits that “do not admit” a periodic steady-state working condition, we do think that there is enough room and an evident necessity to develop new and challenging strategies to overcome the highlighted limitations.

REFERENCES