Multi-hop communications on wireless network-on-chip using optimized phased-array antennas

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A R T I C L E   I N F O
Article history:
Received 16 March 2012
Received in revised form 10 June 2013
Accepted 10 June 2013
Available online 4 July 2013

A B S T R A C T
Network-on-Chip (NoC) as a promising design approach for on-chip interconnect fabrics could overcome the energy as well as synchronization challenges of the conventional interconnects in the gigascale System-on-Chips (SoC). The advantages of communication performance of traditional wired NoC will no longer be continued by the future technology scaling. Packets that travel between distant nodes of a large scale wired on-chip network significantly suffer from energy dissipation and latency due to the routing overhead at each hop. According to the International Technology Roadmap for Semiconductors annual report, the RFCMOS characteristics will be steadily improved by technology scaling. As the operating frequency of RF devices increases, the size of Si integrated antenna will decrease and it is feasible to employ them as a revolutionary interconnect for intra-chip wireless communications. In this paper, we focus on physical requirements and design challenges of wireless NoC. It is demonstrated that employing an optimum-radiation phased array antenna and multihop communications will increase the reliability of on-chip wireless links by several orders of magnitude using a limited power budget less than 0.1 pJ/bit.

1. Introduction

Technology scaling towards nanometer geometries to address the need for higher performance and lower power requirement in IC design have resulted in severe challenges with interconnect technology. To compare the effect of technology scaling on the performance of interconnect and transistor, one can observe that in 1.0 μm Al/SiO2 technology the MOS transistor delay was about twenty picoseconds. At the same time, the parasitic RC delay of a 1 mm interconnect was nearly 1 ps, while employing improved metal and dielectric characteristics, e.g. Cu/low-κ in a projected 35 nm, the transistor delay will become about 1.0 ps, and the RC delay of a 1 mm interconnect will be reduced about 250 ps [1] which clearly shows the true bottleneck in IC performance. Besides, without a new interconnection paradigm, the percentage of interconnections power consumption in a typical microprocessor will change from 51% at 0.13 μm generation up to 80% at 90 nm [2].

The fundamental limitations of electrical interconnects have been investigated by many authors [3–6]. First, lets discuss the limitation called Time of Flight (ToF), which is related to the upper bound of signal propagation speed in a medium with effective permittivity $\varepsilon_{\text{eff}}$ and has been formulated in [5]

$$ToF = 33.33\sqrt{\varepsilon_{\text{eff}}} \text{ ps/cm}$$  \hspace{1cm} (1)
As an example, for global interconnection on highest metal layer where $v_{\text{eff}} = 3.0$ for a low-\(\kappa\) dielectric and a die size of \(2.74 \text{ cm} \times 2.74 \text{ cm} (750 \text{ mm}^2)\) in current technology, the time for a signal traveling on the longest path (as shown in Fig. 1) of 5.48 cm is 316 ps. This would require that the global interconnection clock frequency to be less than 3 GHz and this is far from the projected global frequency of 6.8 GHz at 35-nm technology node in 2012. Fig. 1 points out the effect of ToF limit on the area size that a chip can work synchronously.

Another fundamental limitation of wires, called aspect ratio limit, expresses the maximum achievable bit-rate capacity of electrical interconnects that only depends on the aspect ratio of the wire. According to the Miller’s work [6]

$$B_{\text{max}} = B_0 \cdot \frac{A}{l^2}$$

where \(B_0\) is the bit-rate capacity constant approximately \(10^{16}\) b/s for small on-chip interconnects and \(10^{17}–10^{18}\) b/s for equalized lines, \(A\) is the effective cross-sectional area of the line and \(l\) is the length of interconnect. A model of on-chip interconnections between two metal layers is sketched in Fig. 2. The parameters in Fig. 2 are optimized for minimum line capacitance according to the Bakoglu curves [3]. For such a scenario, a 1 cm length interconnect segment of minimum pitch global wires on 35-nm technology has a maximum bit-rate of 2 Mb/s.

Using fat global interconnects like what is proposed in [5] could improve the single line throughput. However, it reduces the number of such wires and so will decrease the total bandwidth across the chip area. Another solution is to divide global interconnect into small subsections and to insert a repeater at each end [3]. Some challenging issues about repeaters consists of the large amount of via cuts to link buffer nets on substrate and wire segments, difficulty to find optimal places for repeat-

**Fig. 1.** ToF limitation on propagation speed of electrical interconnects at 35-nm generation.

**Fig. 2.** A practical on-chip interconnect layer.
ers and finally their area- and power-hungry nature [4]. Repeated wires on delay optimized devices consumed more than 40% of chip input power [5]. In the annual reports published by the International Technology Roadmap for Semiconductors (ITRS), improvement in metal interconnection by utilizing repeaters, line equalizer and low-κ dielectric would satisfy the need for growing performance to any further extent [1]. Replacing System-on-Chip (SoC) buses by the state-of-the-art paradigm, i.e. Network-on-Chip (NoC) as its communication structure could alleviate the problems of traditional shared metallic buses [7,8]. Fig. 3 shows an NoC with mesh topology.

By permanent scaling of the transistor feature size and interconnect wires to satisfy Moore’s law, traditional NoCs could only postpone the ultra deep submicron (UDSM) interconnect problems for a limited interval. Also, communicating between distant nodes of a massive wired NoC requires considerable power consumption and has high latency of the signal propagation through the intermediate switches. To overcome this problem, a number of novel interconnect solutions have been introduced in the recent years [1]. The noticeable features of these novel interconnects are high bandwidth, low latency and low power consuming communication which can address the performance requirement of the future ICs. 3D stacked, photonic interconnect, microstrip lines, RF coplanar waveguide and wireless links are instances of such novel interconnects.

Due to the improvement of Si RF-MOS transistor characteristics with advances in semiconductor industry, it is feasible to implement electrical circuits operating at frequencies beyond hundreds of GHz. As demonstrated in ITRS, the cut-off frequency of NMOS transistors is projected to reach around THz by 2020. This fact can be extrapolated from Fig. 4. So, such available supreme bandwidth can be utilized by RF transceivers to reach several Tb/s data rates for on-chip applications on the current and the next generation technologies.

![Fig. 3. An NoC with a 4 × 4 mesh topology. S_ij's are switches and pe's are process elements such as processors, memories, IO banks or other IP cores.](image)

![Fig. 4. NMOS cut-off frequency versus year and technology node, extracted from ITRS 2007 [1].](image)
On the other hand, the feasibility of wireless communication through miniaturized on-chip antennas has been studied and implemented in a number of recent works [9–14]. Compare to the other novel interconnects solutions, it can be noted that the wireless communication through on-chip antenna will be more feasible in near term because:

- Antenna-based wireless systems are compatible with the current semiconductor technology, i.e. CMOS. In addition, antennas can be implemented in a metal layer (preferably in the top metal layer) and there is no longer a need for specialized layer.
- Currently, a number of wireless transceivers such as ultra wideband (UWB) transceivers have been developed and optimized for CMOS technology. Moreover, these works on improving the transceiver structures are continuing along with the new semiconductor generations.
- A typical miniaturized on-chip antenna needs a very small area compared to the die size. In volume production, each antenna increases the total cost by about 1–2 cent per die [9].

In this research, the challenges of Wireless NoC will be discussed. We propose a hybrid architecture, where wireless interconnect will be employed for global or semi-global multihop communications, and wired interconnection will be utilized for local area (i.e. antenna radio range).

Related works in the field of on-chip antenna and wireless system will be reviewed in Section 2 and several challenging issues against Wireless Network-on-Chip development will be mentioned. Optimizing such systems to employ for intra-chip communications from antenna radiation point of view, as the first step towards wireless NoC, will be discussed in Section 3. The structure of Wireless NoC network layer together and its problems and the medium access control (MAC) solution mechanism will be explained in Section 4. Finally, the performance of wireless multihop NoC will be evaluated and compared to wireless single-hop or direct communication in Section 5.

2. Related works

As confirmed by ITRS (see Fig. 4) the RF-MOS transistor characteristics is continually improving by technology scaling. As a result, both circuits’ operating frequency and communication bandwidth are increasing. As the cut-off frequency \( f_t \) as well as maximum unity gain frequency \( f_{\text{max}} \) of RFCMOS increase, the size of quarterwave antenna decreases and the available data bandwidth will also increase. For example, in 45 nm CMOS technology and possible frequency of 100 GHz, the length of a monopole \( \lambda/4 \) antenna to be employed on Si substrate is 220 \( \mu \)m. Such miniaturized antenna will decline the cost of antenna integration and related circuits significantly with technology scaling. IC designers will be able to examine numerous wireless systems for on-chip applications.

Feasibility of on-chip wireless interconnects for intra-chip global clock distribution was demonstrated first by Floyd in [9]. A 15 GHz global clock signal is broadcasted across a 5.6 mm die and the received clock by receiver antenna is converted to a 1.875 GHz local clock. In addition, the on-chip antenna can also be applied to data communications [10].

Because of the lossy nature of bulk Si substrate and also its high permittivity constant, implementation of an efficient antenna on such substrate is highly challenging. A number of papers in [11–13] have focused on the design of high

Fig. 5. Typical on-chip printed antennas. (a) Linear dipole, (b) meander dipole, (c) folded dipole, (d) zigzag dipole, (e) loop antenna, (f) inverted-F.
transmission gain on-chip printed antenna. Six types of most popular antennas are depicted in Fig. 5. Optimizing the radiation patterns of the printed antennas for network based intrachip application will be discussed later in Section 3.

Kiomoto and Kikkawa showed that higher substrate resistivity could improve the transmission gain [13]. The effect of other parameters on transmission coefficient such as heat removal sub-layer, substrate thickness and parasitic effects of other metal layers are argued in [10,14], respectively.

Ultra wideband (UWB) communication systems which were successfully applied in wireless sensor networks for high data-rate, short range and low power communication, are suitable candidates for intrachip wireless interconnect. The available unlicensed bandwidth for UWB communication is in the frequency range of 3.1–10.6 GHz. The power spectral density of the signal must be less than $-43.1 \text{ dBm/MHz}$ [15]. However, this constraint will not limit the intrachip application. The structure of a UWB impulse radio transceiver studied in [16] is shown in Fig. 6. The transmitter consists of a modulator such as time hopping pulse position modulator (TH-PPM) or binary phase shift keying (BPSK) and a Gaussian mono cycle pulse (GMP) generator which produces a short cycle pulse without any DC component and consequently the transmitter will consume less power. At the receiver end, the received signal is correlated with a synchronized template pulse and a level detector or 1-bit ADC converts the output signal to a digital data stream.

Implementation of UWB communication systems on ICs is discussed in a number of papers [17,18]. The theoretical basis for multiple access analysis of frequency time hopping PPM UWB was studied by Biradar et al. by assuming perfect symbol synchronization [19]. In this paper, it was demonstrated that increasing the number of active users will drastically degrade the transmission bit error rate (BER). To alleviate the effect of synchronization, differential PPM scheme proposed by Shiu and Kahn in [20] could be employed that results in a better power consumption as well as bandwidth efficiency. Table 1 summarizes a number of implemented or simulated wireless transceivers for intrachip applications. These wireless systems are the primary efforts in this field and more optimization and investigation process is needed for realistic intrachip application. For instance, increasing the bandwidth efficiency by multiple access technique at operating frequency of 100 GHz in 45 nm technology, an aggregate data-rate above 0.5 Tb/s can be achieved that is a satisfactory number for current on-chip applications [25].

The concept of Radio on Chip (RoC) for wireless test control network was first introduced by Zhao et al. [23]. In their proposed design, a number of cores were connected to an RF base station (BS) by wired interconnects, communicated to the other cores through wireless medium using RF-BSs. They assumed circular radio coverage for each RF-node. A simple location-based routing for wireless NoC was proposed in [24]. Zhao and Wang also proposed a synchronous medium access control for their wireless NoC in [25]. Another wireless NoC based on carbon nanotube (CNT) antenna for line of sight (LOS) communication was first introduced by Ganguly et al. [26]. They used their hybrid wireless NoC as a communications backbone for multi-core SoC design and showed that their WiNoCs are capable of outperforming more traditional wired counterparts in terms of network throughput, latency, and energy dissipation.

As discussed so far, the Wireless Network-on-Chip is still a conceptual idea and hence there are a number of challenging but solvable issues against its realization. Some of them are briefly addressed here:

- Intra-chip wireless signal propagation should be characterized and the on-chip multi-path fading must be modeled. Also, the amount of switching noise degradation on the received signal is needed to be investigated more.
- High-speed digital to analog (A/D) and analog to digital (D/A) of Giga Sample per second must be designed to convert signals. However, for a bandwidth efficiency of 1 bps/Hz a single bit comparator could be used.

![Fig. 6. UWB-IR transceiver block diagram (TH = Threshold comparator, LNA = Low noise amplifier).](image-url)
In the irregular network topology, IP-cores must be clustered and assigned to wireless nodes. On the other hand, the designer should place the wireless nodes on the optimum positions in order to minimize routing cost. Ultra high speed, power and area efficient wireless transceivers must be developed for intra-chip application. Efficient radiation on-chip printed antenna should be designed to increase the transmission gain on the wanted directions. A flexible and low latency medium access mechanism is needed to provide a fair access on wireless shared medium for wireless transceivers. The area and power consumption overhead of such a sub-layer must not exceed the limitation of NoC infrastructure.

3. Optimizing wireless interconnect system

In this section, first, the characteristics of a basic on-chip linear dipole antenna intended for intrachip application is evaluated by simulation and then the performance of the proposed integrated phase array antenna is discussed and compared to on-chip dipole antenna.

3.1. Basic on-chip printed dipole antenna

Due to the compact size of printed on-chip antenna, they have been widely employed for inter and intrachip wireless communications. A number of printed antennas for on-chip Si integrated applications are depicted in Fig. 5. The basic form of these antennas is derived from linear dipole element. To evaluate the radiation characteristics of a printed dipole antenna using FIT method, the CST Microwave Studio simulation package is applied. A 260 \( \mu \)m thick high resistivity Si substrate with \( \varepsilon_r = 11.9 \) and 5-k cm resistivity is considered for simulation. The antenna is implemented on a 3 \( \mu \)m thick SiO \(_2\) insulator for which \( \varepsilon_r = 3.9 \). The chip size is assumed to be 2.5 cm \( \times \) 2.5 cm with the current technology. Fig. 7 shows the cross sectional view of the simulation process.

In order to run a simulation around a central frequency of 20 GHz, the length of halfwave dipole element is set to 4 mm. The separation distance between Tx and Rx antenna is assumed to be one forth of chip size, i.e. 6.25 mm. The reflection coefficient \( (S_{11}) \) and transmission coefficient for different placement \( (S_{21}, S_{31}) \) of a dipole antenna pair versus frequency are shown in Figs. 8 and 9, respectively. The \( S_{11} \) is found to be less than \(-10 \) dB in the frequency range of 14.5–23 GHz.

Because of the restricted dimensions of substrate, another resonance mode is excited within the substrate material. Moreover, this constraint causes that an additional component of the radiated field along the antenna arms (y axis) emerges. The graph in Fig. 10 shows the radiation pattern of dipole antenna which clearly illustrates its drawbacks for network based intrachip communication. First, the dipole antenna could efficiently radiate into two directions. This effect is visually elucidated in transmission coefficient between a pair of on-chip dipole antennas for face to face and aligned situations in Fig. 9.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Wireless system</th>
<th>Antenna area (mm(^2))</th>
<th>Transceiver area (mm(^2))</th>
<th>Operating frequency (GHz)</th>
<th>Bandwidth (Gbps)</th>
<th>Radio range (mm)</th>
<th>Energy per bit, ( E_b ) (pJ/bit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Floyd et al. [9]</td>
<td>0.18 ( \mu ) CMOS technology</td>
<td>0.24 ( \times ) 2</td>
<td>Tx: 0.4 ( \times ) 0.29</td>
<td>15.0</td>
<td>1.875</td>
<td>53</td>
<td>( E_b = 48 ) mW</td>
</tr>
<tr>
<td></td>
<td>Intrachip 2 mm Zigzag dipole antenna</td>
<td></td>
<td>Rx: 0.37 ( \times ) 0.58</td>
<td></td>
<td></td>
<td>5.6</td>
<td></td>
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<tr>
<td></td>
<td>Chip area 7 ( \times ) 6 mm(^2)</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>He and Zhang [17]</td>
<td>0.18 ( \mu ) CMOS technology</td>
<td>–</td>
<td>Tx: 0.63 ( \times ) 0.8</td>
<td>4.5–6.0</td>
<td>0.4</td>
<td>–</td>
<td>( E_b = 47 ) mW</td>
</tr>
<tr>
<td></td>
<td>Interchip UWB impulse radio, TH-PPM modulation</td>
<td></td>
<td>Rx: 1.46 ( \times ) 2.24</td>
<td></td>
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<td></td>
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<tr>
<td>Sasaki et al. [18]</td>
<td>0.18 ( \mu ) CMOS technology</td>
<td>Tx: 0.5 ( \times ) 2.98</td>
<td>Tx: 0.1</td>
<td>3.6</td>
<td>1.16</td>
<td>1.0</td>
<td>( E_b = 21.6 ) mW, ( P_t = 40 ) mW</td>
</tr>
<tr>
<td></td>
<td>Intrachip UWB</td>
<td>Rx: 0.45 ( \times ) 4</td>
<td>Rx: 0.99 ( \times ) 0.55</td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td></td>
<td>OOK modulation</td>
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<tr>
<td>Zhang [21]</td>
<td>0.18 ( \mu ) CMOS technology</td>
<td>–</td>
<td>15.0</td>
<td>2.0</td>
<td>5.0</td>
<td>Transmitted power: 0–10 dBm, ( BER &lt; 10^{-5} )</td>
<td>( E_b = 53.1 ) mW</td>
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<td></td>
<td>simulation – coheren BPSK modulation</td>
<td></td>
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<tr>
<td>Chang et al. [22]</td>
<td>0.18 ( \mu ) CMOS technology</td>
<td>Microstrip can be</td>
<td>Tx/Rx: 0.6</td>
<td>2.65</td>
<td>2.65</td>
<td>–</td>
<td>( P = 74 ) mW</td>
</tr>
<tr>
<td></td>
<td>multi-carrier CDMA interconnect</td>
<td>used for wireless</td>
<td></td>
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</tbody>
</table>

Table 1

A number of proposed wireless transceiver systems.
Secondly, one of the maximum values of the directivity in the z direction (perpendicular to the chip surface) leads to a lower transmission gain at similar co-plane antenna chip surface.

Integrated on-chip loop antenna is another basic element for on-chip wireless communication that could alleviate the dipole pattern problems for intrachip application. The radiation pattern of printed loop antenna is omni-directional in the antenna plane [10]. In addition, its maximum radiation is posed on the chip surface. Whereas omni-directional radiation

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**Fig. 7.** The cross sectional view of on-chip dipole antennas on a Si die size 2.5 cm × 2.5 cm.

**Fig. 8.** Dipole antenna reflection coefficient ($S_{11}$) versus frequency.

**Fig. 9.** Transmission coefficient versus frequency of dipole antenna pairs.
of printed loop antenna might waste the power in undesired directions, and therefore, is not suitable for low-power wireless NoC design.

A well-designed on-chip antenna for wireless low power interconnect should efficiently radiate on predetermined direction and be sufficiently attenuated in other directions. A well-known method to achieve this goal is employing the concept of

![Fig. 10. Radiation pattern of dipole antenna at 20 GHz. (a) 3D view. (b) Elevation plane ($\phi = 0^\circ$). (c) Azimuth pattern ($\theta = 90^\circ$).](image)

![Fig. 11. Proposed phased array antenna schematic.](image)
Fig. 12. PA antenna reflection coefficient ($S_{11}$) versus frequency.

Fig. 13. Radiation pattern of proposed PA antenna at 20 GHz. (a) 3D view. (b) Elevation plane ($\varphi = 0^\circ$). (c) Azimuth pattern ($\theta = 90^\circ$).
phased array (PA) antenna. Our proposed PA antenna for planar mesh network topology is presented in the following subsection.

3.2. Proposed on-chip phased array antenna

The proposed PA antenna consists of four quarterwave monopole elements shown in Fig. 11. The array feed network produces a 180° phase difference with equal power between adjacent elements.

To assess the antenna radiation characteristics, the proposed PA antenna is assumed to be fabricated on the same substrate mentioned in Fig. 7. The reflection coefficient \( S_{11} \) of the phased array antenna versus frequency is shown in Fig. 12. As shown in Fig. 12, the –10 dB impedance bandwidth of the PA antenna is much wider than dipole one’s which provides a better matching capability in a wider frequency bandwidth.

The radiation pattern of this antenna is plotted in Fig. 13. As expected, PA antenna has four main lobes which are matched to the orthogonal sides needed for network topology. Such a pattern could reasonably satisfy low-power and reliable wire-less interconnects requirements for NoC applications.

To compare the performance of on-chip antennas under matched conditions, one can compute the transmission gain obtained by utilizing Friis transmission equation [12]

\[
G_a = \frac{P_r}{P_t} = \frac{|S_{21}|^2}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)} = G_t G_r \left( \frac{\lambda}{4\pi r} \right)^2 e^{-2\alpha r}
\]

where \( P_t \) and \( P_r \) are transmitted and received power, respectively, \( \alpha \) is the environmental attenuation factor, \( G_t \) and \( G_r \) are transmitter and receiver antenna gain respectively, \( \lambda \) is the wavelength and \( r \) is the separation distance.

The simulation results for the two dipole antenna pairs in Fig. 7, and the proposed PA antenna pair separated by 6.25 mm, are illustrated in Fig. 14.

The graph in Fig. 14 confirms that the proposed PA antenna has considerable improvement in transmission gain as compared to dipole antenna at the frequency bandwidth range shown in Fig. 8. The \( G_a \) at central frequency of 20 GHz is increased by 27.2 dB and 20.2 dB compared to opposite and aligned dipole pairs, respectively.

4. Network layer

The major challenge in NoC-based SoC design is optimizing the communications backbone. This means that the communications network resources and related overheads must be essentially optimized versus three crucial design parameters: power, area and aggregate bandwidth. NoC power consumption as well as its chip area overhead should be minimized while providing sufficient total bandwidth for intrachip communications between cores. Thus, a traditional layered network design might not satisfy resource optimizing. Though, the layered methodology makes the design process of each layer independent from other layers, and consequently, simplifies the design process.

We propose a hybrid structure for NoC where, the area of the chip is regularly decomposed into smaller sub-areas called Subnets. In a subnet, cores’ connections are made through a local wired NoC. The center core of a subnet is called RF-node. This node is equipped with a wireless transceiver for long distance communications with other RF-nodes. IP-Cores symbolize several special-designed communication and signal processing cores while process elements stand for general-purpose processors. All or a number of the border modules in a subnet are connected to the border modules of the neighbor subnets.
Therefore, each core should be able to diagnose the best way for communicating to destination core, i.e. chooses between (1) send the packet to the destination through wired network, or (2) send the packet to RF-node and then the RF-node will send it to the destination RF-node through wireless network. The structure of a subnet and its components are depicted in Fig. 15.

Communicating in a wireless network is single hop for small size networks, and multiple hops in case of large size networks. Moreover, with a higher transmission power, wireless transceivers can send packets directly to their destinations by a single hop transfer. We will evaluate the performance of transceivers for single and multiple hops intrachip communications in Section 5.

Based on a joint optimization of physical layer and network layer, the topology of wireless network is selected in an efficient way to maximize the transmission gain between neighbor subnets. For an array antenna with four main lobes similar to
what we proposed in Section 3, the flat mesh topology is the best one (Fig. 16) because its radiation pattern has four maximum values towards the main geographical directions on the chip surface. For a loop antenna with omni-directional radiation pattern the hexagonal network in Fig. 17 would have a better performance.

One of the important issues in wireless network is collision which is arisen due to shared nature of wireless medium. As a result, communications in wireless network requires special medium access control (MAC) mechanism. As shown in Fig. 18a, hidden station problem occurs when two RF-nodes which are not in their radio range of each other, send data simultaneously to a common intermediate node. Thus, the sending station A is hidden to station C. On the other hand, exposed station problem can limit a transmission. In Fig. 18b, station B is going to send data to A and C is already transmitting to D. Since C is within the radio range of station B, B should not be allowed to send A.

To overcome these problems, one way is to employ a wired MAC mechanism similar to what was proposed in [25] or wireless MAC presented in MACAW mechanism [27]. An alternative to this is the multiple access communication methods. Due to the short range of wireless transceivers, resources such as time slot, frequency carrier and spreading sequence could be reused in RF-nodes located farther. The area where all resources could be reused is called a cluster. Clusters for wireless

Fig. 17. Spatial reusing in hexagon topology network.
mesh and hexagon networks are shown in Figs. 16 and 17, respectively. The projected resource is carrier frequency which is 5 carriers for each cluster of mesh network (based on proposed efficient radiation antenna) and 7 for hexagon network. Each transceiver sends on one carrier and receives on all surrounding carriers. The effect of multiple access schemes on wireless medium reliability will be discussed in the following section.

For different irregular topologies, the antenna cannot be directive. So, a tolerable antenna pattern is omni-directional like a printed on-chip loop antenna. Using this antenna pattern will increase the number of nodes that share a common wireless medium. So, the available resources will be shared by more nodes or a more complex channel access control method must be employed for such topologies. Also, the placement of RF-nodes should be optimized for efficient wireless connectivity between the cores.

5. Performance evaluation

One of the exigent problems with wireless communication is the transmission of a signal to a long distance from a single antenna. Since, the strength of the transmitted signal decays exponentially with traveling distance, the probability of error occurrence in transmission will increase. The bit error rate (BER) of analog communication system could be improved by increasing the transmitting power or by placing repeaters. A comparison between direct transmitting and utilizing repeaters for transmission lines is presented by Carlson et al. [28]. We apply the same analysis here to demonstrate that multihop communication will cause an improvement in power efficiency as well as reliability of the wireless network compared to long distance transmission. This methodology needs the knowledge about the amount of power attenuation in the wireless channel. We use the Friis transmission equation in (3) as a basis for the performance evaluation. In the first step, several simulations have been run to obtain the attenuation coefficient, $a$, in (3).

Fig. 19. (a) Different transmission situations. (b) Transmission gain versus RF-node positions.
Fig. 19a shows an illustration of different direct transmission situations between RF nodes in the mesh topology. To find the transmission gain $G_a$ in each situation at 20 GHz, the simulation has been conducted with PA antenna pair separated by a distance shown in Fig. 19a. The results are exposed in Fig. 19b. The transmission gain decreases with separation distance as well as the alignment angle. For example, the effect of doubling the distance between antenna pair in a face to face position is 7.9 dB reduction in $G_a$ while the effect of a 45° rotation in a shorter distance ($\sqrt{2}d_1$) will cause a higher reduction of 10.9 in transmission gain. This is because of the directivity of PA antenna gain.

By expressing the Eq. (3) in decibel, the difference of two transmission gains for separation distance of $r_2$ and $r_1$ between antenna pair is given by

$$10 \cdot \log_{10} \left( \frac{G_{a2}}{G_{a1}} \right) = G_{a2, dB} - G_{a1, dB} = -20 \cdot \log_{10} \left( \frac{r_2}{r_1} \right) - 20 \pi (r_2 - r_1) \log_{10} e$$  

(4)

By curve fitting from Fig. 19b, the attenuation coefficient $\alpha$ will be 0.035 Np/mm.

To compare the multihop with single communications, we assume two transmitting situations shown in Fig. 20.

In situation Fig. 20a, the source RF-node transmits directly to the destination situated $d$ mm far. The signal to noise ratio (SNR) for an AWGN wireless channel with a two-sided noise power spectral density (PSD) $N_0/2$ is given by [28]

$$\frac{S}{N}_{Ra} = \frac{ST}{N_0Bw}$$  

(5)

where $S_T$ is the power delivered to the antenna, $L$ is the path loss and $B_w$ is the transmission bandwidth.

In situation Fig. 20b, the source RF-node sends its packet to the receiver through ($m-1$) similar intermediate RF-nodes that are separated by $d_1 = d/m$. If each RF-node is equipped with a high noise figure low noise amplifier (LNA) with the possibility of compensating the channel loss in $d_1$, the SNR at the destination could be written as a function of SNR in the first transmission (SNR$_1$) [28]

$$\left( \frac{S}{N} \right)_{Rb} \approx \frac{1}{m} \left( \frac{S}{N} \right)_{Ra} + \frac{1}{m} \left( \frac{S_T/L_1}{N_0B} \right) = \frac{L}{mL_1} \left( \frac{S_T/L}{N_0B} \right) - \frac{L}{mL_1} \left( \frac{S}{N} \right)_{Ra}$$  

(6)

where $L_1$ is the path loss between each antenna pair. In $m$ sequential retransmissions, the total additive noise will be $mN_1$. The $L/mL_1$ coefficient in (6) is the SNR improvement factor. For a homogenous environment, the path loss is inversely proportional to the square distance and exponentially proportional to environment loss. Thus, the SNR in scenario (a) could be written as

$$\left( \frac{S}{N} \right)_{Rb} \approx \frac{1}{m} \left( \frac{d}{d_1} \right)^2 e^{2\pi(d-d_1)} \left( \frac{S}{N} \right)_{Ra} = m \cdot e^{2\pi d_1(m-1)} \cdot \left( \frac{S}{N} \right)_{Ra}$$  

(7)

![Fig. 20](image-url)
In [28] Carlson et al. demonstrated that for an antipodal binary signaling, the bit error probability is

\[ P_{eb} = Q\left(\sqrt{\frac{S}{N}}\right)_{R_b} = Q\left(\frac{1}{m} \sqrt{\frac{S}{N}}\right)_{R_b} = Q\left(e^{nd}(m-1) \sqrt{m} \sqrt{\frac{S}{N}}_{R_b}\right) \]  

(8)

where \(Q(\cdot)\) is the area in the tail of the Gaussian PDF. In practical intrachip wireless transmitters, the power injected into an antenna is a trivial portion of the total power consumption in transceiver. For example, the power delivered to UWB antenna in [17,18] is around \(-10\) dBm which is very small when compared to total power consumption of 20 dBm for transmitter. If the antenna efficiency is 100% (loss free), the whole injected power will be radiated from antenna and is equal to \(S_T\). If the total power consumption of a wireless transmitter is linearly related to the transmitted power, Eq. (8) can be used as a benchmark for power efficiency comparison. This is a practical assumption.

Another issue that must be considered is the regenerative nature of RF-nodes. Each RF-node in our wireless scheme of Fig. 15 has a full structure transceiver which can receive RF signal, regenerate its carrying digital data contents and then retransmit it. This conversion process could possibly generate a number of errors in recovered digital bit stream. The bit error probability in the first regenerator repeater (transceiver), \(\alpha\), is given by

\[ \alpha = Q\left(\sqrt{\frac{S}{N}}\right)_{R_a} \]  

(9)

When a bit is traveling through a wireless medium between two stations, it may flip due to the channel noise. Thus, the probability of receiving an erroneous bit in the receiver after \(m\) consecutive retransmitting can be written as

\[ P_{eb} = \sum_{i=\text{odd}} m^i \alpha^i(1-\alpha)^{m-i} \]  

(10)

for \(\alpha \ll 1\) and a reasonable \(m\), (10) could be rewritten as

\[ P_{eb} \approx m\alpha = m \cdot Q\left(\sqrt{\frac{S}{N}}\right)_{R_a} = m \cdot Q\left(e^{nd}(m-1) \sqrt{m} \sqrt{\frac{S}{N}}_{R_b}\right) \]  

(11)

Relation (11) shows how bit error probability \(P_e\) linearly increases with the number of hops while exponentially decreases with \(m\). From (8) it can be found that if only repeaters are used, for a fixed bit error probability, each intermediate transmitter needs to transmit \(m\) times higher power while for regenerative RF-nodes this is exponentially less. The power efficiency of multihop transmission scheme compared to repetitive and direct single-hop transmitting scheme is plotted in Fig. 21. As shown in this Figure, one can see that for low-power and low BER intrachip wireless communications, multihop scheme brings about an improvement of several orders of magnitude in power efficiency.

As illustrated in Fig. 21, for a bit error probability of \(10^{-5}\), only one intermediate RF-node could decrease the total transmitter power consumption 6 times (7.7 dB). The performance of multihop scheme will significantly improve by increasing the number of intermediate nodes. The plot in Fig. 21 shows the worst case power efficiency improvement for our PA antenna. This is because the PA antenna gain is directive and for a fixed separation distance, it has a maximum on face to face alignment while the gain will be decreased for other directions.

In order to comprehensively evaluate the multihop wireless system, we assume a frequency time hopping binary PPM UWB multiple access transceiver which is studied and presented by He and Zhang [17]. In [19] Biradar et al. have obtained analytically the bit error rate (BER) and we are using their results. The channel is modeled as AWGN where due to the
efficient radiation pattern of the antenna, the multipath fading effect of the wireless channel could be neglected. However it is demonstrated in [19] that employing an all Rake receiver could efficiently collect the received signal from all paths. The parameters of FTH-PPM UWB transceiver system is listed in Table 2.

Using the results in [19], the average bit error probability of the received signal is given by

$$P_b \leq Q \left( N_1 \frac{\eta E_g}{\sigma^2_{\text{MAI}} + \frac{N_g N_0}{2}} \right)$$ (12)

where $\sigma^2_{\text{MAI}}$ is the multiple access interference and is given by

$$\sigma^2_{\text{MAI}} \approx N_1 \eta E_g (N_a - 1) \frac{1}{8N_0 N_{\text{fh}}}$$ (13)

for a mesh topology in Fig. 16 and with the proposed PA antenna, $N_a$ in the worst case is equal 4 because the received signal power from other RF-nodes are at least 8 dB shorter than neighbor RF-nodes. It is demonstrated by Zhang that the channel noise has two major components: Thermal noise ($N_0T$) and Switching noise ($N_0g$) [21]. The latter is resulted from switching in digital circuits. The interference induced by digital circuits around the implemented on-chip antenna is investigated by several papers [29,30]. The measurements show that the majority of the switching noises has a common mode nature and hence can be significantly rejected by differential or balanced fed antenna such as the proposed PA antenna. Measurements in [30] indicated that selecting RF frequency much greater than the logic operating frequency can reduce the switching noise at the input of a differential receiver. A set of design guidelines has been developed for reducing the impact of switching noise on wireless signal [31]. Thus, the channel noise, as calculated in [21], is given by

$$N_0 = N_{GT} + N_{GS} \approx N_{GT} = 4 \times 10^{-21} \left( \frac{T_{\text{ant}}}{290 K} + F_r \right)$$ (14)

where $T_{\text{ant}}$ is the antenna equivalent noise temperature and $F_r$ is the receiver noise figure. For a printed dipole antenna, $T_{\text{ant}}$ is assumed to be 330°K at 15 GHz. This would double in case of the PA antenna. For $F_r = 10$ dB, noise PSD found to be $N_0 = 5 \times 10^{-20}$. For a wireless system with the following parameters:

- Energy per transmitted bit, $E_g = 0.1$ pJ/bit (0.1 mW at 1 Gbps).
- Integrated proposed PA antenna transmission gain (Fig. 13), $G_a = -36.8$ dB.
- Full bit-rate ($N_a = 1$).

The thermal noise is the majority component if $N_{GT} N_{\text{fh}}$ product exceeds 2500 which is not practical for on-chip UWB transceivers. Thus, the BER of the wireless interconnect in wireless NoC with multiple access scheme is independent of the received signal power, and is given by

$$P_b \leq Q \left( \sqrt{2N_{\text{GS}} N_a N_{\text{fh}}} \right)$$ (15)

Fig. 22 shows a plot of bit error rate versus the number of hopping slots neglecting thermal noise.

From this plot, one can deduce that increasing the number of hopping slots will cause considerable improvement in the bit error performance of the wireless system. However if the shared wireless medium is used by only one transmitter, the multiple access interference, $\sigma^2_{\text{MAI}}$, is equal to zero because the number of users $N_a$, in (13) is 1.

For a minimum pitch global interconnect as predicted in ITRS [1], the capacitance per unit length of a global wire will be within a range of 1.8–2.0 pF/cm and $V_{dd}$ will be scaled to 0.9 V by 2012. So, for a fair comparison between a wireless interconnect system and global wired interconnect, the total power of inserted repeaters on the wire interconnect and also the wireless transceiver power consumption must be accounted. If we assume the third wireless transceiver on Table 1 is driving our PA antenna, the consumed energy per bit could be less than (by an order of magnitude) the reported 53 pJ/bit on a range of 5 mm while this parameter will be around 1 pJ/bit for unpeated global interconnect. As shown in [5], the power consumption of global wires in delay-optimal devices that used repeated wires, are 3 times larger than unpeated wires. This comparison revealed that the energy per bit of the two mentioned interconnect system is approximately equal but it must be noted that by scaling RFCMOS devices and a cut-off frequency around hundreds of giga-hertz, more bandwidth efficient wireless transceivers could be designed and used for on-chip communication. A detailed comparison between wireless

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
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</thead>
<tbody>
<tr>
<td>Gaussian pulse energy</td>
<td>$E_g$</td>
</tr>
<tr>
<td>Wireless transmission gain</td>
<td>$\eta$</td>
</tr>
<tr>
<td>The number of time slots</td>
<td>$N_{th}$</td>
</tr>
<tr>
<td>The number of Freq. carriers</td>
<td>$N_{fh}$</td>
</tr>
<tr>
<td>Repetition code length</td>
<td>$N_r$</td>
</tr>
<tr>
<td>The number of active antenna</td>
<td>$N_a$</td>
</tr>
</tbody>
</table>

Table 2
Parameter of ma-uwb system.
and wired NoC power consumption is available on [25]. The results show the superior performance of WNoC compared to its wired counterpart.

If a MAC mechanism is used, meaning that the wireless channel is not simultaneously used by several RF-nodes the reliability of wireless medium could be expressed by (11). To compute the signal to noise ratio at the first intermediate station, at the first step, the thermal noise power at this regenerator station is obtained by

$$N_1 = N_0B_w = 5 \times 10^{-20} \times 10^9 = 5 \times 10^{-11} W = 10 \times \log \left( \frac{5 \times 10^{-11} W}{1mW} \right) = -70.3 \text{dBm}$$

Thus, the SNR$_1$ will be

$$\left( \frac{S}{N} \right)_{1, dB} \leq S_{1, dBm} - N_{1, dBm} = S_{1, dBm} + G_a - N_{1, dBm} = -10 - 36.8 + 70.3 = 23.5 \text{dB}$$

Finally, the worst case bit error probability in a $4 \times 4$ mesh topology occurs if there is a communication between two corner diagonal RF-nodes where $m = 6$ retransmissions are needed. For this situation the bit error probability will be

$$P_{e, multihop} \approx 6 \times Q\left( \sqrt{\frac{2.35}{10^{-12}}} \right) \approx 4 \times 10^{-50}$$

Thus the BER of a low power wireless interconnects for multihop communications on a chip could be small enough that provide more reliable physical medium for practical implementation. However, an approximately error-free communication link is the first step to establish a reliable wireless on-chip network. From a design perspective, other components like a fair and trustworthy medium access mechanism, router and a reliable end-to-end protocol are needed to satisfy the term of system reliability. The error probability in (18) is an optimistic approximation and needs to be refined with a precise on-chip wireless channel model. To improve the bit error rate beyond $10^{-12}$, the design of time and frequency hopping transceiver would be impractical and a MAC mechanism could considerably increase the BER of the wireless links.

6. Conclusion

To achieve a reliable low-power wireless link, the first step would be the design an efficient integrated antenna. We proposed and evaluated a novel scheme of printed phased array antenna for intrachip communication. The results confirm an improvement of 20–27 dB in transmission gain in desired directions when compared to the traditional printed dipole antenna. Employing PA antenna will increase the reliability of wireless link equipped with MAC mechanism by several orders of magnitude. Due to the directive radiation of PA antenna, it is a suitable candidate for regular wireless network on chip application.

By establishing a multihop wireless infrastructure besides traditional wired NoC for long distance packet transmission, the latency and power dissipation are significantly reduced. We show that the multihop wireless communications could improve the power efficiency as well as provide a reliable interconnect for future NoC implementations.

Acknowledgments

This work was supported in part by the ITRC organization under Grant No. 17865/500. The financial support of the Iran Telecommunication Research Center is gratefully acknowledged.
References


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