WARM SRAM: A Novel Scheme to Reduce Static Leakage Energy in SRAM Arrays

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The increasing sub-threshold leakage current levels with newer technology nodes has been identified by ITRS¹ as one of the major fundamental problems faced by the semiconductor industry. Concurrently, the expected performance improvement and functionality integration expectations drive the continued reduction in feature size. This results in ever-increasing power per unit area and the accompanying problem of heat removal and cooling.² Portable battery-powered applications, fuelled by pervasive and embedded computing, in the last few years have seen a tremendous growth and have reached a point where battery power can’t be increased further.³ This raises the computational throughput per watt target for the future technology nodes. SRAM arrays which are used widely as a system component, such as caches and register files, are getting to be dominant power consumers because of their large capacity and area. Hence any reduction in cache energy can result in considerable overall power reduction. In this paper, we propose a novel circuit technique using depletion mode devices, to reduce the static energy of SRAM array in an on-chip cache by 90% without any performance impact.

Keywords: Leakage Energy, SRAM, On-Chip Cache.

1. INTRODUCTION

Static subthreshold leakage has emerged as one of the major impediments in CMOS scaling. The magnitude of the problem is reflected in the fact that the leakage current per unit transistor width is expected to increase a 1000–10000 fold in going from 180 nm technology node to 70 nm technology node. This appears to pose a problem only for state holding circuits such as memory arrays that are idle for extended periods until one considers the following. In the same period, 180 nm to 70 nm technology node, the on (drive) current is expected to stay constant at 750 μA/μm in order to sustain the historical speed advantage. In the 180 nm technology node, the ratio of on current to leakage current per unit transistor width is approximately 7.5 × 10⁵. This ratio is projected to shrink to 750 in 70 nm technology node and to 75 in 32 nm technology node! Some of the implications of this projection are as follows. In 32 nm node, the leakage current is expected to play a major role in the design of some of the high fanout, computing logic as well. Consider a bus with 30 clients being driven by one client. The twenty-nine off transistors (drivers) from the inactive bus clients are able to leak about one half (38%) of the on drive current of the driving client! Similar concerns will surface for logic blocks such as decoders, multiplexors, and gate arrays. This argues that we need to develop low-leakage design styles even for computing logic with high activity rate.

This paper proposes a CMOS design style with low leakage characteristics. This design style belongs to a family of CMOS design styles that we name warmup CMOS. These logic styles warmup initially to charge some nodes up to a certain potential. The steady state energy savings are delivered in the “warmed-up” state with an initial energy cost for the warmup. The specific warmup CMOS design style presented in this paper relies upon depletion mode transistors to provide proper biasing to reduce the leakage. Hence we name it dep-warmup-CMOS. During the active phase of logic, the depletion mode transistors are transparent (Fig. 1). However, during the inactive phase, the depletion mode transistors leak enough charge to bias the transistors to a point favorable with respect to the leakage current. A low leakage current equilibrium state is forced in the inactive phase. We describe the dep-warmup CMOS design style in Section 2.

An immediate application of dep-warmup CMOS logic design style is in static memory arrays characterized

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by caches and register files. Microprocessors attain significant performance improvement by increasing the size and associativity of on-chip caches. For example, Intel’s latest processor family, Centrino\textsuperscript{15} has a 1 MB L2 cache on-chip. Both dynamic switching energy, and static subthreshold leakage current induced energy of on-chip caches are already significant factors in over-all power consumption of the processors. The static leakage energy would overwhelm the dynamic energy for these caches with the expected 1000–10000 fold increase in leakage current in the 70 nm technology node.

This is why the static leakage power reduction is one of the most important considerations in both high-performance and low standby power circuits’ design. As the device size shrinks, to maintain the same on current, threshold voltage $V_t$ has to be reduced. This causes subthreshold current to increase exponentially. Table I compares 0.18 $\mu$m technology and 70 nm technology with respect to on and off currents. This illustrates the magnitude of the problem.

As we had argued earlier, with feature size reduction, the static energy component of the on-chip caches constitutes a sizeable fraction total processor energy. Circuit techniques such as DVS\textsuperscript{14}, ABB-MTCMOS\textsuperscript{10} have been proposed to reduce the leakage energy in the caches. Control algorithms deploying these techniques estimate the active footprint in the cache to selectively power it. This results in performance penalty as well as in energy penalty in switching the cache lines back and forth from active to dormant state.

Gated-$V_{dd}$\textsuperscript{11} technique interposes a high-threshold transistor between the circuit and one of the power supply rails. Typically a gated-$V_{dd}$ SRAM cell will have an NMOS selectively connecting the cell to the ground rail. When the active signal is asserted, SRAM cell operates normally, but when active is de-asserted, the cell is disconnected from the ground, and the state contained within the cell is lost. The activation transistor and the control mechanism for active can be shared by all cells within a cache line to minimize the extra area needed by the control transistor. Thus this technique reduces the leakage current of a normal threshold transistor to effectively the leakage current of the high-threshold control transistor. For 0.18 $\mu$m technology with $V_{dd}$ as 1 V and control transistor with $V_{dd}$ as 0.4 V, 97% of the static leakage energy could be saved. But the only and the main disadvantage in this method is that the contents of the cache are lost. Hence the control algorithm should be smart enough to switch off the lines only when not needed.

In ABB-MTCMOS\textsuperscript{10}, the static-leakage current is reduced by dynamically raising the transistor threshold voltage, typically by modulating the back-gate bias voltage. In a typical circuit employing ABB-MTCMOS, during normal operation, when active is asserted, the SRAM is connected to $V_{dd}$ and ground and back-gate voltages are set to the appropriate power rails. When active is de-asserted, the PMOS wells are biased using an alternate power supply, $V_{dd}$, at a higher voltage level than the source terminals. And NMOS transistor wells are grounded while their sources are increased to higher voltage level through two diode drops. Thus all the transistors in SRAM experience higher threshold voltages and corresponding drop in leakage current. The drawbacks of this method are, higher energy/delay per transition (due to higher capacitance switching of power lines, both $V_{dd}$ and ground, N-Well, and P-Well consume more energy and takes more time), higher $V_{dd}$ offsets the leakage power savings.

DVS\textsuperscript{14} scales the voltage of (power line) cell to approximately 1.5 times $V_{dd}$ in standby mode. The state of the memory cell is also maintained at this voltage level, hence the state is not lost. In a typical sub-micron process (70 nm) leakage current increases exponentially with supply voltage. Hence by reducing the supply voltage to an optimum value (knee point of the curve), two-fold reduction (both voltage and current) of the leakage power is achieved. But the memory cell in standby mode cannot be accessed (read or written). Hence, access latency increases whenever a memory cell in drowsy state is to be accessed. The capacitance of power rail is considerably less than the capacitance of N-wells and P-wells. A transition from drowsy to normal state is therefore faster when compared with ABB-MTCMOS. Another drawback of this method is reduction in the ‘noise margin’ of the SRAM cell inverters. The voltage at which an inverter transits its state is given by, $V_{dd} = (r(V_{dd} - |V_p|) + V_m)/(1 + r)$, where $r = \sqrt{\beta_p/\beta_n}$.

![Fig. 1. Circuit with depletion device.](image-url)

Table I. Leakage current trend.

<table>
<thead>
<tr>
<th>Technology</th>
<th>$W_{eq}$ (nm)</th>
<th>$L_{eq}$ (nm)</th>
<th>$V_t$ (V)</th>
<th>$I_{leak}$ (nA/μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC [7]</td>
<td>200</td>
<td>100</td>
<td>0.35</td>
<td>0.05</td>
</tr>
<tr>
<td>BPTM [4]</td>
<td>70</td>
<td>38</td>
<td>0.20</td>
<td>53.96</td>
</tr>
</tbody>
</table>
Hence the $V_{dd}$ moves very close to one of the two states, making the SRAM very susceptible to noise. With this DVS scheme and a simple policy of switching all cache lines in L1 to drowsy mode every 2000–4000 cycles, achieves, on average, 71% static energy reduction. This translates into 50% overall cache energy reduction for 70 nm process. This clearly indicates that the static energy forms a considerable fraction of overall cache energy.

Power consumption in any digital integrated circuit, is given by the equation,

$$P_{total} = I_D V_{dd} + \alpha CV_{dd}^2 f$$  \hspace{1cm} (1)

where, \((I_d)\) is the leakage current, which is governed by the diode equation \((I_d(e^{V_{dd}/kT} - 1))\), \(V_{dd}\) is the power supply voltage, \(\alpha\) is the average switching activity factor, \(C\) is the total capacitance of the circuit, and \(f\) is the frequency of operation. The first term in the equation corresponds to the leakage power and the second term corresponds to the dynamic switching power. With the reduction in feature sizes, \(V_{dd}\) has also decreased, forcing a reduction in the threshold voltage \(V_t\) of the transistors. Thus the leakage current \((I_d)\) which depends on \(V_t\), through the diode equation (presented in the preceding discussion), increases. \cite{15}

A more elaborate expression for the sub-threshold leakage current is given by [Ref.\cite{16}, p. 201],

$$I_{ds} = A \exp\left(\frac{q}{nkT}(V_s - V_t - V_{MD} - \gamma V_t + \eta V_{dd})\right)B$$  \hspace{1cm} (2)

where,

\[
A = \mu_C C_{ox} \frac{W}{L} \left(\frac{kT}{q}\right) \right)^{1/2} e^{qV_{dd}/kT}
\]

\[
B = 1 - \exp\left(-\frac{qV_{dd}}{kT}\right)
\]

The leakage power decreases exponentially with respect to \(V_{dd}\) due to the Drain Induced Barrier Leakage effect. \cite{16} This fact has been used by earlier researchers in DVS \cite{17} and in Row-by-Row Dynamic \(V_{dd}\) Control (RRDV) Scheme. \cite{18}

We propose a novel technique using depletion mode devices to achieve a leakage reduction of 90% in SRAM arrays without any additional control mechanism. We call our SRAM as warm sram for the reasons explained in Section 3.

2. PROPOSED CIRCUIT TECHNIQUE

2.1. Circuit Operation

In order to achieve leakage reduction we should be able to dynamically control the voltages \(V_{dd}, V_G\) and \(V_t\). We use depletion mode devices to achieve this. A depletion device works in same way as the enhancement mode device, except that the device is ON even when the \(V_G\) is zero. To understand how depletion mode devices can help in leakage current reduction, consider Figure 1. Let, \(V_{T\text{high}}, V_{T\text{low}}, V_G\), and \(V_{dd}\) be the threshold voltages of the devices, such that

\[V_{T\text{high}} < 0, V_G > 0, V_{dd}\]

When the access signal ACC is HIGH, both the depletion devices are ON hence the virtual power and ground nodes \(V_{acc} = V_{dd}\) and \(V_{GND} = GND\). The circuit is in normal operation mode. When ACC is made LOW both depletion mode devices are switched-off and their \(V_{dd}\) is heavily reverse biased, i.e., for depletion NMOS \(V_{dd} = -V_{dd}\) and for Depletion PMOS \(V_{dd} = V_{dd}\). With \(V_{dd} = 0\) both of these depletion mode devices will be in deep sub-threshold region, hence will have very minimal leakage. One of the two enhancement mode devices will be leaking depending on the OUT state. Hence the charge stored in \(V_{acc}\) node starts getting accumulated in the node \(V_{GND}\). As \(V_{acc}\) decreases, (and simultaneously \(V_{GND}\) increases), the depletion mode NMOS (and PMOS) current increases. Note that the leakage of charge from \(V_{acc}\) to \(V_{GND}\) reduces the \(V_{dd}\) and increases the \(V_{dd}\) for the enhancement mode devices. The leakage current in the enhancement mode device reduces exponentially as the \(V_{dd}\) reduces, \(V_{dd}\) is reverse biased and the \(V_{dd}\) increases. Thus all the three factors in Eq. (2) come in to play and reduce the leakage current dramatically. The circuit reaches a stable point when the current supplied by depletion mode device is equal to the leakage current of the enhancement devices. If the threshold voltages are carefully chosen this equilibrium can be achieved at deep sub-threshold region of depletion mode device, hence reducing the leakage current in the circuit dramatically.

Intuitively, we can see that this equilibrium is reached when \(V_{acc}\) is closer to \(-V_{T\text{high}}\) and \(V_{GND}\) is closer to and \(V_{dd} = V_{T\text{low}}\). Thus \(\text{OUT}\) as \(HIGH\) and hence \(V_{acc} = V_{acc}\) across the NMOS enhancement transistor will be \(V_{T\text{low}} = V_{T\text{high}} - V_{dd}\). In order to differentiate \(V_{acc}\) from \(V_{acc}\), this \(V_{acc}\) is equal to \(V_{T\text{high}} - V_{T\text{low}} - V_{dd}\) > 0, resulting in \(V_{T\text{high}} - V_{T\text{low}} - V_{dd}\). The equilibrium condition of the circuit can be found by solving Eq. (2), substituting appropriate threshold voltages and equating all the currents. To have at-least a voltage difference of 0.3 V between \(HIGH\) and \(LOW\) and for \(V_{dd} = 1\) V, the above equilibrium condition requires (for the case \([V_{T\text{high}}] = [V_{T\text{low}}]\), \([V_{T\text{high}}]\) = 0.65 V. We used 70 nm technology model files provided by BPTM \cite{19} to perform the HSPICE \cite{20} simulation. We chose the following threshold voltages for the HSPICE simulation: \([V_{acc}] = [V_{T\text{high}}] = 0.2\) V, \([V_{T\text{low}}]\) = \([V_{T\text{high}}]\) = 0.65 V; \(V_{dd} = 1\) V. The steady state currents and voltages of different nodes are as given in Table II. In these measurements, the depletion mode transistors were opened (ACC made 1) for 1 ns and then closed. All the three signals, i.e., \(IN\), \(ACC\) and were driven by minimum sized inverters. Hence, they all have the same delay, rise and fall times.
2.2. Leakage Reduction and Performance Impact

Table I shows the leakage current of a minimum sized transistor to be (53.96 nA/μm) × 70 nm which is 3.77 nA. Compared to 10 pA leakage current from our scheme in Table II, we have achieved a leakage current reduction of 377 times, but with a penalty in performance. The performance impact of the extra NMOS access transistor in the charging path and PMOS access transistor in the discharging path could be high. Since these devices are depletion mode devices, this impact can be managed to a great extent. Various delay parameters are listed in Table III. There is a 54.5% increase in the average propagation delay which may not suit high-speed logic circuits. We can reduce the delay by several means. The easiest one is to make the ACC signal rise time slope higher (faster) compared to the input signal slope, or equivalently pre-raise ACC earlier than the input transitions. In this inverter, just by making the ACC rise 10 times faster than the input, we reduced the propagation delay penalty to 18%. But the increase in fall time, which is limited by the PMOS, is still 76%. We can increase the width of the depletion mode transistor, which unfortunately will also increase the leakage current. This is one of basic limitations of this circuit design style. The other limitation is the energy spent in switching \( V_{\text{PWR}} \) node. Note that whenever the input is 1 and \( AC = 1 \), the virtual power node is pulled up to \( V_{\text{AD}} \). However, during the inactivity period (\( AC = 0 \)), the virtual power node leaks some charge to the virtual ground which is about 0.65 V in our design. A complete energy estimate needs to take this switching of the \( V_{\text{PWR}} \) node between \( V_{\text{AD}} \) and \( V_{\text{TABPN}} \) into consideration. The \( V_{\text{PWR}} \) node has capacitance \( C_{\text{AD}} = 2C_{\text{DD}} \). Consider a 0.3 V swing between \( V_{\text{AD}} \) and \( V_{\text{TABPN}} \). The extra energy required then will be:

Extra switching energy = \( e = 0.3C_{\text{AD}} \)

If the circuit is idle for \( \Delta_t \) time, on average, after each active period, the switching will pay-off only if,

\[ \Delta_t \geq C_{\text{AD}} \times 7.9 \times 10^7 \]

Table III. Performance impact of circuit in Figure 1.

<table>
<thead>
<tr>
<th>( t_{\text{AD}} ) (ps)</th>
<th>( t_{\text{AD}} ) (ps)</th>
<th>( t_c ) (ps)</th>
<th>( t_L ) (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base 16.8</td>
<td>10.54</td>
<td>33.63</td>
<td>17.31</td>
</tr>
<tr>
<td>New 25.9</td>
<td>16.32</td>
<td>40.72</td>
<td>30.89</td>
</tr>
<tr>
<td>%Inc 54.2</td>
<td>54.80</td>
<td>21.10</td>
<td>78.50</td>
</tr>
</tbody>
</table>

This is because from Table I, the 70 nm leakage current is 53.96 nA/μm. With \( W_{\text{AD}} = 70 \) nm, this gives the leakage current as \((0.070 \mu \text{m}) \times (53.96 \text{nA/μm}) = 3.77 \text{nA}\). The leakage energy over time \( \Delta_t \) will equal \( 3.77 \times 10^{-8} \times \Delta_t \). For the leakage energy to exceed the extra switching energy of \( V_{\text{PWR}} \times 3.77 \times 10^{-8} \times \Delta_t \geq 0.3C_{\text{AD}} \), which leads to \( \Delta_t \geq C_{\text{AD}} \times 7.9 \times 10^7 \). With 70 nm technology and minimum width transistors, \( C_{\text{AD}} \) typically equals 0.1 fF hence \( \Delta_t \geq 7.9 \) ns. For typical high performance circuits, with clock cycle time as 0.2 ns, we get around 40 cycles as the idle time. Hence the dep-warmup CMOS circuit technique can be applied if the average idle time between active periods is far greater than this break-even window. The immediate application will be in SRAM arrays, which occupy more than 50% of the typical microprocessor's area and consumes more than 50% of the energy.

2.3. Cross Coupled Inverter

The circuit in Figure 1 is not truly regenerative in idle mode, i.e., as the devices are cascaded, the high output \( V_I \) of \( t \)-th stage is less than \( V_{\text{HI}} \) (of \( (t-1) \)-th stage). Similarly the low output \( V_L \) increases. But the \( V_L \) doesn’t go lower than \( V_{\text{TABPN}} \) and \( V_I \) doesn’t increase beyond \( V_{\text{LO}} - V_{\text{TABPN}} \). To find the leakage reduction in that case we can simply cross-couple the inverters and study the circuit. This will be the minimum leakage reduction possible through this method as \( V_{\text{PWR}} \) will be equal to \( V_{\text{IP}} \) and \( V_{\text{END}} \) will equal \( V_{\text{IO}} \). In this scenario, one of the factors in leakage reduction, reverse biased \( V_{\text{pb}} \), doesn’t exist. Leakage current for this cross-coupled inverter estimated using HSPICE\(^\text{™}\) is 515 pA. And \( V_{\text{PWR}} = \text{HIGH} = 742 \text{ mV} \). \( V_{\text{END}} = \text{LOW} = 225 \text{ mV} \). Even though the leakage current increases by 25 times (per inverter) when compared to circuit in Figure 1, we still have achieved a reduction of 12–15 times when compared to the original inverter. Moreover, the high and low levels are only 500 mV apart, and hence require less switching energy. Further reduction in leakage current is possible if multiple cross-coupled inverters share the same depletion device pair.

2.4. Other Applications

The circuit in Figure 1 is well-suited for clocked circuits, where the activity in the circuit is in sync with a clock. Another possible circuit design style with this principle to reduce leakage energy is shown in Figure 2. This circuit also has the charging and discharging timing characteristics of Table III except that either only charging or discharging path is active at any point of time. However, this design style requires each variable to be present in both original and complemented forms. Hence this style will be useful in differential signal design styles such as DCVS. In Ref. [20] Johnson et al. use stacking of transistors to reduce the leakage current. Our method can also be modeled similarly. In the case of low-power circuits, static
power is a major limitation in not moving towards smaller technologies. The proposed technique can then be used to reduce the static power with smaller technologies, hence achieving greater performance when compared to larger technologies without any increase in static power.

3. REDUCING STATIC ENERGY IN ON-CHIP CACHES

As we saw in Section 2, the immediate application of the dep-warmup-CMOS is in SRAM arrays. Hence, in this section, we study its application in caches. The latest processors have two or three levels of caches, namely L0, L1, and L2. L0 is closest to the CPU and L2 is closest to the main memory. To improve the performance, L2 caches are now made on-chip and sized up to 1 MB. In contrast, L1 cache sizes are typically 32 KB to 64 KB. L1 miss rates are on the average less than 2%, hence L2 will be very infrequently accessed when compared to L1. Given this, we validate our circuit design technique with L1 cache, which is in the critical path. If the scheme works with L1, we can infer that it will work with L2 as well (L2 has longer idle periods and is less critical for processor performance).

We use CACTI 3.0,13 as the base model to evaluate the performance impact. Cacti uses the underlying cache architecture shown in Figure 3, which explains the general cache architecture for an N-way set associative cache. The address decoder decodes the incoming address and selects the appropriate set or a row by driving one wordline in the data array as well as the corresponding wordline in the tag array. Every wordline corresponds to a set in the cache and contains as many bitlines as the number of bits in the set. Thus in an N-way set associative cache with block size B bytes, each wordline would drive $N \times B \times 8$ cells.

To reduce the switching power and the driving capacity of bitline drivers, each bitline is made to transit from $V_{DD}$ (1 V in 70 nm process) to $V_{pre}$ (bitline precharge voltage, 0.7 V in 70 nm process). Moreover, sense amplifiers are used to amplify this difference to produce the output data bits. Each sense amplifier monitors a pair of bitlines and detects a differential change. Determination of whether bitline or its complement goes low allows the sense amplifier to infer the memory cell’s contents. When a sense amplifier is shared among several pairs of bitlines, a multiplexer is inserted before the sense amps. These multiplexors are driven by the address decoder. All the bits from a set in an N-way set associative cache are read in parallel. These bits are logically grouped into N ways. To select only one of the ways, the address, which was read (from the tag array) concurrently with the data, is compared with the input address. Only the data from the matching way is sent to the CPU. Thus N comparators are needed for an N-way associative cache. Other techniques such as sub-arrays, block tiling, sub-banking are used to reduce the cache access time. However, in all the cache architectures, all the N-ways are still accessed concurrently and only the matching way is forwarded.

Cacti uses sub-arrays to reduce the bit-line and word-line delays. For a 32 KB 4-way cache with 32 B block size, Cacti finds the optimal configuration as 8 sub-arrays with each having 128 rows of 256 bits. The timing parameters for various components in a 32 KB, 32 B, 4-way, 1 RW port, 70 nm cache are given in Table IV. The cache access time for this configuration is 556.1 ps, which includes the data output driver delay of 76.2 ps. From Table IV it is clear that data array delay does not form the critical path in cache access timing. A 32 bit processor with this cache configuration requires a tag array of 19 KBits, which is just 7.4% of the data array size. Therefore, we apply our method of static leakage reduction only to data array, which is not in the critical path (increase in data array delay will not impact the cache access time), and consumes more than 92% of the static power in the caches.

We can use a depletion device pair per SRAM cell to reduce the leakage power as described in Section 2. However, this will increase the SRAM cell size, and hence the area increase will out-weigh the leakage power reduction. An alternative is to share the depletion mode transistors with multiple SRAM cells. The wordline access signal can be used to control the depletion devices since it already encodes the active periods of a SRAM cell. Hence, no additional control signals need be generated. There are two ways to share the depletion or the voltage clamp devices. As we saw in Table III the fall time $t_f$ is approximately 4 times the rise time $t_r$. We decided to increase the depletion PMOS width by a factor of 4. This leads to approximately equal $t_f$ and $t_r$. For an SRAM cell which is a cross-coupled inverter, write time is not the bottleneck...
as the cross-coupling effect aids in state transition. The read time is impacted only by the discharge path. Hence increasing depletion PMOS width alone is justified. From Table IV data, the data array delay is 85.2% of the tag array delay and data bitline delay is 2.73% of the data array delay. Hence up to 6 times increase in bitline delay will still not increase the overall cache access time. We try to exploit this fact in deciding the number of voltage clamp devices and their sizes. From Table III, we can share one depletion PMOS with 4 SRAM cells resulting in 4 to 5 times increase in the fall time \( t_f \). Based on our earlier calculation of \( t_r \) and \( t_f \), we can share one depletion NMOS with 16 SRAM cells. In our configuration, each word-line has 256 SRAM cells. For every group of 16 SRAM cells, one voltage clamping depletion device pair is used as shown in Figure 4. This dep-warmup CMOS configuration is compared with the base wordline configuration of 256 SRAM cells. The basic SRAM cell we use in HSPICE simulation is shown in Figure 5. We use low \( V_t \) devices

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**Table IV.** Cache access timing for a 32 KB, 4-way, 32 B, 1 RW port, 1 sub-bank cache as given by CACTI.

<table>
<thead>
<tr>
<th>Component</th>
<th>Data array delay (ps)</th>
<th>Tag array delay (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decoder</td>
<td>208.572</td>
<td>099.410</td>
</tr>
<tr>
<td>Wordline</td>
<td>115.975</td>
<td>044.415</td>
</tr>
<tr>
<td>Bitline</td>
<td>011.765</td>
<td>011.898</td>
</tr>
<tr>
<td>Senseamp</td>
<td>072.625</td>
<td>044.625</td>
</tr>
<tr>
<td>Compare</td>
<td>—</td>
<td>112.912</td>
</tr>
<tr>
<td>Mux driver</td>
<td>—</td>
<td>150.077</td>
</tr>
<tr>
<td>Sel inverter</td>
<td>—</td>
<td>016.612</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>408.936</strong></td>
<td><strong>479.949</strong></td>
</tr>
</tbody>
</table>

---

**Fig. 3.** General cache architecture of an \( n \)-way set associative cache.

**Fig. 4.** Warm SRAM wordline.
in the cross-coupled inverters and high $V_t$ devices for the access transistors, in order to reduce the leakage due to the access transistors. Except for the access transistors, all the other transistors have $|V_t| = 0.2$ V.

3.1. Leakage Reduction

The most relevant parameters of the proposed dep-warmup CMOS cache is the leakage reduction achieved by this circuit and the steady state voltages of the nodes. The current measurements presented in Table V are for a single SRAM cell. The steady state values were measured after a bit was written into the cell. When compared to the values presented in Section 2 for the cross-coupled inverter case, we see that $V_H$ has decreased, i.e., moved closer to $|V_t|$. This is because we have shared one depletion mode NMOS with 16 SRAM cells, hence the leakage current in the circuit has to decrease. All the 16 SRAM cells have to share the leakage current supplied by one depletion mode PMOS.

We can reduce the leakage current further by increasing the sharing but that will affect the transition delay and hence impact the performance. From Table V it is clear that we have achieved more than 23 times static power reduction. However, we need to assess the performance impact as well. The factor which will contribute to performance reduction is the delay in charging up $V_{PWR}$ node from 0.686 V to 1.0 V. In the following two sub-sections we will analyze the performance impact on write and read operations.

Table V. Steady state values of a WARM SRAM cell.

<table>
<thead>
<tr>
<th>Param</th>
<th>Base</th>
<th>Warm SRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_L$ (pA)</td>
<td>6250</td>
<td>262</td>
</tr>
<tr>
<td>$V_{(BIT)}$ (V)</td>
<td>1.0</td>
<td>0.666</td>
</tr>
<tr>
<td>$V_{(BIT)}$ (V)</td>
<td>0.0</td>
<td>0.252</td>
</tr>
</tbody>
</table>

3.2. Performance Impact on Write Operation

We performed HSPICE simulations on a subarray of size 128 rows by 256 columns (as given by Cacti) to study the impact on read and write times. Each bit and bitbar line was connected with a transmission gate to the bit value to be written, and with a PMOS transistor to precharge it to $V_{pre}$ for read operation. The wordline enable signal was generated using a delay estimated by Cacti. The values of the different parameters are given in Table VI. There are two assumptions involved in $V_L$ and signal delay parameters. First, the delay of $V_L$ is not affected by the addition of 16 $W_{min}$ depletion mode NMOS transistors. This assumption is valid as $V_L$ is already driving 512 $C_g$ of memory cell access transistors, and an addition of 16 $C_g$ does not increase the delay by more than 3% (or the driver could be sized to absorb this delay). Second, signal is generated from $V_L$ and since it is driving only 64 $C_g$, its delay can be made one tenth of the $V_L$ delay.

Table VI. Transient analysis parameters.

<table>
<thead>
<tr>
<th>Param</th>
<th>Value</th>
<th>Param</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$WL_{t_r}$ and $t_f$</td>
<td>100 ps</td>
<td>Base $t_t$</td>
<td>47.0 ps</td>
</tr>
<tr>
<td>$WL_{t_r}$ and $t_f$</td>
<td>10 ps</td>
<td>Base $t_t$</td>
<td>22.0 ps</td>
</tr>
<tr>
<td>$WL$ pulse width</td>
<td>200 ps</td>
<td>Warm SRAM $t_t$</td>
<td>50.1 ps</td>
</tr>
<tr>
<td>$V_{pre}$</td>
<td>0.5 V</td>
<td>Warm SRAM $t_t$</td>
<td>0.00 ps</td>
</tr>
</tbody>
</table>

Fig. 6. Transient analysis of write operation.
responses for the warm sram. It is clear from these values that the write operation is not getting affected by the presence of depletion mode devices. Firstly we are getting the advantage of depletion PMOS getting switched on ten times faster than the access transistors. Therefore $V_{\text{GID}}$ transits to zero even before access transistors are completely opened allowing bit to become zero with zero delay. Secondly since the bit transits from a non-zero initial value to $V_{\text{DD}}$, the peak current requirement for the transition is smaller. Thus the single depletion NMOS transistor is able to supply the required current for 32 inverter transitions. This fact also illustrates that the proposed circuit uses less energy for bit transitions.

However, the warm sram has one disadvantage in terms of energy, i.e., every time a bit is written, whether the bit is transitioning or not, it has to raise the $V_{\text{PWR}}$ node from $V_{\text{DD}}$ ($\approx 700$ mV) to $V_{\text{GND}}$. This also applies to the output node of an inverter which is in $V_{\text{DD}}$ state. Since $V_{\text{PWR}}$ node has capacitance $518C_{\text{diff}}$ (per wordline) and the output node of an inverter has capacitance $768C_{\text{diff}}$ (per wordline), this energy will approximately equal $327.9C_{\text{diff}}$. For 70 nm technology, $C_{\text{diff}}$ is in the range of $0.11 \text{ fF}$. Hence the extra energy spent will be approximately 36.07 fJ. Note that this extra energy is paid only when the memory cell bit does not change state due to this write. This is because the normal write scheme will not consume any energy in such a case, however warm SRAM will still need 0.14 fJ per bit (where state does not change). Hence, the extra write energy is proportional to the number of bits that do not change state. We calculated the write energy by integrating the input current. This energy is parameterized by the number of bit-transitions (bits changing state). The results are shown in Table VII. The first column of the table specifies the number of cells changing state. This table shows that warm sram consumes less energy than the conventional circuit even with 128 bits changing state (out of 256 in a single row/block). The break-even point is somewhere closer to the point where 70 bits change state. For a write with less than 70 bits changing state, the constant energy to raise $V_{\text{PWR}}$ and $V_{\text{out}}$ nodes for the bits not changing state dominates. This results in higher energy consumption for warm SRAM than for the conventional SRAM. Whenever a cache block is replaced, if we assume a uniform distribution of bit values, we will get on the average 128 bit transitions. For cache access writes, this depends on the access width. The warm sram will be spending at most 36.07 fJ extra energy for any access causing less than 64 bits to transit. When compared to the dynamic energy per cache access, which is estimated by Cacti as 0.3 nJ, this extra energy is very insignificant. Hence we can safely assume that it has little effect on the overall dynamic energy.

### 3.3. Performance Impact on Read Operation

The most critical operation in cache is read operation which occurs twice as often as writes. It is critical because load latency cannot be hidden. The instructions waiting on read results often stall. Whereas, the store (write) latency can be easily hidden using write buffers. No instructions in the immediate vicinity depend on the outcome of the write operation. The tag array access is, however, in the critical path in the cache read, as we observed from Table IV. Hence we can exploit this slack to make the data array path slower without impacting the same cache access time. This is the basis for the chosen depletion mode transistor widths. If we have to reduce the delay any further, we can reduce the degree of sharing, trading it with increase in leakage current. As per Cacti, bitline delay is defined as the delay between the time at which wordline enable is $OV$ and voltage difference between bit and bitbar becomes 100 mV. Cacti uses a precharge voltage of 0.7 V for the 70 nm technology and estimates the bitline delay to be 11.7 ps. We varied the precharge voltage from 0.7 V to 0.5 V in 50 mV steps to study its influence on bitline delay for both the base circuit and the warm sram circuit. The results are shown in Table VIII. The difference in Cacti’s estimation and our results can be attributed to the high-$V_{\text{th}}$ access transistors. Since we are interested in estimating the leakage savings in warm sram, we used high-$V_{\text{th}}$ access transistors in all the other reported simulation results. We used a pulse width of 200 ps for the wordline signal in our simulations. Warm sram bitline delay for 0.7 V and 0.65 V precharge voltages is greater than this 200 ps pulse width for the wordline. Hence, the bitlines did not achieve the 100 mV difference. Furthermore, since 0.5 V closely matches with Cacti’s estimation of the bitline delay, we use 0.5 V as our precharge voltage for all the further simulations. From Table VIII, it is clear that bitline delay increase for precharge voltage of 0.5 V and 0.55 V does not increase both cache access time as well as the wave pipelined cycle time. Thus warm sram does not have any performance impact on cache access time. The read operation for a 0.5 V precharge voltage is shown in Figure 7.

### Table VII. Energy comparison.

<table>
<thead>
<tr>
<th>No of bits</th>
<th>Energy (fJ)</th>
<th>Peak current (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Base Warm SRAM</td>
<td>Base Warm SRAM</td>
</tr>
<tr>
<td>256</td>
<td>320 144</td>
<td>5.53 0.997</td>
</tr>
<tr>
<td>192</td>
<td>240 132</td>
<td>4.14 0.930</td>
</tr>
<tr>
<td>128</td>
<td>160 118</td>
<td>2.75 0.840</td>
</tr>
<tr>
<td>64</td>
<td>80 99</td>
<td>1.36 0.735</td>
</tr>
</tbody>
</table>

### Table VIII. Bitline delay as a function of precharge voltage.

<table>
<thead>
<tr>
<th>$V_{\text{pre}}$ (V)</th>
<th>Base (ps)</th>
<th>Warm SRAM (ps)</th>
<th>%Inc</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.70</td>
<td>39.8</td>
<td>&gt;200</td>
<td>X</td>
</tr>
<tr>
<td>0.65</td>
<td>30.6</td>
<td>&gt;200</td>
<td>X</td>
</tr>
<tr>
<td>0.60</td>
<td>24.1</td>
<td>181.4</td>
<td>652.7</td>
</tr>
<tr>
<td>0.55</td>
<td>21.2</td>
<td>129.3</td>
<td>590.9</td>
</tr>
<tr>
<td>0.50</td>
<td>20.5</td>
<td>113.6</td>
<td>454.1</td>
</tr>
</tbody>
</table>
As is the case with write, read operation also requires extra energy to charge the nodes to \( V_{dd} \). This can be avoided if we don’t switch on depletion NMOS for read operation. This requires additional control logic and a separate driver for depletion NMOS transistors. This may not pay off since the extra energy spent for charging \( V_{\text{PWR}} \) and output node is at most 36 fJ (based on our prior estimation). This potential energy saving is insignificant when compared to per access dynamic energy of the cache. This energy estimate is worst case since the \( V_{\text{PWR}} \) node acts like a capacitor and is discharged by the leakage current in the circuit. The time the node takes to reach the steady state depends on the leakage current magnitude. It takes more than 200 ns to leak down to the steady state value from \( V_{dd} \) at room temperature \(( T = 25 \degree C)\) as shown in Figure 8. If the cache line was accessed again within this 200 ns period, we will spend less energy than 36 fJ on charging \( V_{\text{PWR}} \) and output node to \( V_{dd} \). We calculated the energy used per word line access for different inter-access time intervals. The results are shown in Table IX. These results are very close to our estimates. This also shows that if two accesses happen within 25 ns of each other, we don’t spend any extra energy compared to the base SRAM cell design. The reason why the warm SRAM energy is less than the base circuit at 25 ns inter-access
In the preceding sections we saw how warm sram: A Novel Scheme to Reduce Static Leakage Energy in SRAM Arrays. Gomathisankaran and Tyagi

Table IX. Read energy with respect to time after an access.

<table>
<thead>
<tr>
<th>Time (ns)</th>
<th>Energy (fJ)</th>
<th>Extra energy (fJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>23.99</td>
<td>–1.93</td>
</tr>
<tr>
<td>50</td>
<td>33.86</td>
<td>7.94</td>
</tr>
<tr>
<td>75</td>
<td>41.56</td>
<td>15.64</td>
</tr>
<tr>
<td>100</td>
<td>47.22</td>
<td>21.30</td>
</tr>
<tr>
<td>125</td>
<td>51.38</td>
<td>25.46</td>
</tr>
<tr>
<td>150</td>
<td>55.27</td>
<td>29.33</td>
</tr>
<tr>
<td>175</td>
<td>57.45</td>
<td>31.53</td>
</tr>
<tr>
<td>200</td>
<td>59.44</td>
<td>33.52</td>
</tr>
<tr>
<td>300</td>
<td>59.44</td>
<td>33.52</td>
</tr>
</tbody>
</table>

For warm SRAM, the case of base circuit as it is discharging more current. To charge the 4-way cache. The extra access energy for warm SRAM is static leakage energy savings for a hypothetical 32 KB, access times of a cache. In this section, we evaluate the reduce the leakage energy without impacting the read/write access times of a cache. From Table XII it is evident that more than 80% of the accesses occur within 100 cycles of another access. These numbers depend on the cycle time. We use both 0.2 ns and 0.5 ns as the cycle times to illustrate the energy savings. In both the cases, 100 cycles is less than 50 ns hence we penalize only the accesses occurring after more than 100 cycles from another access with 33.52 fJ. We chose 0.2 ns because it is the wave pipelined cache cycle time estimated by Cacti and 0.5 ns because it approximates the cache access time.

Another source of extra energy is the access control signals generation for the depletion NMOS and PMOS. Since depletion NMOS is driven by the wordline WL signal, we will not incur any extra energy for that. However, we have to generate this and will be approximately (1/8)th of the wordline driver energy (as this signal has to drive only 64WL, (1/8)th the capacitance driven by WL). From Cacti, the wordline energy is 158.95 fJ. Hence, we assess 19.87 fJ extra energy per access to generate signal. We take this into account as well while calculating the energy savings.

Table XI lists various benchmarks and the number of execution cycles for 500 Million instructions and the corresponding energy savings. The energy saving is calculated with the leakage currents given in Table V. For a 32 KB cache, this gives us the base leakage 1.638 mW while the warm sram leakage power as 68 µW. Using these figures and taking the energy penalty incurred by our method into consideration, we achieve a 90% reduction in leakage energy on average.
in a 32 KB data array (for both 0.2 and 0.5 ns cycle times) without impacting the cache access time. Table XIII lists the energy savings for various SPEC2000 integer benchmarks for both 0.2 ns cycle time and 0.5 ns cycle time.

DRG cache,\(^\text{21}\) which uses gate-grounded transistor to reduce sub-threshold leakage current in SRAM cell, achieves 26–27\% of energy savings with a performance penalty of 5.4\% in 70 nm technology. Thus our WARM SRAM achieves better leakage reduction with lesser performance impact.

4. MODEL VALIDITY

In all our HSPICE simulations, we have assumed that enhancement mode file model with its threshold voltage modified to suit the depletion device’s characteristics. We justify the validity of this assumption in this section. We discuss only the depletion NMOS case, however the discussion is equally applicable to depletion PMOS as well. Note that existing CMOS processes typically do not support depletion mode devices since it requires an extra mask. However processes evolve to support the devices prevalent in a period. If deep-warmup-CMOS style gains favour with designers, the processes will normally evolve to accommodate it. It is not an issue of technical feasibility.

Depletion NMOS is formed by implanting donor atoms in the substrate. The threshold voltage of such a device is given by Eq. (3) \([\text{Ref. [17], p. 238]}\):

\[
V_t = V_{th} + \gamma (\sqrt{\phi_{bn} + V_{bn}} - \sqrt{\phi_{tn}}) \tag{3}
\]

Where,

\[
V_{th} = V_{bn} + \phi_{bn} - \frac{qN_d d_i}{C_{ox}} \left(1 + \frac{d_i C_{ox}}{2\epsilon_{ox}}\right) + \gamma (\sqrt{\phi_{bn}})
\]

\[
\gamma = \left(1 + \frac{d_i C_{ox}}{\epsilon_{ox}}\right)\gamma
\]

\[
V_{bn} \rightarrow \text{Flat band voltage}
\]

\[
\phi_{bn} \rightarrow \text{Built in potential} (\phi_{tp} - \phi_{bn})
\]

\[\gamma \rightarrow \text{Body effect coefficient of the unimplanted substrate}\]

\[d_i \rightarrow \text{Implantation depth}\]

\[N_d \rightarrow \text{Donor concentration}\]

Note that a depletion mode transistor has higher body effect compared to enhancement mode devices. Hence \(N_d\) and \(d_i\) should be varied to get the required device characteristics. The first point of consideration is that the depletion NMOS should get cut-off when \(V_{th} = 0.65 \text{ V}\) and \(V_{pe} = 0 \text{ V}\). Hence by equating 3 to \(-0.65 \text{ V}\), we can solve for \(N_d\) and \(d_i\).

The second point of consideration is that when \(V_{th} = 1 \text{ V}\) the gate should have gain comparable to what is predicted by the enhancement mode model. If these two operating points can be verified then our circuit will yield a similar result if we use proper depletion model for the devices.

There are four regions of operation in a depletion device,

1. Cut-off—device is completely depleted at the source end.
2. Surface depletion—surface is depleted but the buried channel exists conducting the current.
3. Surface accumulation—as \(V_{th}\) increases beyond threshold, inversion occurs and carriers are accumulated on the surface.
4. Surface accumulation/depletion—as \(V_{th}\) or \(V_{bd}\) increase beyond a certain value, it depletes the channel on one of the sides making the device behave like a saturated enhancement mode device.

Our operating points should be in cut-off and surface accumulation regions. The device enters surface accumulation region if \(V_{th} > V_{pe}\) where \(V_{th} = V_{th} + \phi_{bn}\). The gain of the device in surface depletion region is given by \(\beta = \mu_b C_{ox}/(1 + \sigma)\), where

\[
\sigma = \frac{C_{ox}d_i}{\epsilon_{ox}} \left(\frac{C_{ox}d_i}{2\epsilon_{ox}} + 1\right)
\]

Even though \(\mu_b\), bulk mobility, is typically larger than the surface mobility, the factor \((1 + \sigma)\) tends to reduce
the gain in surface depletion region when compared to the enhancement mode device. Once surface accumulation occurs the variations of channel charge with $V_{dd}$ occur at the surface, and, thus, the gain is determined by the surface mobility and oxide thickness only. In other words the gain is comparable to the enhancement mode device. One problem with depletion device could be that if the implantation depth is too high then controlling the buried junction just with gate voltage will not be possible as the surface inversion will occur before pinch-off condition could be reached. This can be overcome if the depth is not made very large or with high $V_{dd}$ the buried channel could be depleted. In our circuit since both drain and source are always above 0.65 V this condition can never occur.

The process parameters for the 70 nm technology we are considering are,

$N_{sb}$ → Substrate doping concentration = 6 x 10$^{16}$ cm$^{-3}$

$N_{ch}$ → Channel doping concentration = 1.2 x 10$^{18}$ cm$^{-3}$

$X_{j}$ → Junction depth = 299.99 x 10$^{-10}$ m

$\gamma$ → Oxide thickness = 16 x 10$^{-10}$ m

$\gamma$ → Body effect coefficient of bulk = 6.563 x 10$^{-2}$

We can solve Eq. (3) for various values for $\gamma$, i.e., $d_{f}$ for the condition $V_{dd}$ = 0.65 V. We can then choose the solution closest to our assumptions. The various values of $N_{sb}$ and $\gamma$ for various $d_{f}$ values are listed in Table XIV.

Note that there are various possible solutions but we should choose the one with the lowest $\gamma$. Depending on the process and the maximum $N_{ch}$ allowed, the device has to be scaled to take into account the decrease in the gain. In all these cases, note that $V_{dd}$ < 0 hence both $V_{dd}$ and $V_{dd}$ are >$V_{dd}$. This places the device in surface accumulation region when switched on. Hence, our assumption of validating the warm sram circuit technique with enhancement device models is justified. With proper depletion mode models, we can verify other characteristics of the device such as subthreshold leakage characteristics. However, to within a first order approximation, our circuit can achieve the claimed static energy reduction.

5. CONCLUSION

The static leakage energy is one of the biggest challenges facing the semiconductor industry in the near to intermediate term future (3–10 years). The static energy consumption grows exponentially with reduction in feature size. On-chip caches occupy a major fraction of the processor’s area. This holds both for high performance and for low power embedded processors. Since static leakage energy constitutes a large fraction of cache energy, and hence of total processor energy, on-chip caches form a good target for static energy reduction techniques. We proposed, modelled, and verified a new CMOS design style, warmup CMOS. These devices operate best when warmed up like an engine, where some of the key nodes have attained a certain potential. The warming-up cost is paid only once for each activity period, but the savings more than offset the initial warmup cost. The specific version of warmup CMOS presented in this paper is based on depletion mode devices—dep-warmup CMOS. We presented a SRAM cell design in dep-warmup CMOS and its block level implementation. The detailed SPICE simulations estimate the static leakage energy savings for L1 caches at more than 90% without any affect on the performance. We are further investigating other warmup CMOS design styles and their application to broader logic blocks.

Acknowledgments: The authors would like to acknowledge support from NSF Grant CCR 0209078 and AFRL through contract number F33615-02-C-1238.

References


Table XIV. Process parameters for depletion NMOS

<table>
<thead>
<tr>
<th>$\gamma$</th>
<th>$d_{f}$ (10$^{-6}$m)</th>
<th>$\sigma$</th>
<th>$N_{ch}$ (10$^{16}$ cm$^{-3}$)</th>
<th>$V_{dd}$ (V)</th>
<th>$V_{dd}$ (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5y</td>
<td>24.21</td>
<td>0.625</td>
<td>28.2</td>
<td>-0.6786</td>
<td>-37.06</td>
</tr>
<tr>
<td>2.0y</td>
<td>48.41</td>
<td>1.5</td>
<td>14.23</td>
<td>-0.6881</td>
<td>-54.84</td>
</tr>
<tr>
<td>3.0y</td>
<td>100</td>
<td>5</td>
<td>5.667</td>
<td>-0.7084</td>
<td>-78.78</td>
</tr>
</tbody>
</table>


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