High-Precision Current-Based CMOS WTA/LTA Filters

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Abstract
The design, simulation and implementation of high-precision current-based CMOS WTA/LTA filters are reported. The circuits are fast, compact and exhibit a high resolution and a low-power consumption. Therefore, they result attractive to be used in massive parallel processing structures, i.e. neural networks. HSPICE simulation results are presented in AMIS 0.5μm technology. In addition, experimental results are reported with monolithic NMOS and PMOS transistors.

1. Introduction

Maximum and Minimum (MAX/MIN) are inherent operators of nonlinear systems such as nonlinear filters, fuzzy systems and artificial neural systems. Therefore, MAX/MIN operators are widely used in a large variety of nonlinear signal processing procedures, including image processing, pattern recognition and data compression, to name a few. CMOS MAX/MIN circuit realizations are available in both, digital and analog fashion. Their choice depends on the features required by the system in which they are going to work.

Analog CMOS MAX/MIN processors are usually known as “Winner-Takes-All” and “Loser-Takes-All” (WTA/LTA) circuits. The operation of a WTA circuit consists of identifying the largest input value among its N external inputs. On the other hand, the operation of a LTA circuit consists of finding the smallest input value among its N external inputs. Depending on the nature of signals they deal with, analog WTA/LTA circuits can be classified in three main groups[1]: charge-mode, voltage-mode and current-mode filters. The current-based approaches have been most frequently employed for processing information directly from sensors and transducers. This is the case, for example, of many photodetectors, which transform optical signals into electrical signals in current-mode. In the present work, we focus on the current-based circuits.

Numerous analog CMOS WTA/LTA architectures have been reported by different authors in literature[2-10]. Some of the most popular WTA/LTA current-mode circuits are showed in Figure 1.

Figure 1. Some of the most popular current-based WTA/LTA architectures.
The WTA of Lazzaro is one of the most employed current-based circuits. As can be appreciated in figure 1, it has a very compact cell with only two transistors. Unfortunately, it is highly mismatch sensitive. Moreover, it demands large swings of voltage at common node, $V_X$, in order to inhibit to the “loser” cells, resulting in a low-speed operation. Numerous authors have tried to improve the circuit of Lazzaro. This is the case of DeWeerth and Fish, who in order to overcome the disadvantage of low-speed operation, have added hysteresis to Lazzaro’s cell by means of a local feedback loop, as depicted in figure 1, thus enlarging the speed of the cell. Nevertheless, the cell still presents mismatch sensitivity.

The advantage of the nonlinear processor proposed by Demosthenous is its low-power dissipation. However, as we can appreciate in figure 1, it presents large area requirements because of its $O(N^2)$ complexity. Therefore, it results impractical for many applications. In general terms, when several external inputs to the operator are required, mismatch and complexity become important constraints because the area requirements are enlarge and precision is reduced. This is not the case of the structure proposed by Serrano, which exhibits a high-precision with an $O(N)$ complexity. The motivation of Serrano was to design a high-performance WTA with multi-chip capability. The main drawback with this cell is the need of compensation to ensure stability.

The processor of Gwo-Jeng consists of a complex design. It exhibits a fast processing rate but at the same time, low-resolution and large area requirement because of the large number of transistors involved. The Cheng’s circuit presents a high resolution. Unfortunately, it possesses $O(N^2)$ complexity and consequently its area requirements are large. On the other hand, the circuit reported by Ramirez is a feedforward cell based on the flipped voltage follower working with low voltage supply (1.5V). Thus, compactness and low power consumption are achieved In addition, since no large voltage swings at internal nodes occurs, the processing rate is not slowed down. Moreover, by controlling the current sink at the common node, the rank order from a set of input signals can be extracted.

Some of the architectures reviewed not only compute the maximum or minimum from a set of input signals but also some other nonlinear operations such as the median and the rank order. Thus, rank order filtering can be applied. The circuit proposed by Siskos has the maximum, minimum and median operations available. It presents a high processing rate. However, it also has a complex operation and a large area requirement, as can be seen in figure 1, due to its $O(N^2)$ complexity. Another analog rank order processor was proposed by Poikonen. It presents $O(N)$ complexity and is mismatch sensitive.

### 2. The nonlinear MAX/MIN operation

A mathematical model that realizes the nonlinear MAX operation and exhibits $O(N)$ complexity is presented as follows. Consider a current system of $N$ cells, such that each cell $j$ produces an output $I_{0j} = x_j H(I_j - I_0)$ with $j = 1, 2, \ldots, N$. $H(\cdot)$ is the step function, $I_j$ the external input to the $j_{th}$ cell, and

$$I_0 = \sum_{j=1}^{N} I_{0j} = \sum_{j=1}^{N} \alpha_j H(I_j - I_0) \quad (1)$$

![Figure 2](#).

**Figure 2.** Model and analysis of the system: (a) the mathematical model, (b) the current approach which accomplishes the model and (c) the analysis of the cell.
Figure 2(a) represents graphically the functions \( f_j(I_0) \), which is set by equation (1) and \( f_0(I_0) = I_0 \). Their intersection provides the solution of (1). If the parameter \( \alpha_j > 0 \) for all \( j \) (\( \forall j \)), (1) has a unique equilibrium point \( S \). Furthermore, if \( \alpha_j \geq I_j \) (\( \forall j \)), then the value of \( I_0 \) at the equilibrium point \( S \) is set by \( I_0 = \max(I_j) \) and the cell that drives a nonzero output, \( I_0 \neq 0 \), is the winner. If each input \( I_j \) is changed to \( I_j - I_0 \), where \( I_0 \) is an upper bound for all input, an LTA or MIN circuit results.

Figure 2(b) shows a current mode circuit that implements the operation of one cell for the case \( \alpha_j \equiv I_j \). It consists of a two-output current mirror, a digital inverter, and a MOS transistor. Each cell \( j \), receives two input currents, \( I_j \) and \( I_0 \), and delivers one output current \( I_0 \). The inverter acts as a current comparator. If \( I_0 > I_j \), the inverter output \( v_{o0} \) is low, the MOS transistor is OFF, and \( I_0 \) is zero. On the other hand, if \( I_0 < I_j \), the inverter output \( v_{o0} \) is high, then the MOS transistor is ON and \( I_0 = I_j \).

Figure 2(c) shows the equivalent circuit of a cell. By means of circuits analysis, it is possible to prove that the dynamics of the cell can be modeled by the following first order nonlinear differential equation [5]:

\[
C_c v_{o0}(t) + C_c (v_{o0}(t) - v_{M}) + I_j = I_0(t) = \sum_{j=1}^{N} I_{0j} \tag{2}
\]

where \( C_c \) is the total capacitance available at node \( v_{o0} \), \( C_c \) is the total conductance at this node and \( v_{M} \) is the inverter swing voltage.

By applying Lyapunov stability analysis to expression (2) it has been found that conditions for asymptotical stability are [5]:

\[
AM < \frac{C_c}{\alpha_j} \left( \frac{\alpha_j}{C_p} + \frac{\alpha_j}{C_g} \right) \tag{3}
\]

where \( A \) is the gain of the inverter, \( M \) is the number of cells, \( \alpha_j \) is the total transconductance at the output of the circuit, \( \alpha_j \) is the parasitic capacitance at the output node and \( C_g \) is the parasitic capacitance between the inverter and the source of the NMOS switch.

The Pole splitting technique can be applied in order to attain stability. By adding a compensation capacitor to between the input of the inverter and the source of the NMOS switch, as illustrated in figure 2(c), the new conditions for stability are:

\[
C_A > \frac{\alpha_j}{\alpha_j / C_g + \alpha_j / C_p} \tag{4}
\]

Note that now the stability condition does not depend on gain \( A \) and it is easier to fulfill. However, now capacitor \( C_A \) degrades the setting speed of the system. Capacitor \( C_A \) acts as a Miller capacitance.

3. Design of the WTA/LTA circuit

As described earlier in section 1, there are several criteria to evaluate the performance of a WTA/LTA circuit. Nevertheless, it is difficult to find a cell which gathers high resolution, high speed response, compactness and low power consumption. Since these figures of merit are desirable in many nonlinear signal processing tasks, i.e. neural networks, the design of a circuit which performs appropriately under those issues is needed. We propose a new current-mode WTA/LTA circuit based on the Serrano’s structure that suits in a better way the demands discussed earlier.

![Figure 3. Block diagram of the current-based WTA/LTA circuit.](image-url)
is to follow the largest input signal value.

The most difficult about the design of the system is to ensure its stability. Because of the nonlinear nature of the system and the feedback loop, the Lyapunov stability criterion must be applied. A first order model from the circuit’s dynamic behavior is carried out and by means of the pole splitting technique an asymptotically stable circuit within the dynamic range can be achieved [11].

Figure 4. High precision current-based CMOS MAX/MIN operators proposed: (a) LTA, (b) WTA

Figure 5. Simulation Results: (a) 5 inputs WTA circuit, (b) 5 inputs LTA circuit, (c) layout.

Figure 6. Experimental Results: (a) 2 inputs WTA circuit, (b) 2 inputs LTA circuit.
Table 1. Results obtained compared with other architectures proposed in literature.

<table>
<thead>
<tr>
<th>Author/Year</th>
<th>Technology</th>
<th>Min Diff. Reached [\mu m]</th>
<th>Size [\mu m²]</th>
<th>Power [mW]</th>
<th>Voltage Supply [V]</th>
<th>Proc. Time [ns]</th>
<th>Operation capabilities</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lazzaro (1995)</td>
<td>2.0 \mu m</td>
<td>2</td>
<td>0.013</td>
<td>5.09</td>
<td>5</td>
<td>30-50</td>
<td>MAX function available</td>
</tr>
<tr>
<td>DeWeerth (1995)</td>
<td>NR</td>
<td>2</td>
<td>NR</td>
<td>5</td>
<td>5</td>
<td>5-15</td>
<td>MAX function available</td>
</tr>
<tr>
<td>Serrano (1995)</td>
<td>2.0 \mu m</td>
<td>1</td>
<td>0.070</td>
<td>1.96</td>
<td>5</td>
<td>20-300</td>
<td>MAX function available</td>
</tr>
<tr>
<td>Domenhers (1996)</td>
<td>2.4 \mu m</td>
<td>&lt;1</td>
<td>NR</td>
<td>0.15</td>
<td>5</td>
<td>110</td>
<td>MAX function available</td>
</tr>
<tr>
<td>Sistores (1999)</td>
<td>1.2 \mu m</td>
<td>5</td>
<td>NR</td>
<td>3</td>
<td>3</td>
<td>30</td>
<td>MAXMINMEDIAN functions available</td>
</tr>
<tr>
<td>Guo-Jeou (2000)</td>
<td>0.6 \mu m</td>
<td>16.5</td>
<td>NR</td>
<td>0.125</td>
<td>5</td>
<td>25</td>
<td>MAX function available</td>
</tr>
<tr>
<td>Polisoven (2002)</td>
<td>0.18 \mu m</td>
<td>1</td>
<td>NR</td>
<td>NR</td>
<td>NR</td>
<td>100-300</td>
<td>RANK ORDER functions available</td>
</tr>
<tr>
<td>Chien-Cheng (2003)</td>
<td>0.35 \mu m</td>
<td>&lt;1</td>
<td>NR</td>
<td>3.3</td>
<td>NR</td>
<td>4</td>
<td>MAX function available</td>
</tr>
<tr>
<td>Fish (2005)</td>
<td>0.35 \mu m</td>
<td>3</td>
<td>0.0006</td>
<td>0.89</td>
<td>3.3</td>
<td>12</td>
<td>MAX function available</td>
</tr>
<tr>
<td>Proposed (2005)</td>
<td>0.5 \mu m</td>
<td>250*</td>
<td>0.007</td>
<td>1.8</td>
<td>1.8</td>
<td>5-20</td>
<td>MAXMIN functions available</td>
</tr>
<tr>
<td></td>
<td></td>
<td>250*</td>
<td>LTA 0.008</td>
<td></td>
<td></td>
<td>5-20</td>
<td></td>
</tr>
</tbody>
</table>

* Input Range = 250 nA - 400 nA
** The highest frequency for acceptable performance = 100KHZ, @ 100KHZ proc. time = 80ns

The design of the system was made with a CMOS technology in a similar fashion to that proposed by Serrano. We employ CMOS current mirrors, MOSFET transistors as switches and a CMOS inverter as the current comparator. Figure 4 shows the architecture of our design. The difference compared with the Serrano’s structure is the current mirror used, Serrano chose the simple current mirror and we chose the flipped-voltage current mirror (FVCM). The election of the FVCM enhance the performance of the circuit since the mismatch effect of the simple current mirror is minimized [12]. Thus, the offset effect is reduced with no significant losses in the dynamic range[13]. Moreover, the power supply value is bounded by the inverter and even with the election of the lowest riel value allowed, the FVCM exhibits a good-enough dynamic range. Since the power consume is determined almost totally by the inverter, the election of the lowest riel value allowed reduces the power consume. The speed response is also determined by the inverter, so, an appropriate selection of the size of the PMOS and NMOS must be done. Unfortunately, due to the compensation the settle time is slowed down. However, the band of frequency obtained is good-enough to accomplish image processing, for instance nonlinear filtering tasks like impulsive noise removal and/or edge detection[14].

4. Results

A five inputs WTA and a 5 inputs LTA have been design and simulated. A voltage supply of 1.8V is employed and a bias current of 50\mu A flows through every single cell. The design proposed was carried out using double poly AMIS 0.5\mu m technology. Figure 5 (c) shows the corresponding layouts. TANNER L-EDIT was used in the elaboration of the layouts.

Simulations results obtained with HSPICE and showed in figure 5(a) and 5(b) correspond to Montecarlo analysis from the extracted circuit of 5(c). The Drennan mismatch model was used [15]. 5 triangular inputs were supplied. 30 iterations were executed corresponding to the 99% from all possible variations cases. As can be appreciated, WTA/LTA filters with high precision performance was reached. In order to verify the functionality of the architecture proposed, monolithic implementation of a two inputs WTA and a two inputs LTA with NMOS and PMOS transistors from advance linear devices inc were also implemented. Figure 6 shows the results obtained. As can be appreciated, both WTA and LTA functions were effectively performed. Finally, the summarized results of our design and comparisons with other architectures are showed in table 1.
5. Conclusions

The design and simulation of high precision current-based CMOS WTA/LTA filters in double poly 0.5μm technology have been presented. Simulation results set that compared with other approaches, the circuit proposed performs appropriately under four figures of merit: high resolution, high speed operation, low power consumption and compactness. These features make it attractive to perform in massive parallel nonlinear signal processors, i.e., neural networks. The circuit has been fabricated, we are actually waiting for the chip to realize all the corresponding measurements. In addition, experimental results obtained with monolithic ALD1106 NMOS and ALD1107 PMOS transistors have been also reported. Those results have been useful to verify the functionality of the proposed circuits.

5. References


