Abstract — In this paper, a novel three-dimensional space vector algorithm for four-legs multilevel converters is presented. It can be applied to active power filters or neutral current compensator applications for compensating harmonics and zero sequence using natural coordinates. This technique greatly simplifies the selection of the 3-D space where a given voltage vector is supposed to be found. The algorithm drastically reduces the algorithm complexity and the calculations of the active vectors with the corresponding switching time which generate the reference voltage vector. In addition, the low computational cost of the proposed algorithm is always the same and it is independent of the number of levels of the converter.

I. INTRODUCTION

Four-leg multilevel converters are finding relevance in active power filters and fault-tolerant three-phase rectifiers with capability for load balancing and distortion mitigation thanks to their ability to meet the increasing demand of power ratings and power quality associated with reduced harmonic distortion and lower EMI [1][2].

A four-leg multilevel converter permits a precise control of neutral current due to an extended range for the zero sequence voltages and currents. In Fig. 1 a four-leg diode clamped three-level inverter is shown. This topology presents the advantages of four-leg voltage source converters [3] and the corresponding to the multilevel converters [4].

In [6], a new 3D-SVM in abc natural coordinates is applied to conventional four-leg voltage source converters showing the advantages of using these coordinates. The first generalized 3D-SVM algorithm for multilevel converter was proposed in [7][8]. This three-dimensional algorithm is a generalization of the well-known 2D-space vector technique [9][10][11][12], reducing the control complexity and the computational load. The space vectors will be in a plane if the system is balanced [9]. However, it is necessary to generalize to a 3D-space if the system is unbalanced or if there is zero sequence or triple harmonics because the reference vectors are not on a plane.

In this work, a very simple 3D-modulation algorithm for four-leg multilevel converters based on the generalized 3D-SVM algorithm for three-leg multilevel converters, proposed in [7], is presented. The computational cost of the proposed method is very low and it is independent of the number of levels of the converter. This technique can be used as modulation algorithm in all applications that provide a 3D-vector control.

II. MODULATION TECHNIQUE DESCRIPTION

A. Reference vector synthesis

Since the switching of any power topology stays at discrete states, space vector modulation is used to approximate a reference voltage vector \( u_{ref} \) calculating the time to its closest state vectors. The modulation law requires the actual voltage vector \( u \) to equal its reference value \( u_{ref} \), which is represented in the stationary reference frame. During each modulation sub-cycle of duration \( T_m \), a switching sequence is generated. It is composed of four switching state vectors \( u_1(t_1), u_2(t_2), u_3(t_3), \) and \( u_4(t_4) \), where \( t_1, t_2, t_3, \) and \( t_4 \) are the on-state durations of the active switching state vectors. The four vectors nearest to the reference vector must be identified. The proposed 3D-SVM algorithm easily calculates the four state vectors which generate the reference vector in four-leg multilevel power converter systems. Thus, the reference vector will be pointing to a volume which is a tetrahedron into a cube of the prism. The vertexes of that tetrahedron are the state vectors of the switching sequence. In addition, the...
algorithm permits to obtain the corresponding duty cycles without using tables or trigonometric functions. The modulation algorithm input is the normalized voltage vector. The normalization only depends on the number of levels of the multilevel converter, \( n \), and the voltage level value of the DC-link capacitors, \( V_{DC} \) [4]. In general, the reference vector must be scaled by the normalization constant: \( \sqrt{\frac{2}{3}} \frac{V_{DC}}{n-1} \) to be into the range \{-\( (n-1) \),..., \( (n-1) \}\}.

However, the algorithm and the graphics add the term \( (n-1) \) for considering the range between \{0, ..., 2\( (n-1) \)\}, simplifying the representation.

**Step 1:** Calculate the coordinates of the sub-cube reference vertex where the reference vector is found. The space vectors of a four-leg multilevel converter form a prism in a 3D-space. This space can be decomposed into several cubes, where six tetrahedrons generate the total volume of each cube. The 3D-prism containing the state vectors which generates the reference vector in four-leg three-level converter is shown in Fig. 2.

For a certain reference vector in three-phase coordinates \((u_{an}, u_{bn}, u_{cn})\), the integer part of each component \((a, b, c)\) is calculated, where:

\[
\begin{align*}
    a &= \text{integer} (u_{an}), \\
    b &= \text{integer} (u_{bn}), \\
    c &= \text{integer} (u_{cn}).
\end{align*}
\]

Where \(u_{an}, u_{bn}, u_{cn} \in \{0, ..., 2(n-1)\}\).

The cubes into the 3D-prism space is formed by a certain number of sub-cubes depending on the number of the levels of the converter. Only one sub-cube for two-level converters, eight sub-cubes for three-level converters, twenty-seven sub-cubes for four-level converters. In general, \((n-1)^3\) sub-cubes into each cube, where \( n \) is the number of levels of the multilevel converter. However, it is important to notice that there are another sub-cubes located between the cubes and each plane prism that also belong to the control space. They must be taken into account in the modulation algorithm. The coordinates \((a, b, c)\) are the origin coordinates corresponding to the reference system of the sub-cube where the reference vector is pointing to.

**Step 2:** Six tetrahedrons are considered in each sub-cube. Therefore, it is necessary to define the tetrahedron where the reference vector is pointing to. This tetrahedron is easily found using comparisons with three 45° planes into the 3D space which define the six tetrahedrons inside the sub-cube.

**Step 3:** Once \((a, b, c)\) coordinates are known, the main step of the algorithm consists in calculating the four space vectors corresponding to the four vertices of a tetrahedron into the selected sub-cube (in step1). These vectors will generate the reference vector. Configurations of the 3D space with different number of tetrahedrons into the cube have been studied. However, the minimum number of comparisons is obtained using the six tetrahedrons shown in Fig. 6.

**Step 4:** Control space.

Whatever normalized reference vector is supposed to be found into the 3D-prism space. However, the prism total volume is not totally covered by the cubes corresponding to each multilevel converter. For this reason, if a given reference vector is located into a tetrahedron, where one of its vertices is out of the prism planes, the algorithm modulation assigns switching time equal to zero to this space vector. It is due to the reference vector is pointing to a plane prism and the three nearest space vectors, located on this plane prism, will generate it. This case is showed in Fig. 7.

**Step 5:** Calculation of the switching times.

The new algorithm calculates the four state vectors on-line into the 3D-prism space and the corresponding duty-cycles using a maximum of three comparisons for calculating the suitable tetrahedron. The algorithm modulation is so easy due to the 45° planes of each cube and the prism planes are coincident, as it is showed in Fig. 8.

Fig. 2. Generalized 3D-space for a four-leg three-level converter

Fig. 6. Tetrahedrons into each cube with the corresponding state vectors.
B. General structure of the algorithm

The flow diagram of the proposed 3D-modulation algorithm for four-leg multilevel converters for choosing the tetrahedron where the reference vector is pointing to is shown in Fig. 9.

Notice that the algorithm is extremely simple. The computational load is always the same and it is independent of the number of levels. In addition, the algorithm provides the switching sequence that minimizes the commutations number of the semiconductor devices.

III. CALCULATION OF DUTY-CYCLES

Once the state vectors which generate each reference vector are known, the corresponding duty-cycles are calculated. The algorithm generates a matrix $S$ with four state vectors and the corresponding switching times $t_i$. Where $S_{an}$ $S_{bn}$ $S_{cn}$ with $i = 1, ..., 4$ are the coordinates of each state vector and $d_i$ is the corresponding duty cycle.

\[
S = \begin{bmatrix}
S_{an} & S_{bn} & S_{cn} & d_1 \\
S_{an} & S_{bn} & S_{cn} & d_2 \\
S_{an} & S_{bn} & S_{cn} & d_3 \\
S_{an} & S_{bn} & S_{cn} & d_4 \\
\end{bmatrix}
\]  

Where $T_m$ is the sample time.

The state vectors are the vertexes of the corresponding tetrahedron that generates the reference vector. The equations to be solved are the following:

\[
\begin{align*}
ua &= S_{an} d_1 + S_{bn} d_2 + S_{cn} d_3 + S_{dn} d_4, \\
ub &= S_{an} d_1 + S_{bn} d_2 + S_{cn} d_3 + S_{dn} d_4, \\
uc &= S_{an} d_1 + S_{bn} d_2 + S_{cn} d_3 + S_{dn} d_4, \\
d_1 + d_2 + d_3 + d_4 &= 1.
\end{align*}
\]

The numeric evaluation of the duty cycles or on-state durations of the switching states are reduced to a simple addition as it is shown in Table I.

The coordinates $(a, b, c)$ represent the different voltage levels between each phase and the neutral. They take values between zero and $2(n-1)$, where $n$ is the number of levels of the multilevel converter. The duty cycles are only functions of the reference vector components and the integer part of reference vector coordinates. In addition, the optimized switching sequence is selected in order to minimize the switching number. The new algorithm calculates on-line the four state vectors into the 3D space and the corresponding duty-cycles using only a maximum of three comparisons for calculating the suitable tetrahedron. The computational load is always the same and it is independent of the number of levels of the multilevel converter.

V. RESULTS

The algorithm has been successfully implemented. The considered conditions are a 55 \( \Omega \) resistive load, a 1.2 mH smoothing inductance, a 10kHz switching frequency and a 40V dc-link voltage. The algorithm has been successfully simulated using Matlab (Simulink). The simulated results for the four-leg multilevel converter have been obtained using a continuous model formulated in terms of control functions. The experimental results have been obtained thanks to a real prototype using a TMS320VC33 DSP microprocessor.

In order to prove the proposed technique an unbalanced voltage reference composed of a fundamental component with 20V amplitude, 20% of zero sequence and 20%...
Experimental results for phase c voltage

 Experimental results for phase b voltage

 Experimental results for phase a voltage

 Table I: States Sequence and switching times.

\[
\text{Case } 1.1: (S_{1_{a_{n}}}, S_{3_{a_{n}}}, S_{5_{a_{n}}}) = (a, b, c) \\
\quad d_1 = 1 + a - u_{an} \\
\quad d_2 = -c + u_{cn},
\]

\[
\text{Case } 1.2: (S_{1_{a_{n}}}, S_{3_{a_{n}}}, S_{5_{a_{n}}}) = (a + 1, b, c + 1) \\
\quad d_1 = 1 + a - u_{an} \\
\quad d_2 = b - c - u_{bn} + u_{cn},
\]

\[
\text{Case } 1.3: (S_{1_{a_{n}}}, S_{3_{a_{n}}}, S_{5_{a_{n}}}) = (a + 1, b + 1, c + 1) \\
\quad d_1 = 1 + a - u_{an} \\
\quad d_2 = b - c - u_{bn} + u_{cn}.
\]

 Another reference vector containing a fundamental component with 20V amplitude, 20% of zero sequence and 20% inverse sequence has been used. Voltage reference for each phase is represented in Fig. 10. Voltage references of each phase are illustrated in Fig. 11(a), 12(a) and 13(a). The simulated results of this experiment are shown in Fig. 11(b), 12(b), 13(b) and the experimental results are shown in Fig. 11(c), 12(c), 13(c).

Fig. 11 Voltage for phase a composed of a fundamental component with 20V amplitude, 20% of zero sequence and 20% inverse sequence

Fig. 12 Voltage for phase b composed of a fundamental component with 20V amplitude, 20% of zero sequence and 20% inverse sequence

Fig. 13 Voltage for phase c composed of a fundamental component with 20V amplitude, 20% of zero sequence and 20% inverse sequence

Another reference vector containing a fundamental component with 40/3^{1/2}V amplitude and 120% of the third harmonic has been proved for the sake of clarity. Voltage reference for each phase is illustrated in Fig. 14. The voltage reference, the simulated results and the
Experimental results of this experiment are shown in Fig. 15. Clearly, the voltage signal across the phase resistor follow the input reference signal. These results show the good performance of the proposed algorithm.

**IV. CONCLUSIONS**

The 3D space vector modulation algorithm for four-leg multilevel converters presented in this work is very useful to readily calculate the switching sequence and the on-state duration of the respective switching state vectors corresponding to the space vector modulation used in multilevel converters. The proposed technique directly allows optimizing the switching sequence minimizing the number of switching in four-leg systems. The computational complexity is very low and independent on the number of levels of the converter. This algorithm does not use trigonometric functions or look-up tables. It has been satisfactorily implemented in very low-cost microcontrollers. This technique can be used as modulation algorithm in all applications needing a 3D control vector such as four-leg active, where the conventional two dimensional space vector modulation can not be used.

**V. REFERENCES**