Validation of and Delay Variation in Total Ionizing Dose Hardened Standard Cell Libraries

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Abstract—A ring oscillator based test structure with special power multiplexing to allow accurate active and standby (leakage) power measurements with minimal test chip pin count is presented. This structure is used to validate radiation hardened by design (RHBD) standard cell library gates for TID hardness and delay. Additionally, the performance of standard commercial two-edge gates and their annular counterparts are also compared experimentally. The gate delay and energy per transition is shown to be significantly increased for some RHBD gates over their two-edge counterparts. Large ring oscillator delay variations are also shown, even with all test die from the same wafer.

I. INTRODUCTION

A standard cell library is a key element in VLSI design to automate logic design and allows automatically placed and routed (APR) logic layouts. Recently, there has been increasing emphasis on designing hardened ICs for spacecraft and other harsh environments using radiation hardening by design (RHBD) rather than more costly specialized processes [1][2]. There are many tradeoffs in cell library design, including cell selection and cell height. These choices are both constrained and complicated when using an RHBD methodology.

This paper describes the implementation of a 90 nm standard cell library supporting logic synthesis with APR. Comparisons are made against non-hardened but otherwise identical library cells. We also describe the test structures used to validate the library. The library is portable between two versions of the process, having different gate lengths, allowing rapid design migration between them. A novel ring oscillator with power multiplexing is used to validate the library hardness, delay and power. The experimental results demonstrate excellent hardness by less than 2% increase in standby leakage current after 1.6 Mrad(Si) Co-60 irradiation.

A. Total Ionizing Dose Effects

Total ionizing dose (TID) effects are produced when ionizing radiation creates electron-hole pairs within the oxides [3]. Sub-5 nm gate oxides allow carriers to escape. Consequently, the isolation oxides, i.e., shallow trench isolation (STI), are the most vulnerable to TID effects in modern microcircuits. The overall effect of TID is a negative shift in MOS transistor threshold voltage (Vth). NMOS transistors suffer from increased leakage current with TID from two primary components. Drain-to-source leakage in a single NMOS transistor is produced by a reduction in the Vth at the transistor edges, i.e., the interface between the thin and thick oxides [4]. Here, positive charge trapped at the STI edge increases the source-to-drain leakage current Ioff. Leakage paths are also created under the STI between diffusion areas, i.e., between NMOS sources or drains at different biases or from an NMOS source/drain diffusion to the N type well.

B. Radiation Hardening by Design

Designers of hardened circuits face difficult engineering tradeoffs. Special hardened processes, which are due to low volumes, more expensive, generally lag the commercial state-of-the-art. The requisite hardness may also be reached by clever micro-architecture, circuit design, and layout. The latter approach, which can use of the latest commercially available fabrication processes, is known as radiation hardening by design RBHD [1][2].

RHBD for TID mitigation focuses on layout techniques. Using annular, or edgeless, transistors can significantly reduce NMOS transistor drain-to-source leakage increase due to TID, since the same bias is then applied across any transistor edge that intersects the isolation oxide. By creating a back to back diode structure interrupting any current path created by trapped positive charge, P+ guard rings effectively mitigate leakage increases due to TID between adjacent N+ diffusions. These guard rings also help to protect against SEL.

C. Paper Organization

The motivation for this work has been briefly described in Section I. The test structure used to characterize the library is presented in Section II. Section III explains the standard cell design, focusing on RHBD considerations. Section IV covers the energy and delay measurements of RHBD and two-edge gates. The TID results for the RHBD and two-edge gates are described in Section V. The conclusion comprises Section VI.

II. TEST STRUCTURE

Ring oscillators are commonly used to electrically characterize standard cells. Generally, multiple pins per structure (at least one independent power and output pin) make the structure design simple, but wastes test chip area by making the test chip pin-limited. The power multiplexed ring oscillator standard cell characterization test structure uses power and output multiplexing (see Fig. 1) requiring only three power pins for all the ring oscillators. VDD supplies the control logic with power, VDDX supplies power to the ring oscillator that is selected for the current test and VDDY supplies power to the remaining ring oscillators, i.e., those whose output is not selected. A decoder selects between the ring oscillators and one global enable controls all the ring oscillators.

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oscillators. This approach reduces the number of pins to \( N+5 \) for \( 2^N \) ring oscillators. This reduced pin count allows the ring oscillators to efficiently share the same test die with other test structures.

The power and leakage of each ring oscillator can be independently measured at the test chip pins. Since \( V_{\text{DDX}} = V_{\text{DDY}} \), the power multiplexing does not affect the power supply current measurements, since the same potential is applied to both sides of the multiplexing transistors. All of the ring oscillators include enables to ensure proper startup.

Both RHBD and equivalent two-edge gate ring oscillators are included in the test structure. Transistors are sized to provide the same drive current for the different versions. Oscillators with different inputs switching and output multiplexing allows comparisons of gate delay, energy per transition and leakage current for the RHBD and non-RHBD gates, as well as an analysis on the different switching characteristics between annular transistors with their drains on the outside versus the inside.

III. STANDARD CELL LIBRARY DESIGN

The annular NMOS transistors can impact both the drive current and leakage substantially and complicate the modeling and extraction [5]. Example cell library gate layouts are illustrated in Fig. 2 to illustrate the implementation of the annular transistors, guard rings and well/substrate taps. There are full diffusion stripes below both the \( V_{\text{DD}} \) and \( V_{\text{SS}} \) power rails to reduce the likelihood of single event latchup (SEL) or well bias collapse. All N-type diffusions at different potentials are separated by P-type guard rings. The library is portable between the low standby power (LSP) and standard versions of the 90 nm bulk CMOS target process. The former requires 20 nm longer gates, and thus sets the transistor sizes. The standard process gate lengths are shrunk, but the diffusion contact locations are the same.

A. Annular Transistor Impact and P/N Ratio

On a 90 nm process, the minimum sized annular transistor requires 3× greater area than the minimum sized two-edge transistor and the minimum width is increased by about 6×. The annular transistors increase the active power dissipation due to increased transistor gate width, increased interconnect and intermediate stack capacitance. The NAND2 gate in Fig. 2 (middle top) illustrates the latter; the stack node between the NMOS transistors is necessarily on the outside of both annular transistors and has about 5× the capacitance as a conventional two-edge gate stack.

Most commercial libraries choose the PMOS/NMOS width ratios to optimize the overall power delay product of the gates. This results in a PMOS to NMOS width ratio of about 1.5 despite an approximately 3× NMOS and PMOS transistor mobility difference [6]. RHBD cells often use equal drive currents to limit the single event transient (SET) duration on a hit collected by the N+ diffusions. In our library, power/performance is the optimization target, setting the PMOS to NMOS ratio to approximately 1.5.

B. Cell Height

The cell height determines the overall packing density. We chose our library cell height to maximize the transistor packing density and minimize metal usage, while comprehending the required spacing for guard rings and the continuous \( V_{\text{DD}} \) and \( V_{\text{SS}} \) tap diffusions at the cell top and bottom. P-type guard rings also increase the standard cell size. The inability to cross the guard rings with polysilicon requires metal 1 (M1) for every CMOS transistor pair. This also reduces the ability to route within the cells using M1. As shown in Fig. 2, the cell height allows two NMOS transistors above one another, increasing the density of NAND gates and latches. The library uses three different annular NMOS transistor sizes of 1, 1.4, and 2 units. Multiples of these produce larger cells by combining transistors in parallel. This allows the synthesis tool to choose a larger or smaller gate in the same \( \sqrt{2} \) relative increment from any size except the minimum.

Cell selection and size granularity are important
considerations in cell library design [7] including for hardened
ASICs [8]. Researchers have shown that good results can be
obtained with relatively small cell libraries [7] for a limited set
of designs. Nonetheless, the library richness significantly
impacts APR block speed and density. The RHBD library here
contains about 40 unique logic functions with 260 cells.

IV. EXPERIMENTALLY MEASURED ENERGY AND DELAY

Twenty fabricated ring oscillator test structures were tested
(see Fig. 3). All came from the same wafer. The relative
difference in delay and energy per transition between the logic
gates with annular and two-edge transistors is shown in Figs.
4 and 5, respectively. The annular inverters, NAND gates with
the top (a) input switching, and NOR gates with both inputs
switching independently have a gate delay that is up to 10%
larger than their two-edge equivalents. While slower, the
energy per transition and leakage of the RHBD gates is
greater, allowing us to quantify the performance and power
impact of TID mitigation on a gate by gate basis. As the gate
transistor width increases, the impact of RHBD diminishes,
evident by comparing the 010, 014, and 020 gates, which have
NMOS widths of 1, 1.4, and 2 units, respectively.

The annular NAND gates with the slower (bottom NMOS
(b)) input switching have a gate delay that is significantly
larger, by 10% to 25%, than their two-edge equivalents. This
is due to the increased capacitance on the intermediate node
(see Fig. 1), and the drive strength difference between the
annular transistor with its drain on the inside versus the
outside. The impact is largest for the narrowest gates. The 010
two input RHBD NAND gate has over 5× greater intermediate
node capacitance than the two input two-edge NAND gate.
The drive current (I_{DSAT}) of an annular transistor with the
drain on the outside is 15% less than with the drain on the
inside, which also contributes to the greater NAND delay.

The energy per transition of the RHBD gates with the fast
(a) input switching is increased due to higher capacitance in the
poly “neck”, which adds input gate capacitance but does
not contribute to current drive. With the slower (b) input
switching, the higher RHBD gate switching energy is
attributed to high intermediate node capacitance. As transistor

gate width increases, the effect diminishes.

In many cases, the RHBD standard cell leakage current is
significantly greater than that of their two-edge equivalents,
ranging up to 47% more. The annular transistor topology
increases DIBL for the source inside topology. The leakage
current for the annular inverters is approximately 20% larger
than the same inverters with two-edge transistors. As NOR
gate total transistor width is dominated by the PMOS
transistors, the leakage impact is less.

V. EXPERIMENTAL TID RESULTS

A. Total Ionizing Dose Testing

Two test chips were irradiated in a Co-60 Gammacell at
approximately 1 krad(Si)/min. Measurements were taken at
200, 400, 600, 1000, and 1600 krad(Si). All measurements
were taken “in-situ” while the device under test (DUT) was
being irradiated. An initial test showed no significant I_{DSAT}
measurement effect due to photocurrents. A post anneal
measurement was taken 20 minutes after the DUT was
removed from the Gammacell.

One DUT was irradiated while the oscillators were running,
to simulate an operating CMOS microcircuit. The rings were
briefly halted using the enable signal to measure leakage
currents at each measurement point. The RHBD standard cells
showed no significant increase in gate delay, energy per
transition or leakage current up to and including the 1.6
Mrad(Si) dose (see Fig. 6).

Another DUT was irradiated while the oscillators were
halted to simulate the worst case situation. I_{AVG} is the average
oscillators only show the average delay, so this is essentially the within-die systematic variability. Fig. 7 plots the two-edge and RHBD inverter and NOR2 gate delays with the minimum unit and 2× NMOS gate widths vs. the speed of the same gates with 1.4× gate width. The trend is clear for both gates, but some annular gate ring oscillators fall considerably off the trend line. In general, the two-edge inverters have a tighter distribution, while the NOR2 gates have similar groupings.

Modern processes have a preferred polysilicon gate direction. In the cell library here the long annular transistor edge follows this direction, but substantial current flow is through the other direction due to the loops at the end. Gate corners require a longer channel length, resulting in a longer than minimum average gate length. Some ring oscillators show substantial deviations in delay as gate width increases, which could manifest as larger RHBD path level variability.

VI. CONCLUSION

A 90 nm RHBD cell library design and characteristics have been described. The cell height was chosen based on both wiring complexity and annular transistor packing. A novel power and output multiplexing ring oscillator test structure has also been described, which can maximize test silicon area utilization when characterizing delay, active power, and leakage of standard cell libraries. The RHBD library has been shown to have excellent TID hardness, proven experimentally above 1.5 Mrad(Si) to have no significant increase in cell ISB. Significant differences in energy and delay are manifested between RHBD cells and their two-edge counterparts.

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REFERENCES