A Nanowatt ADC for Ultra Low Power Applications

Karim Abdelhalim
Carleton University
Department of Electronics
5170 Mackenzie Building
1125 Colonel By Drive
Ottawa, Ontario K1S 5B6
kabdel@doe.carleton.ca

Leonard MacEachern
Carleton University
Department of Electronics
5170 Mackenzie Building
1125 Colonel By Drive
Ottawa, Ontario
leonard@ieee.org

Samy Mahmoud
Carleton University
Systems and Computer Engineering
Room 4456 Mackenzie Building
1125 Colonel By Drive
Ottawa, Ontario
mahmoud@sce.carleton.ca

Abstract—An 8-bit successive approximation analog-to-digital converter (ADC) for ultra low power applications is presented. It is designed in a standard 0.13μm CMOS process technology. The design can operate with low voltage supplies down to 0.45 V. It makes use of sub-threshold transistor operation to achieve nanowatts of power consumption at sample rates exceeding 60kS/s. A specially designed switch allows large input swings. Post layout simulations show an INL and DNL of approximately 0.3LSB and 0.45LSB respectively.

I. INTRODUCTION

Some applications such, as found in the biomedical field, require ultra low power consumption as opposed to high speed operation. By combining the low power consumption advantages of a successive approximation register ADC architecture with low power sub-threshold analog and digital design techniques, an ultra low power ADC can be designed. Using a standard 0.13μm CMOS technology, an 8-bit ADC was designed that functions down to voltages as low as 0.45 V while consuming nanowatts of power. This paper presents an ADC that provides ultra low power consumption and medium resolution for sample rates as low as 1kHz to sample rates as high as 150kHz. This is ideal for biomedical applications as input signals are often less than 1kHz and low power consumption is a necessity if the circuit is to be implanted inside the human body or if it is to be used in a battery powered device such as a pacemaker or hearing aid. Section 2 of this paper presents the circuit architecture of the ADC. Section 3 describes the design of each component. Section 4 provides post layout simulation results of the ADC and its components.

II. CIRCUIT ARCHITECTURE

The circuit uses a successive approximation architecture based on charge redistribution. This architecture uses a binary weighted capacitor array as the digital to analog converter needed for the successive approximation ADC. This architecture was demonstrated for ultra low power applications in [1]–[3]. It provides low power consumption because it only requires one comparator, no sample and hold circuitry, low frequency CMOS digital logic and analog switches. There are four main phases during the conversion cycle, as described in [4]: [i] First the analog data is sampled onto the bottom plate of the capacitors as \( V_{in} \), while the top plate is grounded as shown in Fig. 1. [ii] Next, the charge is then held as the bottom plates of each capacitor become grounded, forcing the top plate to reach negative \( V_{in} \) as shown in Fig. 2. [iii] Next, the approximation stage occurs as shown in Fig. 3 where the digital SAR logic controls the switching starting with the most-significant bit (MSB) and the comparator controls whether the voltage is positive or negative at the top plate of the binary weighted capacitor array. If the voltage on the top plate is positive then the approximation was too high, so this bit is considered to be a 0 and the top plate is returned to its negative value as before. If the voltage stays negative, then this bit is considered to be a 1 and the new negative voltage on the top plate is kept. This is repeated for each bit, thus the conversion phase will take \( n \) clock cycles, where \( n \) is the number of bits. [iv] After the least-significant bit (LSB) is reached, the digital data is valid and a new conversion cycle begins. The full conversion should take approximately \( n+3 \) clock cycles, one for sampling the analog signal, one for forcing it negative, \( n \) for approximating, and one for outputting the digital data.

III. CIRCUITS

A. Comparator

In order to reduce power consumption at low sample rates, the comparator was designed to operate in the sub-threshold
MOSFET regime where the current of the MOSFET is given by [5]:

\[ I_{DS} = I_{DS0} \frac{W}{L} e^{\frac{V_{GS} - V_T}{V_{Tn}}} \] (1)

in which \( W \) and \( L \) are the width and length of the MOSFET respectively, \( V_T \) is the thermal voltage, and \( I_{DS0} \) and \( n \) are process parameters. For a \( V_{DD} \) of 0.5V a gate-to-source bias voltage of 0.1V was selected which puts the transistor deep into sub-threshold operation. A \( V_{GS} \) of 0.1V provides accurate modeling and allows for ultra low bias current for the comparator. The comparator outputs a digital 1 if a negative voltage is present and a digital 0 if a positive voltage is present at the gate of M1 in Fig. 4. The circuit uses a differential amplifier with active PMOS loads (M3 and M4) and zero threshold transistors which are available in this CMOS process at the inputs (M1 and M2) as seen in Fig. 4. The amplifier was designed for maximum gain centered at 0V to compare negative and positive voltages. A CMOS inverter is placed at the amplifiers load to force the output to either a digital 1 or 0.

B. Capacitor Array

The capacitors were implemented using MIM-caps. The LSB capacitor was chosen to be approximately 50fF, which was implemented by placing 4 capacitors of 200fF in series for matching purposes. The MSB uses 32 capacitors of 200fF in parallel giving a capacitance of approximately 6.4pF. A 12 by 10 array of 200fF MIM-caps was used for the capacitor array, with dummy capacitors placed around the ring of the capacitor array to minimize mismatch on the outer capacitors. Interconnects were routed in a higher level metal, and the smaller capacitors were placed closer to their respective switches in order to reduce their interconnect capacitance.

C. Switch for Top Plate of Capacitor Array

With voltages reaching as low as negative \( V_{REF} \) it is difficult to use a simple NMOS transistor to reset the top plate of the capacitor array because \( V_{GS} \) becomes significant and charge loss occurs from the capacitor array which results in errors at the output, especially at low sample rates.

A solution to this problem is to use the switch shown in Fig. 5. The control signals for this switch are shown in Fig. 6. First, \( \text{Precharge} \) goes high, while \( \text{Control} \) is held low. This turns on transistor M1 and applies GND + \( V_{TP} \) to the top plate of the capacitor while the bottom plate of the capacitor has \( V_{DD} \) applied to it. Next, \( \text{Precharge} \) goes low, while \( \text{Control} \) goes high. With transistor M1 off, GND is then applied to the bottom plate of the capacitor. This forces the voltage at the top plate of the capacitor array to become close to negative \( V_{DD} \). This allows transistor M3 to remain on allowing the top plate of the capacitor array to be grounded during the sampling phase of the analog signal. Transistor M2 is a high threshold NMOS (0.6V) which helps prevent charge leakage from the capacitor array when the capacitor in Fig. 5 is being charged and discharged. The control signals for this switch are generated from the successive approximation digital logic by
adding a single additional AND gate. Transistor M3 has its n-well connected to GND when resetting the capacitor array to prevent any increase in $V_{TP}$ due to the body effect. Once the analog to digital conversion begins, the n-well gets connected to $V_{DD}$ which prevents latch-up when the drain of M3 reaches positive voltages.

D. Successive Approximation Register and Switch Array

The successive approximation register uses static CMOS digital logic operating in the subthreshold regime. The SAR logic was based on [3]. Extra circuitry was added to generate control signals for the switch described in the previous section and to reset the digital logic after each conversion cycle. Each switch is implemented using a standard CMOS transmission gate. The transistor sizes were larger for switches loaded by a large capacitor (more significant bit), to match the delays through the switches.

IV. SIMULATION RESULTS

The ADC was designed in a 0.13μm CMOS technology using 0.171mm$^2$ of chip area. All simulation results include the effects of parasitics extracted from the layout.

A. Comparator Power Consumption

The comparator’s power decreases exponentially with decreasing $V_{DD}$. This is because current in the sub-threshold operation is governed by equation (1). As the bias voltage decreases with $V_{DD}$, the current decreases exponentially. Even at $V_{DD}=0.8V$, the power dissipated by the comparator is far less than the power dissipated by the SAR digital circuit.

B. Comparator Monte Carlo simulation

The comparator’s average switching point is approximately one LSB when a $V_{DD}$ of 0.5V and a $V_{REF}$ of 0.256V is used based on process and mismatch variations as simulated together in a Monte Carlo statistical analysis. With an improved layout this figure should drop significantly closer to the expected 0mV. Simple calibration techniques were added to allow for tuning after tape-out. The comparator’s power consumption varied between 32nW and 144.1nW due to the exponential current relationship of the sub-threshold region, however its maximum power of 144.1nW is still low when compared to the digital SAR controller.

C. Comparator Summary

The comparator is designed for a $V_{DD}$ of between 0.45V to 0.8V. At a $V_{DD}$ of 0.5V the comparator provides enough bandwidth for sample rates as high as 70kS/s while consuming only 63.1nW of power. This provides enough bandwidth as the ADC can provide a maximum of 10kS/s when a $V_{DD}$ of 0.5V is used.

D. ADC Linearity Results

Fig. 7 shows INL results for all 256 codes. The INL excluding capacitor mismatch for this ADC was determined to be 0.3LSB.

The maximum DNL excluding capacitor mismatch as shown in Fig. 8 is determined to be 0.45 LSB, and is typically between 0.15LSB and -0.25LSB.

E. Dynamic Results

A 1 kHz sine wave was input into the ADC at 60.3kS/s, the FFT of the output is seen in Fig. 9. The signal-to-noise-
and-distortion ratio (SNDR) was 49.7dB giving an effective number of bits (ENOB) of 7.97. The spurious free dynamic range (SFDR) was 58.8dB. A 10 KHz sine wave input gives an SNDR of 45.2dB and an ENOB of 7.22 at 60.3kS/s.

**F. Power Consumption**

For supply voltages of 0.4 V and 0.6 V the digital SAR circuit consumes 70.4nW and 166nW respectively for a sample rate of 100 kS/s. As $V_{DD}$ increases and the sample rate increases, the power consumption of standard CMOS logic increases as

$$P = CV_{DD}^2f$$

and may consume more power than other components in the ADC. A $V_{DD}$ of 0.6V leads to the ADC using only 8.97pJ per conversion cycle as seen in Table I. These results exclude gate leakage current due to electron tunneling, as our models do not take this into account during simulations. However, a pessimistic estimate from our process guide adds less then 4nW of total power to the entire ADC when a $V_{DD}$ of 0.6V is used. This amount is much smaller then the total dissipated power of the ADC.

**G. Summary of ADC Results.**

The simulated results including parasitics based on full layout are summarized in Table II. The core layout is shown in Fig. 10. It uses approximately 0.171mm$^2$ of area. The capacitor array uses the majority of chip area as expected.

V. SUMMARY

An 8-bit ADC was designed for ultra low power applications and low sample rates such as those found in the biomedical field. By using sub-threshold operation and low power digital design techniques the ADC dissipates only 538nW of power at a sample rate of 60kS/s. As $V_{DD}$ is increased higher sample rates can be achieved but the digital logic begins to dissipate more power then other components of the circuit. The chip in a standard 0.13μm CMOS technology requires an approximate layout area of 0.171mm$^2$ for the ADC.

VI. ACKNOWLEDGEMENTS

Recognition goes to Scott Miller for setting up the design tools kits for the 0.13μm CMOS technology and NSERC and NCIT for funding this work.

REFERENCES


