New threshold voltage definition for undoped symmetrical DG MOSFET

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Abstract

A new threshold definition is proposed for symmetrical undoped double gate MOS (DGMOS). Threshold voltage is calculated using the potential model described in [1] with only two fitting parameters, the values of which do not depend on device geometry. Comparison with the results of numerical simulations and other models of $V_T$ is presented and good accuracy of the new model is demonstrated.

1. Introduction

Double gate structure provides reduction of short channel effects [2] allowing for more aggressive channel-length scaling. In the case of very small devices undoped channels make it possible to eliminate statistical fluctuations of doping concentration [3]. In such conditions the classical definition of the threshold voltage based on the Fermi level does not apply. Unfortunately, new definitions proposed in [4,5] neglect the dependence of threshold voltage on body thickness or gate oxide thickness. The analysis presented in [6] while interesting does not lead to a convenient, analytical formula. Other models [7,8] were tuned to achieve good agreement with DIBL or threshold voltage roll-off, but the absolute threshold voltage calculated according to these models is still less accurate than the model proposed in this paper.

2. Threshold definition

A simplified cross-section of the considered device is shown in Fig. 1. The new 1D definition of the threshold voltage is based on the relationship between surface potential and gate voltage (simulated using ATLAS [9] and shown in Fig. 2). Two regions of this relationship may be observed: subthreshold and above threshold. In Fig. 1 the new 1D definition of the threshold voltage is based on this phenomenon. The threshold voltage is the gate voltage at which the following condition is fulfilled:

$$\phi_S = V_G - \Delta \phi_S \quad (1)$$

where $\phi_S$ is the surface potential, $V_G = V_S - V_T$ the difference between the gate-to-source voltage and flatband voltage, and $\Delta \phi_S$ is the fitting parameter.

Using the relationship between gate voltage and surface potential proposed in [1] threshold voltage may be described as:

$$V_{th} = \frac{kT}{q} \ln \left( \frac{\phi_0 + \phi_{MAX}}{\sqrt{2kTn_i^*}} \right)^2 + e^{\phi_{MAX}} + \Delta \phi_S \quad (2)$$

$\phi_{MAX}$ is the maximum value of the potential in the middle of the channel (see Figs. 1 and 2) and

$$a = \frac{\phi_0(V_G - V_{th})}{\phi_{MAX}} \quad (3)$$

Other symbols in (2) have their usual meaning. Although our approach ignores the quantum phenomena and short-channel effects, it is useful because it reduces the complexity of mathematical description.

3. Comparison with numerical simulations

The fitting parameters $\Delta \phi_S$ and $a$ are determined by means of numerical simulations of transfer characteristics using ATLAS [9] and extraction of threshold voltage from these characteristics (based on the maximum of the second derivative [3] for $V_{DS} = 10 \text{ mV}$). The best agreement is obtained for:

$$\Delta \phi_S = 1.1 \frac{kT}{q}$$

$$a = 0.795$$

A comparison between several models and the values of threshold voltage extracted from the characteristics simulated numerically is presented in Figs. 3 and 4 as a function of channel thickness and gate-oxide thickness, respectively. Both, the models and simulations neglect quantum effects. The values of the fitting parameters of the models taken from the literature are as stated in the original publications. As it was mentioned before, the model of Taur [4] is independent of channel thickness in contrast to the results of the simulations. Its dependence on the dielectric thick-
ness is in quantitative agreement with the simulations, but the accuracy is the worst of all models over the whole range of tox. The model of Chen et al. [5] generally underestimates the value of threshold voltage and fails to saturate at thicker channels, moreover, it does not take into account the dependence of VT on dielectric thickness. The model of Shih and Wang [7] is in qualitative agreement with the simulation results both in terms of tSi and tox dependence, but overestimates the values of threshold voltage. The model presented in [8] is quite good for all investigated gate oxides and thin channels, but fails completely for thicker tSi. The model presented in this paper offers the best accuracy over the whole range of the considered channel and gate-oxide thicknesses and its error does not exceed 10 percent.

4. Summary

A new threshold definition is proposed stating that threshold takes place when the difference between surface potential and gate voltage is sufficiently high. The model of the threshold voltage based on this definition is simple and has only two fitting parameters. With constant values of these parameters it shows good agreement with the values extracted from the simulated characteristics in the range of device parameters (channel and gate-oxide thickness) interesting from the point of view of aggressive miniaturization. Its accuracy (the error does not exceed 10 percent) is superior to that of other models presented in the literature.

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References