A GaAs SOI HEMT Fabricated by Fluidic Self-Assembly and Its Application to an RF-Switch

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SUMMARY The heterogeneous integration of GaAs HEMTs on a polyimide-covered AlN ceramic substrate was demonstrated using a fluidic self-assembly (FSA) technique. We used thin device blocks for the FSA, which have various advantages. In particular, they can reduce the drain-source capacitance \( C_{ds} \) of the assembled HEMTs if the substrate has a low dielectric constant. This is a novel kind of semiconductor-on-insulator (SOI) technology. The dc and RF properties of the GaAs HEMTs on the polyimide/AlN substrate were studied and the reduction of \( C_{ds} \) was confirmed. This technique was successfully applied to the SPDT switch, where a low \( C_{ds} \) is essential for good isolation.

key words: heterogeneous integration, fluidic self-assembly, HEMT, SPDT switch, SOI

1. Introduction

Recently, heterogeneous integration (HI) technology has been attracting much attention. It enables us to integrate devices made of various materials on various substrates. One of the most promising techniques of HI is fluidic self-assembly (FSA) [1], [2]. FSA is an innovative process enabling us to arrange small device blocks, the sizes of which are a few tens of micrometers, onto substrates regardless of the substrate materials. It employs a stochastic process, where small scattered device blocks are captured in recesses on the host substrate placed in a fluid. For example, we have succeeded in arranging a disk-shaped block into each of one hundred recesses on a Si substrate [3]. Virtually any type of device and substrate can be used in this integration process.

In this paper, we discuss the FSA of GaAs high electron mobility transistors (HEMTs) on polyimide-covered AlN ceramic substrates. This process is a type of semiconductor-on-insulator (SOI) technology and it can reduce the capacitances of HEMTs, particularly the drain-source capacitance, \( C_{ds} \). A single-pole-double-throw (SPDT) switch is also demonstrated using this technique, since the reduction of \( C_{ds} \) is important for microwave switching applications.

The paper is organized as follows. In Sect. 2 we introduce the FSA technique. In Sect. 3, we discuss our FSA technique, which uses thin asymmetric device blocks. The results of FSA using AlGaAs/GaAs HEMT blocks on AlN ceramic substrates are also discussed in this section. In the Sect. 4 we describe the fabrication and the properties of HEMTs on a polyimide-covered AlN ceramic substrate, and also their application to SPDT switches. Finally, we summarize this paper in Sect. 5.

2. Fluidic Self-Assembly

Figure 1 schematically depicts the FSA technique. The host substrate is placed on a tilted sample holder in a fluid. The device blocks are made of the guest material. The blocks scattered onto the Si substrate slide over the substrate and fall into the recesses. This is a stochastic process, and the blocks not captured by the recesses are collected and scattered again until all of the recesses are filled with blocks.

FSA has various advantages compared with heterogeneous epitaxial growth and wafer bonding. First, the lattice mismatch and the difference in the thermal expansion coefficients between the substrate and device materials have little effect on FSA. Second, large host wafers, for example, 10-inch Si, can be used for this technique even if we can only use smaller guest wafers (e.g., III-V materials). This is in contrast to wafer bonding. Third, the FSA process is very cost-effective due to the excellent efficiency of material use. This is because the device blocks can be fabricated densely over the entire wafer. These advantages make the FSA method promising for realizing various heterogeneous integrated circuits. Furthermore, this method is applicable to non-crystalline substrates, such as glass and plastic films. Thus, it should be possible to fabricate integrated circuits using the most suitable devices made of the optimum materials on the most suitable substrates.
Figure 2 shows a schematic view of the equipment used in our experiments. As described above, in the fluid the blocks scattered onto the host substrate slide over the substrate and fall into the recesses. Blocks not captured by the recesses accumulate at the bottom of the vessel. These blocks are repeatedly collected and scattered onto the host substrate. In our experiments, this recycling process was carried out manually using a pipet. We observed and recorded experiments using a microscope placed over the vessel. A sonic vibrator was set under the substrate holder to help the blocks slide on the substrate smoothly.

3. FSA Using Asymmetric Thin Device Blocks

In this section, we will describe a novel FSA technique using thin asymmetric device blocks and its application to AlGaAs/GaAs HEMT blocks.

3.1 Using Thin Device Blocks

The blocks should be arranged with a proper orientation and proper face. Originally, the use of thick device blocks having a special shape was proposed to ensure a proper arrangement [2]. It has been reported that thick blocks (larger than 10 μm) having a trapezoidal shape can be successfully arranged in recesses having a complementary shape. However, thin device blocks have various advantages, such as, a short growth time and a simple fabrication process [4]. Moreover such thin device blocks reduce excess capacitances if they are arranged on low-dielectric-constant materials.

We proposed a very simple method for use with thin device blocks. To ensure a face-up arrangement we used blocks having no inversion symmetry as shown in Fig. 3. The figure shows a HEMT block consisting of an AlGaAs/GaAs system, as described in the next subsection. The thickness of the blocks was approximately 2 μm. The blocks have no inversion symmetry but 180° rotational symmetry. Therefore, they can be assembled in the recesses in a device-side-up configuration with two equivalent in-plane orientations. Figure 4 shows an example of the results of assembly on an AlN ceramic substrate using these device blocks. We also added guide structures for efficient assembly. The recess and guide structures were fabricated from polyimide. All the recesses in the 6 × 6 grid were successfully filled with device blocks, demonstrating the effectiveness of using asymmetric device blocks.

3.2 Fabrication Process of the HEMT Blocks

The AlGaAs/GaAs HEMT blocks were fabricated by the epitaxial lift-off technique (ELO). The epitaxial layers were grown by MBE. A GaAs buffer layer was first grown, followed by a 200 nm i-AlAs layer as a sacrificial layer. Then, a thick undoped GaAs buffer layer and AlGaAs/InGaAs/AlGaAs pseudomorphic DH-HEMT layers were grown in succession for the device blocks. The total thickness of the blocks to form was 2 μm. After the growth, HEMTs were fabricated by conventional wet etching and the liftoff process. The gate length and width of the HEMTs were 1.2 and 100 μm (50 μm × 2), respectively. Next, the HEMTs were covered with photoresist and patterned to define the block area. The photoresist was then baked at 200°C for passivation during the ELO process. The sample was etched by the SiCl₄ RIE and a sulfuric-acid-based etchant using the passivation layer as a mask. The etching depth was slightly larger than 2 μm to expose the AlAs sacrificial layer.
Then the sample was dipped into HCl solution to selectively etch the AlAs sacrificial layer. As a result, the device blocks were separated from the substrate. Finally, the blocks were rinsed in D.I. water and stored in methanol, which was also used as a carrier liquid for FSA.

The size of the blocks was $74 \times 128 \, \mu m^2$. This implies that about 1 million device blocks can be fabricated on a 4-inch substrate.

3.3 Properties of HEMTs after FSA

The blocks were then assembled onto the host substrate by FSA, as described in the previous subsection. The host substrate used here is an AlN ceramic, the structure of which is shown in Fig. 5 [4]. First the AlN ceramic substrate was covered by a first polyimide layer. It was then covered by a second polyimide layer, which was patterned to be guide structures. Then an SiO film was deposited by evaporation. The recesses were then patterned on the polyimide/SiO layers by RIE, during which the SiO layer acts as a mask. After FSA, the devices were covered by photoresist and baked at 200°C for planarization. The photoresist has holes for wirings (vias). Finally, Ti/Au was evaporated onto the substrate and patterned to form wires and pads. Figure 6 shows a photomicrograph of the fabricated HEMT on an AlN ceramic substrate.

Figure 7 shows the $I_D - V_D$ characteristics of the fabricated HEMTs before and after FSA. Open circles represent for the device before ELO and closed circles represent the device after FSA. The maximum gate voltage was 0.8 V with 0.2 V steps. The gate length and width were 1.2 and 100 μm, respectively.

HEMTs after FSA. The characteristics of the same HEMT before ELO are also shown in the figure as a reference. No degradation was observed in the $I_D - V_D$ characteristics. The threshold voltage also showed no change after FSA.

We also measured and compared the RF characteristics of the fabricated HEMTs. Figure 8 shows the current gain $|h_{21}|$ and the unilateral gain of the HEMTs after FSA and before ELO. $f_T$ and $f_{max}$ for the device on the AlN ceramic substrate were 7.1 and 11.8 GHz, respectively. These values were almost the same as those for the HEMT on a GaAs substrate, where $f_T$ and $f_{max}$ were 7.2 and 12.5 GHz, respectively.
3.4 Long-Term Stability of the HEMT Blocks Stored in Methanol

The device blocks were stored in methanol. Figure 9 shows the threshold voltage and maximum transconductance of the HEMTs stored in methanol as a function of time. No degradation or threshold voltage shift were found after more than 4 months.

4. Application to an RF Switch

As mentioned previously, thin HEMT blocks can reduce excess capacitances if they are integrated on a material having a low dielectric constant. This is advantageous for various high-frequency applications. In this section, we discuss the integration of HEMT blocks on a polyimide-covered AlN ceramic substrate, and the fabrication of an SPDT switch using such a device. The isolation of the RF switch depends on the excess capacitance, particularly the drain-source capacitance, $C_{ds}$. Therefore, the reduction of $C_{ds}$ by using thin device blocks on a low-k material should be effective for fabricating a high-performance RF switch.

4.1 Fabrication Process of the SOI Devices

The HEMT blocks used in this experiment were the same as those described in the previous section. The structure and fabrication process for the integration on a polyimide-covered AlN ceramic substrate are shown in Fig. 10. First, 3.8-μm polyimide layer was coated on the AlN ceramic substrate using a spin coater, which was followed by the deposition of a 400 nm thick SiO layer by vacuum evaporation. These layers act as a low-k material for the SOI structure. Next, 3-μm-thick polyimide and 400-nm thick SiO layers were again deposited on the substrate. Recesses were formed in these layers by RIE. The upper SiO layer acts as an etch mask, and the lower SiO layer acts as an etch stopper during the recess formation in the polyimide layer. After the FSA of HEMT blocks, the substrate was covered with photoresist and patterned to form vias. Then it was baked at 200°C at 60 min. The circuit was completed by e-beam deposition and the liftoff of Ti/Au to form the wires and pads.

4.2 Device Properties

Figure 11 shows the $I_D - V_D$ characteristics of the fabricated SOI HEMT. Good FET characteristics were obtained. The slightly negative conductance observed at a high gate voltage and high drain voltage might be due to the poor thermal conductivity of the polyimide layer. This should be improved if a metal thermal path is embedded under the block to connect the device block and the AlN ceramic substrate. Further studies on the structure and fabrication process of the SOI HEMT are required.

Next, we investigated the off-state capacitances of the HEMT from the S-parameters. For simplicity, capacitances were estimated from the following approximations.
Table 1 Off-state capacitances of the fabricated HEMTs. (The gate length and width are 1.2 and 100 μm, respectively.)

<table>
<thead>
<tr>
<th></th>
<th>GaAs</th>
<th>Polyimide/AlN</th>
</tr>
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<tbody>
<tr>
<td>( C_{gd} ) (fF)</td>
<td>20.1</td>
<td>15.4</td>
</tr>
<tr>
<td>( C_{gd} ) (fF)</td>
<td>28.1</td>
<td>25.5</td>
</tr>
<tr>
<td>( C_{gs} ) (fF)</td>
<td>38.1</td>
<td>34.8</td>
</tr>
</tbody>
</table>

Fig. 12 Circuit configuration of the fabricated SPDT switch.

\[
\begin{align*}
\mathcal{Y}_{12} & \approx \omega C_{gd} \\
\mathcal{Y}_{22} & \approx \omega (C_{gd} + C_{ds} + C_{dss})
\end{align*}
\]

Here \( C_{gd} \) and \( C_{ds} \) are the gate-to-drain capacitance and the pad capacitance, respectively. The gate voltage was set to \(-2\) V with \( V_{ds} = 0 \) V to investigate their effects on the isolation characteristics. The results are summarized in Table 1. The capacitances were lower on the polyimide/AlN substrate. In particular, \( C_{ds} \) showed the largest decrease of about 25%. This is a significant result demonstrating the effectiveness of the polyimide/AlN substrate.

4.3 SPDT Switch

We fabricated an SPDT switch on a polyimide/AlN ceramic substrate. Figures 12 and 13 show the circuit configuration and a microphotograph of the fabricated circuit, respectively. The resistors were fabricated by the e-beam deposition of a thin layer of NiCr.

First, the proper operation of the switch was confirmed using a dc input signal, as shown in Fig. 14. The input was connected to a dc voltage source of 1 V. The control voltages were 0.6 and \(-2\) V for the ON and OFF states, respectively. The control signal successfully switched the input dc voltage, as shown in the figure. Then, the circuit was tested using a network analyzer. The results are shown in Fig. 15. The insertion loss and isolation were \(-3.3\) and \(-17.4\) dB at 20 GHz, respectively. These values can be improved by using more sophisticated circuit design and HEMTs with a shorter gate length. The values were in good agreement with the result of the circuit simulation using device capacitances shown in the Table 1. This indicates that the leakage power was about 30% lower than that on GaAs substrates.

5. Conclusion

A novel GaAs SOI technology was proposed using the FSA. Thin GaAs HEMT blocks, the size of which was \(74 \times 128 \mu m^2\), were successfully assembled on a polyimide-covered AlN ceramic substrate. To assemble the blocks with device-side-up configuration, we introduced novel device blocks having no inversion symmetry. It has been demonstrated that \( C_{ds} \) can be reduced using this technology. This technique was successfully applied to an SPDT switch.
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References


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