Considering MEEF in Inverse Lithography Technology (ILT) and Source Mask Optimization (SMO)

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ABSTRACT

Mask Error Enhancement Factor (MEEF) plays an increasingly important role in the DFM and RET flow required to continue shrinking designs in the low-k1 lithography regime. The ability to model and minimize MEEF during lithography optimization and RET application is essential to obtain a usable process window (PW). In Inverse Lithography Technology (ILT), MEEF can be included in the cost function as a nonlinear factor, so that the inversion minimizes MEEF, in addition to optimizing PW and edge placement error (EPE). ILT has been shown to optimize masks for a given source. Using ILT for contemporaneous Source and Mask co-Optimization (SMO) can provide further benefit by balancing the complexity of mask and source. Results demonstrating the benefits of “MEEF-aware” ILT and SMO for advanced technology nodes are presented in this paper.

Keywords: MEEF, Inverse Lithography Technology, ILT, Source Mask Optimization, SMO, RET, SRAF

1. INTRODUCTION

As lithography moves deeper into the regime of low k1-factor, co-optimization of layout, mask, and lithography is critical to deliver a production-worthy patterning solution. The goal of co-optimization is to create a design, along with its corresponding solution of resolution enhancement technologies (RET), that is less sensitive to manufacturing process variations. The most important evaluation metric of the performance of a given RET solution is to characterize its performance across a specified depth of focus (DOF) and exposure latitude (EL); this is commonly referred to as process window (PW). PW calculation has been traditionally evaluated without considering mask errors.

At low k1 lithography resolution approaches the imaging limit, image contrast is poor, and the mask error enhancement factor (MEEF) is growing closer to intolerable limits. It becomes increasingly important to consider MEEF and mask error in the total budget of process variations, so we must consider how layouts, illumination, and mask patterns affect MEEF.

For years, source optimization and mask pattern correction have been conducted as two separate RET steps. In the last decade or so, the mask pattern correction changed from rule-based OPC to model based OPC, from sparse OPC to dense (pixel) OPC. Recently, Inverse Lithography Technology (ILT)[1] has been applied more broadly as the next generation of mask correction technology [2-8]. As for source optimization, the conventional disk-shaped illumination source has been gradually replaced by off-axis illuminators, such as annular, C-Quad, and QUASAR™, in order to gain image contrast and PW. However, using the conventional approach, the source was optimized based on fixed mask patterns; in other words, OPC and SRAFs were not considered in source optimization. This solution results in a source optimized only for dense patterns, but which may not work well through pitch because of the tight coupling between illuminator design and SRAF placement. This is important because defocus behavior of sparser patterns often limits process window.

Using SMO with ILT, an ILT-optimized mask is generated for each designated illumination condition in order to find the best combination of source and mask. This approach has been applied to explore and select lithography processes and design rules for advanced semiconductor technology nodes [9, 10]. In this paper, new algorithms with more intelligence are introduced into source mask optimization with ILT to generate better solutions.
The extensive use of RET in low $k_1$ lithography increases the complexity of two dimensional (2D) simulations. Characterization of MEEF using the traditional cutline CD approach is insufficient to assure the identification of all lithographically marginal areas in a complex 2D design. In this paper, a new method of edge-based MEEF, full field pixel-based MEEF, is presented. “MEEF-aware” PW and Process Variation (PV) bands are introduced. Use of MEEF and PV band in Inverse Lithography Technology (ILT) and SMO are discussed, and real case studies obtained from leading semiconductor manufacturing companies are presented.

2. MEEF EXPLORATION

2.1 Edge-based MEEF

MEEF is defined as the wafer CD variation as a function of the mask CD variation to wafer level (1X), in which MEEF can be expressed mathematically [11, 12]:

$$MEEF = \frac{\partial CD_{\text{wafer}}}{\partial CD_{\text{mask}}}$$

Although we define MEEF with respect to a global mask bias, points along perimeters of image patterns move by different amounts. A CD measurement is the difference between two edge positions, which may move by different amounts under the influence of mask bias, complicating the interpretation of MEEF. Furthermore, we are often interested only in the position of a single edge, such as when characterizing line-end pull-back. In order to capture the sensitivity of each edge to mask error, an edge-based MEEF calculation is proposed. It can be written as

$$MEEF_{\text{edge}} = \frac{\partial EPE_{\text{wafer}}}{\partial EPE_{\text{mask}}}_{\text{normal}}$$

where EPE is used instead of CD. $\partial EPE_{\text{mask}}$ is the mask perturbation per edge, equal to $\frac{1}{2} \partial CD_{\text{mask}}$ in the traditional definition, i.e. the mask is evenly biased. $\partial EPE_{\text{wafer}}$ is measured as the distance between the image contour of a perturbed mask and the image contour of a nominal mask along its normal direction, as illustrated in Figure 1. Therefore, the edge-based MEEF can be extracted from the ratio of perturbation from wafer to mask. Along the edge of nominal, two edge-based MEEF numbers can be calculated for positively (+) and negatively (-) biased masks, respectively. The two MEEF numbers are usually slightly different from each other due to asymmetric response to bias-up and bias-down. The magnitude of difference in MEEF of ± biased mask depends on local environment and is larger for high MEEF area. Since mask error can be either positive or negative, central difference approximations to the derivative are appropriate.

![Aerial image contours](image_url)

Figure 1. An example of aerial image contours from regular and biased masks. EPE based MEEF is calculated from the delta between positively (+) and negatively (-) biased masks along normal direction of nominal image contour.
2.2 Full Field Pixel-based MEEF Map

Traditionally, MEEF is calculated by measuring CD change across a cut-line. Multiple cut-lines are placed across potentially challenging areas. This method is often sufficient for relatively simple patterns. For a complex two-dimensional pattern, however, due to the strong proximity effect among nearby features and high inter-correlation among illumination conditions, mask, and OPC at low-k1, it becomes more challenging to pre-identify all of the weak points. Because the number of cut-lines is practically limited, the cut-line approach may not measure all critical locations. A full-field rather than a limited cut-line analysis of MEEF is therefore important to assure the capture of all critical information needed for a complex 2-dimensional design.

From the definition of edge-based MEEF given in the previous section, one can derive the MEEF of every segment along an image contour. Due to the variation of MEEF, the image contours must be divided into small segments in order to accurately calculate MEEF everywhere. The native implementation of ILT in pixel-based space makes it ideal to render edge-based MEEF into a full field MEEF bitmap. As shown in Figure 2, a full field color MEEF map generated from Luminizer™ Explorer displays the color-coded MEEF value of each pixel along the aerial image contour. MEEF hotspots are visually apparent on the map. In the previous section, we mentioned asymmetry of MEEF across a pair of edges due to the different proximity environment. It is evident from the MEEF map that at these highly non-uniform locations, two sides of a contour do not display the same colors. Traditional CD cut-line based MEEF will average out the two sides of a contour, underestimating MEEF. This can potentially hide serious design problems.

![Figure 2](http://example.com/figure2.png)

**Figure 2.** (a) Design target clip; (b) Aerial image contours of +/- biased masks; (c) full field edge-based MEEF bitmap showing MEEF distribution and hotspots. Red color represents high MEEF and cool color represents low MEEF value. Each pixel along the contour represents the edge-based MEEF of the edge segment inside the pixel.

The MEEF map is visually useful for identifying hotspots. In addition to the MEEF map, Luminizer™ Explorer also generates MEEF statistics. The tolerance for process variation can be different for different parts of a design. For example, the tolerance for the inner corner of a metal line can be much higher than for line-end. To provide a better assessment of MEEF, automatically categorized MEEF reports are generated for each type of topology, such as line-ends, outer corners, inner corners, etc. Figure 3 shows different types of geometry-based topology markers and reported MEEF statistics for each topology, with maximum and average MEEF values. Aside from automatically generated topology markers, customized user-defined markers can also be added to the design for further customized analysis. Additional MEEF reports can be generated for each type of user-defined topology regions.
2.3 MEEF Aware Process Window and PV Band

Process window is the most important metric in lithography simulations for evaluating the performance of a given RET solution. Achieving a certain minimum depth of focus (DOF) at a given exposure latitude (EL) is the paramount goal. Process window calculation traditionally is based on a perfect mask, assuming no mask errors, no corner rounding, etc. In reality, process variation always leaves residual mask errors which affect process window for on-wafer printing. When MEEF is low, the impact of mask error is small compared to the total budget of process variation. In a low k₁ regime, MEEF increases substantially to the level of 4~6, or even higher. Mask errors are magnified several-fold and have a much more pronounced impact at wafer level. DOF predictions that do not consider MEEF are usually unrealistically optimistic.

To obtain a more realistic view of whole process variations, mask error must be factored into process window calculations. Given mask bias, \( m \), inferred from mask targeting specifications, MEEF aware process window is calculated as the common process window of unbiased and \( \pm m \) biased masks. As shown in Figure 4, when MEEF and a 1nm mask bias were included in the computation, DOF at 5%EL was reduced from \( \sim 220 \)nm (Figure 4(a)) to \( \sim 145 \)nm (Figure 4(c)).

In addition to process window, another useful way to study the predicted quality of printed image is by analyzing PV bands. The band is generated by calculating wafer aerial image at the various process conditions and combining the resulting images into a band. The width of the band represents the range within which a feature will print as the process conditions vary. Typically the conditions used to generate PV bands are %EL and defocus, as shown in Figure 4(b). If MEEF and mask error are also included in the process variation conditions, a much larger band area is generated as seen in Figure 4(d), which suggests a much worse image variation than would result from a perfect-mask assumption. Figure 4(b) and 4(d) represent the best and worst cases from mask variations, respectively. Actual variation would be expected to fall between the two extreme scenarios.

### Topology MEEF Statistics:

<table>
<thead>
<tr>
<th>Topology</th>
<th>Maximum</th>
<th>Average</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line end</td>
<td>6.80</td>
<td>3.59</td>
</tr>
<tr>
<td>Smooth</td>
<td>4.82</td>
<td>2.38</td>
</tr>
<tr>
<td>Outer corner</td>
<td>5.71</td>
<td>3.39</td>
</tr>
<tr>
<td>Inner corner</td>
<td>4.22</td>
<td>2.88</td>
</tr>
<tr>
<td>Others</td>
<td>6.79</td>
<td>2.75</td>
</tr>
</tbody>
</table>

### Overall MEEF Statistics:

- Maximum MEEF : 6.80
- Average MEEF : 2.66
- Standard deviation : 0.71

Figure 3. Automatically generated geometry based topology markers overlay with MEEF map. MEEF statistics of each topology type as well as overall combined of all topology types are generated for detailed analysis.
3. USE MEEF IN INVERSE LITHOGRAPHY TECHNOLOGY (ILT)

3.1 Basic Workflow of ILT using Level Set Methods

Luminescent’s approach to ILT is based on a branch of mathematics co-invented by Stan Osher at UCLA. Commonly known as Level-Set Methods [13], these techniques have been applied to solve inverse problems in a wide range of engineering disciplines such as image processing and fluid dynamics. In our formulation, the design intent target and simulated wafer contour are represented in 2D pixilated arrays (2D gray scale image). The post-correction mask is represented as 2D level-set function, and mask transmission as 2D, potentially complex, array (Figure 5). The above formulation of the problem has a variety of advantageous properties. For example, the level-set representation allows for contours to merge, break, appear, or disappear, in a consistent, mathematical representation. Various functions (for example, the wafer image) can be determined as closed form expressions. The mask function itself is an element of a Hilbert-space which is much larger than the two-dimensional space of the photomask, which allows for “more global” solutions to be found [14].

A lithography forward model, which simulates the mask effects, scanner optics, resist development, and even etching and SEM bias, are created and used in ILT. Such forward model is similar to models used in OPC and lithography simulators. Therefore, once a mask pattern is given, a forward simulation can be run to compute the aerial and latent image, and from the latent image to printed resist image, and even etched image.
A cost function (also called a merit function, energy function, or Hamiltonian) can be defined which provides a measure of the quality of the solution, or the “goodness” of the mask. In a simple case, the cost function could be the absolute value of the difference between the wafer image and the target pattern, integrated over the area of the mask. In practice, a number of additional elements may be included in the cost function. For example, the wafer pattern at various conditions throughout the process window (i.e., over or under exposed and/or plus/minus focus), the Normalized Image Log Slope (NILS) of the image, the robustness against MEEF, or other factors as deemed appropriate. The actual functional form may be different from the form as described above as well. Elements that are not directly related to lithography may be included; for example, simple masks may be preferred over complex masks, and terms to this effect may be included in the cost function as well. What is essential is that the cost function is a functional of the mask function, and minimizing cost function allows us to find the optimal mask, according to the criteria we have chosen.

Represent mask pattern, wafer contours and target in level set allows us to compute the gradient of the cost function with respect to the mask patterns, and this enables us to use modern minimization algorithms to solve the lithography inverse problem in a fast and efficient way in order to be used in full chip correction.

Another important aspect of the minimization problem comes in the form of constraints. A variety of constraints are imposed by the realities of mask manufacturing; for example, two disjoint chrome regions must be separated by a minimum distance, and a chrome line must have a minimum width. We address these constraints by defining a sub-space of the full Hilbert space of mask functions, and restricting our solution to this sub-space.

A key distinctive feature of ILT is the absence of pattern-dependent heuristics, and the ability to broadly explore wide areas of solution space. This lead to an very important features in RET - Sub-Resolution Assist Features (SRAFs), which are mask features that do not print on the wafer which are detached from the edges of the main mask patterns, and yet manipulate the light reaching the wafer so as to accentuate the wafer image. In the past, these were placed empirically, with great care, and frozen in place during the computation of the rest of the mask. In contrast, ILT can determine optimal SRAFs simultaneously with the rest of the mask. Level Set Methods naturally support SRAFs in the inversion calculation. The Level Set surface evolves during the inversion calculation, which allows the SRAFs to generate, change dimensions, and even vanish. For example, when the mask pattern level set surface crosses the “0” level set, which defines the mask contour, SRAFs appears; when the surface is changing, SRAFs change shape and size; and when the surface does not cross “0” level set, SRAFs disappear. In ILT, SRAFs are treated the same as main features, so SRAFs and main features are co-optimized during inversion. In addition, SRAFs are consistent with the gradient flow used for the inversion calculation, so the SRAF signal can be naturally carried by the gradient of the cost function.

Figure 5. The level-set representation of mask problem and the flow of using Level Set Methods to solve the lithography inverse problem.
function. The absence of segmentation scripts is another significant advantage because it usually requires significant engineering resources to write such scripts for different patterns on different design layers[15-20].

3.2 Adding MEEF in ILT Cost Function

ILT can use multiple simulated wafer images at different process conditions in the cost function ($E$). Traditionally those different process conditions are defocus and off-nominal exposure conditions as depicted in (Figure 6(a)) and expressed in the following

$$E = \sum_{x,y} \sum_{E,D} \sum_{n} w(E_i,D_i) \sum_{m} w_{topo} (f(mask) - target)$$

One way to consider MEEF in the cost function of ILT can be implemented by adding image contours simulated with biased masks (e.g., +1nm and -1nm) into the multiple image planes (Figure 6(b)). The new cost function becomes

$$E = \sum_{x,y} \sum_{E,D,M} \sum_{n} w(E_i,D_i,M_i) \sum_{m} w_{topo} (f(mask) - target)$$

3.3 Case Study of Use MEEF in ILT

The following example shows the impact of use MEEF in ILT. In this study, design clips from an advanced memory technology 4Xnm node were used. Maximum MEEF and DOF values for all topologies and line-end only are shown in the charts (Figure 7). Results of running ILT with and without MEEF in cost function are compared for various source conditions, such as C-Quad, QUSAR™ and dipole. By looking at the overall distribution of the MEEF and DOF, one can notice that the maximum MEEF in ILT solution and MEEF for line-ends were reduced about 25% with implementation of MEEF term in cost function, while the common DOF was reduced ~10% with corresponding MEEF reduction. Therefore, finding the right balance between MEEF and DOF is important in any litho optimization for advanced technology nodes. In addition, it is feasible to find certain source conditions under which the MEEF is reduced and DOF is improved (looking at individual dots in the chart).
4. USE MEEF IN SMO

4.1 SMO and How to Include MEEF in SMO

If ILT is used only for mask optimization, the improvement may be limited by the source, because some sources (e.g., disk) do not benefit from SRAFs, while other sources (e.g., QUASAR™) require more complicated SRAFs than others (e.g., annular). In such cases, SMO is required to maximize the improvement of ILT and to bring the right balance between mask and source complexity.

In the Luminescent implementation of SMO, the Level Set Method is used in source optimization – instead of representing the mask patterns with level set function, the source map is represented by level set function. During the minimization process, the level set function evolves to achieve a minimized cost function (e.g., the difference between aerial image and ideal image) via a gradient flow, and the gradient flow is based on the cost function itself. This flow is combined with the mask inversion flow so that a simultaneous mask & source co-optimization is achieved. In such flow, MEEF can be integrated into the cost function of SMO as a nonlinear term in addition to DOF.

4.2 SMO Case Study for Advanced 4Xnm Memory – SMO can balance complexity between source and mask

Figure 8 shows an example of SMO for an advanced memory device. The target pattern is a 4Xnm contact array with different pitches in X and Y directions. Three combinations of source and mask are shown in this example. In the first scenario, the illumination is a fairly simple QUASAR™, but the mask pattern is quite complicated, especially the SRAF patterns. A reasonable process window (DOF 141nm @6% EL) was achieved. In the second scenario, the mask pattern, including rectangular SRAFs is fairly simple; however, the source map is very complicated. The process window is similar to that in scenario one. In the third scenario, both mask pattern and source map are fairly simple. The higher complexity on mask increases mask write time and difficulty of mask inspection. This case study demonstrates that one can push the complexity from mask to source in order to reduce OPC and mask making cost, which is in practically useful for memory arrays.
4.3 SMO Case Study for Advanced 4X Memory – SMO can further improve process window and MEEF than ILT alone

The following is another SMO case study for an advanced 4X memory device. In this case, ILT and SMO were compared with customer’s POR source and mask. As shown in Figure 9, when the POR source was kept and ILT was applied, DOF is increased about 30%, while MEEF is reduced from 7.3 to 5.1. When a free-form SMO was applied, DOF and MEEF were further improved. Free-form source obtained from SMO generally gives the best performance; however, it may be difficult to manufacture such a complicated DOE. In such case, a DOE constrained source optimization may become a more realistic solution. In this example, a parametric source, a rotated QUSAR™ plus disk illumination, is also shown as a solution, and is clearly a better solution than the POR in terms of both DOF and MEEF.
Figure 9 shows a case study of SMO for an advanced memory device. The target pattern is a customer’s 4Xnm contact design.

4.4 SMO Case Study for Advanced 22nm Logic – A typical SMO Workflow and Impact of Use MEEF in SMO

SMO for a logic device is usually more complicated than for a memory device, because in most cases the target of memory SMO is the memory array, but for logic, SMO must consider many variations of patterns, including 1D through pitch patterns, SRAMs, and some random logic clips. Also, because so many different patterns must be considered for logic SMO, the optimized source of logic SMO tends to be more regular than the source of memory SMO. This suggests that logic SMO is not as important and useful as memory SMO, because in most cases, logic SMO will end up with annular illumination. Such understanding has to change at the 32nm technology node and beyond, due to the fact that lithography is becoming so challenging. Off-axis illumination has to be used to improve imaging, and design rules have to change to compensate for the restrictions of lithography rules.

Before doing SMO for a combination of various patterns, SMO for each individual pattern is first presented. Figure 10 shows the design target of three 1D patterns at critical design rule pitches. The most dense line/space pattern has only one direction in order to obtain a better lithography performance. The other looser pitch patterns have both x and y components. For such simple dense 1D patterns, there are theoretical answers to the best source from partially coherent 2 beam imaging or 3 beam imaging theory. As shown in Figure 10, the SMO algorithm obtained answers consistent with the theoretical results.
The next step is to review the SMO result for random logic clips. Typically, random logic clips are complicated 2D patterns that include not only dense, but also semi-dense and isolated patterns. In such a case, there is no simple theoretical answer. In addition, source optimization only will not provide the right answer, because mask bias (i.e., OPC) and SRAFs are needed for the semi-dense and isolated patterns to maximize the common process window. ILT, due to its integrated approach to optimize main patterns and SRAFs without any pre-defined rules (except mask rules), becomes the best choice for SMO by combining it with source optimization algorithms. Figure 11 shows the SMO result for a random logic clip. In this case, the smooth region (as marked on the design clip) was used in the cost function. A free-form source and an inverse mask satisfying customer mask rules (minimum CD and space: 20nm, minimum corner to corner: 15nm, minimum segment length: 10nm) were obtained.

The examples above show the SMO results for individual clips. For 22nm logic SMO, variations of critical patterns have to be included. In the following, a typical SMO workflow is explained (Figure 12). First, various patterns, including 1D through pitch patterns at critical design rule CDs and pitches, some SRAM patterns, and samples of random logic clips are used to calculate free-source SMO. This free-form source for multiple design clips is noticeably different from any of the free-form sources for each individual pattern. The free-form source gives the best lithography
performance, but it may be difficult to manufacture the necessary diffractive optical elements (DOEs). Therefore, one could use a free-form source as a guideline, and approximate it with a parametric source. In this case, a Disar plus QUSAR™ resembles the approximate shape of the free-form source. Now a DOE constrained composite source SMO is performed to find the right values for those variables in the composite source, such as open angle, sigma in and sigma out, to give the best lithography performance. After the composite source SMO, a regular source satisfying DOE constraints are obtained.

Figure 11. SMO workflow for 22nm logic

Once the SMO flow is established, one can study the impact of MEEF in SMO. Figure 12 shows the SMO results with and without consideration of MEEF. The PV band was used in this study as the parameter to optimize in SMO. Since process margin requirements on focus, dose latitude and mask bias can all be specified, PV band is a good way to understand, visualize, and quantify the process margin. It is also less computationally expensive than calculating DOF, exposure latitude and MEEF; therefore, it is now commonly used in SMO calculations. From Figure 12, one can clearly see, after including the MEEF, that the PV band is significantly reduced.

Figure 12. Comparing SMO results for 22nm logic with and without considering MEEF

Figure 13 shows the summary of the final results of SMO compared with customer source and mask for a 22nm logic pattern. Again, the PV band is used as the indicator for SMO result. It is clear that Luminescent’s SMO source and mask outperform the customer’s source and mask across the board. For reference, SMO results based on other DOE
constrained sources, such as annular, C-Quad, Disar, Disar plus annular, are also shown in this chart. It can be seen that the SMO source also outperforms those sources in addition to the customer’s source.

Figure 12. Summary of SMO results for 22nm logic

5. SUMMARY AND CONCLUSIONS

MEEF is an important factor that cannot be ignored in low k1 lithography. It must be included in mask pattern correction and source-mask optimizations. An edge-based MEEF calculation is proposed to address the need for more detailed analysis of MEEF in a complex 2D environment in a low k1 regime. A full-field MEEF color bitmap using edge-based MEEF definition is presented to provide easy visual identification of hotspots. The automated placement of topology markers to cover all pattern feature types ensures that all marginal lithographic spots will be identified. A categorized MEEF report associated with each topology type allows users to evaluate MEEF at different proximity environment.

Traditional process window evaluation without considering MEEF and mask error can undermine resolution enhancements due to the increased impact from mask errors in low-k1 lithography. A third dimension (MEEF) in process window assessment is introduced to provide a more realistic litho simulation in the DFM flow. The method of creating a MEEF-aware PV band, including mask bias, is presented to show wafer image variability under all process variations from dose, defocus and mask error. It provides a more realistic view of image quality against process variations, and also becomes a computationally efficient way to optimize process window including MEEF in SMO.

DOF and MEEF are often competing factors in a RET solution, but are not totally coupled. For a given illumination condition, a trade-off between MEEF and DOF can be made with different variations of mask pattern. It is also feasible to find an optimized solution that not only improves the DOF, but also reduces the MEEF.

MEEF and DOF should be considered simultaneously in mask correction and SMO. Use of MEEF in ILT and SMO generates optimized results for low K1 lithography. ILT, an integrated solution for OPC and model-based SRAF, provides a superior SMO solution when combined with source optimization. Solutions presented here demonstrate how ILT can provide effective SMO for 4x nm process nodes, which require consideration of high MEEF values.
REFERENCES