Hybrid CMOS/Magnetic Process Design Kit and application to the design of high-performances non-volatile logic circuits

Invited Paper

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Abstract—Spintronics (or spin-electronics) is a continuously expending area of research and development at the merge between magnetism and electronics. It aims at taking advantage of the quantum characteristic of the electrons, i.e. its spin, to create new functionalities and new devices. Spintronic devices comprise magnetic layers which serve as spin polarizers or analyzers separated by non-magnetic layers through which the spin-polarized electrons are transmitted. Typically, they rely on the Magneto Resistive (MR) effects, which consists in a dependence of the electrical resistance upon the magnetic configuration. These devices can be used to conceive innovative non-volatile memories, high-performances logic circuits, RF oscillators or field/current sensors. This paper describes a full Magnetic Process Design Kit (MPDK) allowing to efficiently design such CMOS/magnetic hybrid circuits. The latter can help circumventing some of the limits of CMOS-only microelectronics.

I. INTRODUCTION

Magnetic Tunnel Junctions (MTJs) are well known as the basic elements of Magnetic Random Access Memories (MRAM) ([1]), a new kind of non-volatile memory which combines high writing/reading speed, low-power consumption, density, hardness to radiations and endurance. Due to this unique set of performances, MTJs can also be used in logic circuits. Although their intrinsic non-volatility naturally encourage to use them in memories, they can also be used to intrinsically mix memory and logic parts of the circuits to push forward the limits of CMOS microelectronics and allow new functionalities. To evaluate the performances of such hybrid circuits, it is necessary to be able to integrate these new devices in classical design suites. At transistor level, the design of a logic circuit requires a model of the electrical behavior of the components and a set of tools to draw and check the layout of the circuit before manufacturing. At higher level, standard cells are required to allow automatic design of a circuit from a Hardware Description Language (HDL) description. In the first part of this article, we will present the hybrid Magnetic CMOS/Technology. Then, we will describe how mixing CMOS and magnetic devices can result in innovative and high-performances non-volatile logic circuits. At the end, we will present a full Process Design Kit for the CMOS/magnetic technology to design such circuits.

II. DEVICE AND TECHNOLOGY

A. Magnetic Tunnel Junctions

MTJs (Fig.1) are nanostructures composed of two Ferromagnetic (FM) layers separated by an insulating layer. The magnetization of one layer, called Reference Layer (RL) is pinned in a fixed direction and acts as a reference, while the magnetization of the second one, called Storage Layer (SL) can typically be switched between two stable directions, Parallel (P) or AntiParallel (AP) to the magnetization of the RL. According to the relative orientations of the magnetizations of the SL and the RL, the electric resistance of the MTJ changes, with an hysteretic behavior: the resistance in the AP state is larger than in the P state. Today, most MRAM technologies are based on 1 MTJ-1 transistor cell arrays (1 MTJ to store information and 1 selection transistor, ([2],[3])). To read the stored data, a current flows through the MTJ and is typically compared to a reference current to determine the resistance of the MTJ and thereby the logical stored data. Writing the MTJ can be performed in different manners, using either an external magnetic field or a spin-polarized current.

The first writing technique, called FIMS for Field Induced Magnetic Switching, consists in using external magnetic fields to control the magnetization of the SL. Two perpendicular lines are used to generate the write field: the word and bit lines (Fig.2(a)). Only the MTJ at the crossing of the two lines can be written. This approach suffers from selectivity problems because, due to process variations, the field generated by a single line can sometimes write a MTJ (half selected instability). In order to circumvent the selectivity problems in this writing scheme, another approach was proposed by...
Motorola in 2003 ([4]). It is called toggle MRAM and relies on the use of a so-called Synthetic Anti-Ferromagnetic (SAF) layer. This toggle scheme strongly reduces half selected instability and therefore improves the FIMS write margin. This writing scheme was used by Motorola, then Freescale and now Everspin for all their product families, from 256Kb to 16Mb for a large panel of applications. Although toggle MRAM contributed to make MRAM competitive for a lot of applications, the principle of magnetic field writing remains globally not scalable: reducing the volume of the storage layer results in a decrease in its thermal stability. The only solution to counteract this is to increase the anisotropy. But in this case, the switching field increases and correlatively the write current: reducing the size of the devices does not reduce the write energy and the scalability is limited by electromigration issues in the word and bit lines.

The Thermally Assisted Switching (TAS) approach was proposed to circumvent the limitations of the FIMS approach and relies on the strong dependency of the magnetic properties upon temperature ([5]): a pulse of current is first applied throughout the MTJ to heat it above a so-called “blocking” temperature (Fig.2(b)). It can then be easily switched by a low-magnetic field. Subsequently, the heating current is switched off so that the MTJ cools down to ambient temperature. This heating and cooling process only takes about 20ns. This technique is more scalable since the heating current is proportional to the surface of the MTJ. It insures an excellent retention of the information in standby for more than 10 years. This technology is being developed by the MRAM manufacturer CROCUS-Technology.

We have seen with the MR effects that the magnetization of FM layers can influence the flow of electrons in a structure and so its resistance. The opposite phenomenon exists: a spin-polarized current can act on the magnetization of a FM layer, by interaction between the spin of the electrons and the magnetization. This phenomenon was first predicted in 1996 ([6]) and experimentally observed a few years later. When the current flows through the RL, the conducting electrons get polarized by the interaction with its magnetization. After flowing through the SL, the electron polarization is reoriented along the SL layer magnetization direction. By action-reaction principle, a part of the polarization of the electrons is transmitted to the SL magnetization, under the form a torque called Spin Transfer Torque (STT). If the current density is strong enough, the contribution of all the electrons is strong enough to switch the magnetization of the SL. This can be used as another way to write MTJs. The STT MRAM cell is greatly simplified in comparison to FIMS MRAM cell since no field lines are required (Fig.2(c)). Each cell only consists of a MTJ connected in series with a selection transistor. The writing is performed using bipolar pulses of current. The reading is performed at lower current to avoid write errors during read. Another interesting property of STT is that it can inject energy and compensate the losses in the system, leading to steady state precessions of the magnetization. The frequency of the precessions is in the GHz range and can be used to conceive RF oscillators ([7]).

B. Hybrid CMOS/Magnetic technology

The hybrid technology presented here has been developed in the framework of French national projects. The magnetic devices are fabricated at CEA-LETI and CROCUS-Technology, in post-process above the STMicroelectronics 130nm CMOS process. Fig.3 shows a cross-section of the technology: it integrates the whole standard CMOS process, the magnetic layers with the MTJ itself, top and bottom electrodes plus vias to connect the MTJ to the CMOS layers. An interesting feature of this post process is its full compatibility with any standard CMOS process.

III. HYBRID CMOS/MAGNETIC LOGIC CIRCUITS

A. Embedded memory

Logic systems are typically composed of a pure computational part and a memory part in which the input and output data of the calculation are stored. Complex systems have a memory hierarchy, comprising different memory types: the closer the memory is to the computational part, the faster it is. When going away from the computational part, the speed is less critical and the density becomes more critical. Due to their unique set of properties which combines speed, low-power consumption, integration density and non-volatility, MRAM
could replace parts of the memory hierarchy. As a result, the architecture of processors could be redesigned to take advantage of MTJs to improve performances, in particular in terms of power consumption and related heating issues.

B. Non-volatile SRAM

The operating frequency of Flip-Flops or low-level cache is larger than 1GHz. Classical MRAM cannot reach such speeds. However, beside classical 1T-1MTJ structure, non-volatile SRAM was proposed, called Black and Das cell ([8], Fig. 4). This structure looks like a classical SRAM latch, with an additional pair of MTJs, a set of transistors to write the MTJs (for example transistors to produce the heating current in TAS technology) and an AutoZero (AZ) transistor. Two logic values are stored in this latch: an information in the latch itself (Q and Q\text{bar}), which is the information available and an information stored in a differential way in the MTJs (one MTJ is Parallel while the other is AntiParallel). While the AZ transistor is open, the MTJs have no influence and the cell works as a standard SRAM, with the same speed. When the AZ transistor is closed, the latch is shortened, and the difference of resistance in the magnetic branch unbalances it. When the AZ signal is removed, the latch switches to a state corresponding to the value stored in the MTJs. In the AZ operation, the latch operates as a sense amplifier to read the MTJs state. This cell can be used for example to backup the active data in the magnetic part and to restore it at any time within a few hundreds of picoseconds. Combined with a classical SRAM latch, this cell can be used to create a Non-Volatile Flip-Flop (NVFF, [9], [10]).

C. Field Programmable Gate Array

Field Programmable Gate Arrays (FPGA) are essentially composed of memory. They are currently based on SRAM and/or Flash memory. SRAM-based FPGA are fast to program, but less dense and require an additional non-volatile memory (typically Flash) to permanently store information when powered off. Fully Flash-based FPGA are denser, but the writing time and energy consumption prevents them from being used for reconfigurable computing for example. MRAM-based FPGA could combine the advantages of the two approaches to obtain a really fast non-volatile FPGA. In such a FPGA, a shift register based on the non-volatile SRAM Flip-Flop presented previously could be used for example to load the configuration once in serial, then to back it up in the magnetic part, so that it can be loaded in less than 1ns at startup (or reloaded at any time) in case of failure ([10]). The use of the non-volatility also allows new functionalities. Shadowed reconfiguration consists in changing the functionality of a circuit without affecting its ongoing operation. This is eased by the use of non-volatile SRAM cells since writing the magnetic configuration does not affect the value stored in the latch. In addition, by using several pairs of MTJs instead of one and a tree of selection transistors several configurations could be chosen (multicontext, [10]).

D. Low-power non-volatile logic circuits

In advanced CMOS technologies, the drastic reduction in the size of devices results in a strong increase of the power consumption, especially of the standby power consumption due to leakage. This also results in heating and reliability issues. Several techniques are being used to limit the power consumption at the technology level (SOI, HiK gates [11]), at the design level (using Multi or Variable Threshold MOS transistors [12]) or at the system level (clock gating, power gating, Dynamic Voltage and Frequency Scaling). Power gating consists in cutting off the power supply of unused blocks to avoid leakage and thereby limit the standby power consumption. To avoid loosing the active data, it is possible to store them in distant very low-leakage or non-volatile register (resulting in delays an dynamic power consumption). It is also possible to only reduce the supply voltage in the retention phase (but in this case a small leakage remains). Using non-
how design techniques can be adapted to lead to innovative add non-volatile memory functionality to logic circuits and illustrates the potential advantages offered by using MTJs to was proposed in [15]. This circuit is a simple example which power consumption. An example of non-volatile full adder speed, simplifying interconnections and reducing dynamic between logic and memory, reducing footprint, improving divinity (i.e. a logic function in CMOS technology right on the Si substrate and a memory capability built above the logic function in back-end magnetic technology, the two functions being interconnected by vertical vias (see Fig.5 left). In addition to reduce the standby power consumption, this concept allows multiplying and shortening interconnections between logic and memory, reducing footprint, improving speed, simplifying interconnections and reducing dynamic power consumption. An example of non-volatile full adder was proposed in [15]. This circuit is a simple example which illustrates the potential advantages offered by using MTJs to add non-volatile memory functionality to logic circuits and how design techniques can be adapted to lead to innovative hybrid CMOS/Magnetic architectures.

Fig. 5. Principle of Janus (logic-memory) components. Right: logic-in-memory (multiplying and shortening the interconnections between logic and memory parts of a circuit).

volatile registers allows easing the power gating techniques. Indeed the data can be very quickly stored in the non-volatile parts and the power supply totally switched off. On demand, the data can be immediately reloaded and the circuit restarts with full performance and without additional operations. This has given birth to the concept of normally-off electronics ([13]).

E. Logic-in-Memory

Beyond the use of MTJ as non-volatile memory elements in electronic circuits, the advantages of MRAM technology in terms of low-power consumption, speed, cyclability, hardness to radiations and their ability to be manufactured in back-end magnetic technology above CMOS elements also allow to introduce memorization capabilities in the logic part of the circuit itself (Fig.5). This concept is often referred as logic-in-memory ([14]). In this framework, it is possible to develop Janus components, presenting two faces (as the mythological divinity) i.e. a logic function in CMOS technology right on the Si substrate and a memory capability built above the logic function in back-end magnetic technology, the two functions being interconnected by vertical vias (see Fig.5 left). In addition to reduce the standby power consumption, this concept allows multiplying and shortening interconnections between logic and memory, reducing footprint, improving speed, simplifying interconnections and reducing dynamic power consumption. An example of non-volatile full adder was proposed in [15]. This circuit is a simple example which illustrates the potential advantages offered by using MTJs to add non-volatile memory functionality to logic circuits and how design techniques can be adapted to lead to innovative hybrid CMOS/Magnetic architectures.

IV. HYBRID CMOS/MAGNETIC PROCESS DESIGN KIT

Designing hybrid architectures embedding CMOS and magnetic devices requires integrating the magnetic elements in standard design suites of microelectronics. It is therefore necessary to provide a hybrid Process Design Kit (PDK) within standard design suites to be able to conceive hybrid circuits containing magnetic devices.

A. Spice model of the MTJs

Several SPICE-like models of MTJ were presented in literature. The model developed at SPINTEC ([16], [17]), valid for all MTJ writing schemes (FIMS, TAS, STT), is written in C language, compiled for SPECTRE simulator of Cadence. It takes into account the static and dynamic behavior of the magnetization under external applied field or spin transfer torque, the dependence of the resistance upon the magnetic state, the dynamic evolution of the temperature and the dependence of the magnetic and transports parameters versus temperature. The compiled model is generic and contains the generic equations governing the physical behavior of the MTJ. The parameters corresponding to a given technology are provided via a corner file. Fig.8(a) shows a schematic window in Cadence design suite, which represents a very simple MRAM memory cell composed of a MTJ connected in series with a selection transistor. Fig.8(b) explains the labeling of the nodes; bl0 and b1l represent the top and bottom ends of the MTJ (b1l is connected to the selection transistor). fl0 and fl1 are the ends of a current line eventually required for magnetic field generation. Fig.6 shows simulation results for a Thermally Assisted Switching (TAS) writing scheme. Fig.6(a) and (b) respectively show the heating current through the junction and the resulting increase of temperature of the junction. Fig.6 (c) and (d) respectively represent the current through the current line to generate the write magnetic field and the resistance of the junction. For a heating current large enough to reach the blocking temperature of the storage layer, the voltage exhibits a step like behavior when a magnetic field is applied: this is due to the magnetization switching and the resulting change of resistance. Oscillations can be seen around the magnetization switching due to the peculiar magnetization dynamics during switching which is taken into account in the model. We can also notice that even before and after switching, the voltage is not constant. This is due to the variation of the conductance associated with the temperature variation of the junction. Finally, at magnetic switching, the temperature dynamics changes because the resistance changes and correlative the power dissipated in the MTJ by Joule heating. Fig.7 shows examples of simulation results for STT writing. According to the respective value of current and applied field, we can obtain switching (Fig.7(a)), In-Plane Precessions (Fig.7(b)) or Out-of-Plane Precessions (Fig.7(c)). Results obtained using the present model were compared to previously published theoretical macrospin calculations and are in very good agreement.

B. Layout and physical verification tools

To draw the layout of hybrid circuits, a pCell of the MTJ has been proposed. A pCell (parametrized Cell) is a layout view of a device, whose shape and geometry are automatically adapted to the size specifications of the designer and which respects the design rules of the manufacturer. The pCell can be directly included in a layout, for any size of the device. Fig.8(c) presents the layout of a simple 1MTJ-1T cell, made using the pCell of a MTJ and a pCell of a MOS transistor.
C. Standard cells, digital design tools

A complex digital architecture is generally synthesized automatically from elementary logic functions called standard cells. Several standard cells of Non-Volatile Flip-Flops (NVFF) based on the Black and Das principle have been designed, characterized and included in a standard digital design flow in the framework of a collaboration between CMP and Spintec. In order to be able to run digital simulations for advanced and complex designs, a full Verilog description of the NVFF has been developed. It takes into account the behavior and also the timing checks for the MTJs heating duration, writing and reading. To design non volatile blocks using the innovative flip-flop standard cell described above, the synthesis uses a specific library containing only registers made of CMOS and MTJs. The connections between all the magnetic signals are defined in the HDL description where all these signals need to be declared and interconnected to manage the MTJ writing and reading. As a consequence, the netlist extracted from the synthesis includes the NVFF and both connections of CMOS and magnetic signals. The abstract view of the NVFF is given in order to place and route a full block composed of standard cells, using standard tools. To complete final simulations, an Standard Delay Format (SDF) file including the NVFF internal timings can be extracted from the placed and routed layout to back annotate the netlist to run more accurate simulations.

V. CONCLUSIONS

Hybrid CMOS/Magnetic circuits appear to be good candidates to circumvent the limits of classical CMOS electronics. The hybrid CMOS/magnetic technology is new and therefore is not as mature as CMOS technology. However steady progress are observed in terms of MTJ performances and process variations thanks to all the ongoing R&D effort on MRAM. Since the technology is very similar for MRAM and hybrid CMOS/MTJ non-volatile logic, these progresses will directly benefit to this field. When this hybrid technology is stabilized, characterization results with good statistics will be provided to improve the accuracy of the models and to standardize the tools. Nevertheless, several circuits have already
been fabricated yields very encouraging results. Moreover, the writing schemes based on Spin Transfer Torque or Thermal Assistance are very scalable, since the switching of the magnetic state is driven by the current density. The advantages of mixing MTJs with CMOS devices should become more and more obvious with advanced technologies. Of course, this new technology can be used together with other design techniques to improve the performance of electronic circuits, especially in terms of power consumption. Some research has to be carried out to see how these different techniques can be combined. In particular, some of these techniques are efficient at the full system level. It is then necessary to evaluate the opportunities provided by this technology for complete systems and in comparison or combination with existing techniques and for advanced technologies.

REFERENCES


