A 2-16 GHz CMOS Current Reuse Cascaded Ultra-wideband Low Noise Amplifier

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Abstract—This paper presents the design of a 2-16 GHz ultra wide band low noise amplifier (UWB LNA). The proposed LNA has a gain of 11.5 ± 0.85 dB with NF less than 2.82 dB. Good input and output impedance matching, good isolation and linearity are achieved over the operating frequency band. The proposed UWB LNA consumes 18.14 mW of power from 1.8V supply. This UWB LNA is designed and simulated in 0.18 µm CMOS process.

Keywords—low noise amplifier (LNA), ultra wideband(UWB), Noise Figure (NF).

I. INTRODUCTION

Due to CMOS technology cost effectiveness and compatibility with silicon-based system on-chip (SOC) technology, it can be considered the most prevailing technology for RF integrated circuits (RFIC) implementation [1]. In February 2002, UWB frequency range (3.1 GHz-10.6 GHz) was approved by the Federal Communication Commission (FCC) for commercial application. UWB wireless technology has the capability of transmitting data over a wide spectrum of frequency bands with very low power, high data rates and at very low cost. Imaging systems, sensor networks, ground penetrating radars (GPR) and wireless personal area networks (WPAN) are applications in which UWB wireless technology can be applied. UWB is expected to substitute almost all wired networks with a wireless connection that features hundreds of megabits of data per second [2].

LNA can be considered one of the most important blocks included in the UWB front-end RF receiver. The role of the LNA is to receive and amplify signals over the ultra wide band frequency range. LNA specifications include low and flat noise figure, high and flat power gain, good input and output impedance matching, good reverse isolation and acceptable linearity [1] and [3].

The Common Gate (CG) and Common Source (CS) topologies are two well known different configurations for narrow band LNA design. The common gate low noise amplifier has a good wideband impedance matching, high isolation and good linearity. The CG configuration has also a good noise performance, but it was found that high and flat gain can’t be achieved through single stage common gate amplifier [1], [2] and [4].

In this work, we propose an UWB LNA employing a current reuse cascaded amplifier based on common source stages, followed by a common gate stage. The proposed LNA achieves many advantages due to this configuration. The proposed LNA specifications are high and flat gain, very low noise figure, good input and output impedance matching, high reverse isolation and good linearity.

Recently, current reuse cascaded amplifier has been presented in literature as a suitable configuration for LNA implementation because of its low DC power consumption, high and flat gain, low NF and high reverse isolation [1] and [6]. The current reuse circuit is followed by a CG stage used as a buffer to improve the output impedance matching and flatten the LNA gain.

This paper focuses on the design and simulation results of UWB LNA. It is organized as follows. In Section II, the circuit implementation and the conditions of establishing wide band impedance matching, flat gain and low noise figure are discussed. Section III presents the simulation results, and highlights the benefits of the proposed configuration. Finally, conclusion is drawn in Section IV.

II. CIRCUIT DESCRIPTION

Figure 1. Schematic of the proposed UWB LNA

The schematic of the proposed ultra wide band low noise amplifier is shown in Figure 1 which illustrates that the RF
signal is received through the input port (RF\textsubscript{in}) and forwarded to the first amplifying stage passing through the input impedance matching circuit formed by the gate inductor \(L_{g1}\) and the degeneration inductor \(L_{d2}\). After amplification, the received signal is passed to the gate of the second stage through the capacitive-inductive coupling formed by capacitor \(C_f\) and inductor \(L_{g2}\). Finally, the amplified signal is sent to the source of the common gate buffer and then out to the output port (RF\textsubscript{out}).

To achieve a good input impedance match over the desired bandwidth, wideband impedance matching techniques can be used. A traditional impedance matching technique uses a source degeneration inductor topology as shown in Figure 2 [2]. The input port of the circuit is matched to a desired resistance of value \(R_s\) at a certain resonance frequency \(\omega_r\). The bandwidth of this matching technique depends on the quality factor of the source inductor \(L_s\). The gate inductor \(L_g\) helps defining this resonance frequency where the input impedance of the circuit is given by:

\[
Z_m = j\omega L_s + \frac{1}{j\omega C_{gs}} + \omega_T L_s = j\omega L_s + \frac{1}{j\omega C_{gs}} + R_s. \tag{1}
\]

Where \(Z_m\) is the input impedance of the circuit, \(\omega_T = g_{ds}/C_{gs}\), \(\omega_T\) is the current-gain cut off frequency, \(g_m\) and \(C_{gs}\) are the transconductance and the gate-source capacitance of the input stage \((M_I)\) respectively. \(V_s\) is the RF signal source whose output impedance is \(R_v\).

To achieve a high flattened gain, gate peaking technique can be used [7]. To enhance the high frequency gain of the second stage of the current reuse core, a gain-peaking technique is suggested which helps in achieving a high and flat gain. The used shunt capacitive-resistive feedback technique participates in gain flatness and stabilization of the amplifier. The buffer stage also contributes in gain flatness.

The reduction of noise figure is achieved with the employment of resistive feedback technique. Resitive negative feedback is a technique usually used for desensitization of a circuit and making the gain and input impedance less sensitive to parasitic components, temperature, and process variations [10]. Resistive feedback technique also affects the noise figure of the LNA [8]. It is known that the common problem with the use of resistive feedback in LNAs is that the feedback loop injects thermal noise to the input side, and hence, degrades the NF [10]. The proposed UWB LNA overcomes this problem of noise figure degradation by the implementation of a weak resistive feedback. The optimization of the amplification stages formed by \((M_I, M_2\) and \(M_3\) helps in optimizing the flatness of the noise figure over this bandwidth.

The series resonant circuit consisting of the capacitor \(C_{out}\) and the inductor \(L_{out}\) is playing the role of the output impedance matching circuit. The output port is matched to 50 Ohms which is considered the input impedance of the next stage. The resistive termination formed by the resistor \(R_{out}\) decreases the quality factor of this output resonant circuit extending its matching bandwidth.

III. Simulation Results and Discussion

The proposed UWB LNA is simulated with Agilent Advanced Design System (ADS) using TSMC CMOS 0.18 \(\mu\)m technology. The simulation results are discussed below.

A. Power gain

The power gain represented by \(S_{21}\) achieves 10.65 ~ 12.3 dB over 2 GHz-16 GHz band of frequency as shown in Figure 3. This high and flattened gain is achieved through the current reuse cascaded core. This gain flatness is resultant of the control of the current-gain cut off frequencies \(\omega_{T1} = g_{ds}/C_{gs}\), \(\omega_{T2} = g_{ds}/C_{gs}^2\). It is clear that these values depend on the transconductance \((g_m)\) and gate-source capacitance \((C_{gs})\) of the amplification stages.

B. Noise Figure

In ultra wideband applications, it is required to have a low flattened noise figure in addition to the high and flat gain. Traditional narrow band methods for low noise design are not suitable for wideband design. It is known that the first stage of cascaded matched blocks has the main contribution to the total noise figure [11]. We can conclude that to reduce the noise figure of a cascaded amplifier, it is needed to reduce the noise figure of its first stage.
The value of the NF can be optimized through the optimization of the factors that affect that NF. An equivalent circuit of the first stage which is dominant for noise factor calculation is shown in Figure 4 [1].

![Equivalent Circuit of the first stage for noise calculation](image)

Figure 4. Equivalent Circuit of the first stage for noise calculation [1].

An approximate analysis of the noise figure (\(\text{NF} = 10 \log_{10} f\)) of this topology is given in [1] in which \(f\) is the noise factor of the UWB LNA. The noise factor \(f\) can be given by:

\[
f = 1 + \frac{R_g + R_{ds} + R_{ss} + R_{le}}{R_s} + \frac{\delta \alpha \omega^2 C_{gss}^2 R_s}{5 g_M 1} \\
+ \frac{R_{FB} \left( (L_{g1} + L_s) C_{gss} \right)^2}{R_s \left( g_{M1} R_{FB} - 1 \right)^2} \\
+ \left[ s^2 + s \left( \frac{\omega_{o,rfbn}}{Q_{rfbn}} \right) + \omega_{s,rfbn}^2 \right] \\
\cdot \frac{\gamma g_{M1} (R_{FB} + R_s)^2 \left( (L_{g1} + L_s) C_{gss} \right)^2}{\alpha R_s \left( g_{M1} R_{FB} - 1 \right)^2} \\
+ \left[ s^2 + s \left( \frac{\omega_{o,dn}}{Q_{dn}} \right) + \omega_{s,dn}^2 \right] \\
f \equiv 1 + \frac{R_g + R_{ds} + R_{ss} + R_{le}}{R_s} + f_g + f_{rfbn} + f_{dn}.
\]

Where

\[
\omega_{o,rfbn} = \sqrt{\frac{1 + g_{M1} R_s}{(L_{g1} + L_s) C_{gss}}},
\]

\[
Q_{rfbn} = \frac{1}{R_s + \alpha \omega_{rf} L_s} \cdot \sqrt{\frac{(1 + g_{M1} R_s)(L_{g1} + L_s)}{C_{gss}}},
\]

\[
\omega_{o,dn} = \sqrt{\frac{1}{(L_{g1} + L_s) C_{gss}}},
\]

\[
Q_{rfbn} = \frac{1}{(R_s || R_{FB}) + \alpha \omega_{rd} L_s} \cdot \sqrt{\frac{(L_{g1} + L_s)}{C_{gss}}}.
\]

\(f_g, f_{dn}\) and \(f_{rfbn}\) are gate noise factor, drain noise factor and feedback resistor noise factor respectively. \(\alpha, \delta\) and \(\gamma\) are constants equal to 0.85, 4.1 and 2.21 respectively.

It is noted that to reduce the noise figure we should implement \(L_{ss}\) and \(L_s\) with high quality factor \((Q)\). From equation (2), it is clear that the noise figure is inversely proportional to the feedback resistor \(R_{FB}\). In other words, the noise factor is dependent on the strength of the used feedback technique. Strong feedback increases the noise figure so the reduction of the strength of the resistive feedback decreases the noise figure.

In addition, it is clear that the noise factor is also inversely proportional to the transconductance of the input stage \((g_M)\). This indicates that the noise figure is reduced with the increase of the drain current of the first stage of the amplifier. This reduced noise figure 2.82 ~ 2.14 dB is mainly accomplished through the control of these two parameters. The noise figure of the designed LNA is shown in Figure 5.

![Simulation results for NF](image)

Figure 5. Simulation results for NF.

C. Input impedance matching

The series resonant impedance matching performance can be optimized through the optimization of the inductances of \(L_{ss}\), \(L_{rf}\) and the resistance of the feedback path \(R_{FB}\). The simulation results of the input return loss \(S_{11}\) is shown in Figure 6.

![Simulation results for input return loss](image)

Figure 6. Simulation results for input return loss.
The degeneration inductor and the gain peaking inductor are used to optimize the resonance frequency. The resistive feedback technique is used to widen the impedance matching bandwidth. The input return loss is less than -8.3 dB over the operating bandwidth.

D. output impedance matching

Good output impedance matching is required for good UWB LNA. This objective was achieved through the use of CG buffer stage. A series resonant circuit with a resistive termination is applied for this goal. As shown in Figure 7, the output return loss is less than -8 dB ($S_{22} < -8$ dB) over the operating bandwidth.

E. Reverse Isolation

Unilateral LNA is preferable to prevent power reflection from the output side to the input side. The good isolation features of the common gate contribute to the enhancement of the isolation of our proposed UWB LNA. The LNA reverse isolation factor over this bandwidth is less than -28.7 dB. The simulation results for the reverse isolation $S_{12}$ is shown in Figure 8.

F. Linearity, DC power consumption and Stability

One of the most important challenges in UWB systems is the frequency band allowed for system overlap from other applications. Actually when DC power consumption increases the linearity is improved [12]. So through the enhancement of the transconductance of the amplification stages and the buffer stage, we can improve the LNA linearity. The input referred third order intercept point (IIP3) is calculated to be -7 dBm at mid frequency (9 GHz).

Reduction of DC power consumption is achieved in the design of this UWB LNA through current reuse technique. This LNA operates from a 1.8V power supply and consumes about 18.14 mW. The consumed power is divided between the current reuse cascoded amplifier and the buffer stage. The amplifier core consumes about 10.6 mW and the dissipated power in the buffer stage is about 7.5 mW. The proposed UWB LNA is unconditionally stable over this wide range of frequency.

Table I shows a summary of the designed UWB LNA performance in comparison to other recently published UWB LNA implemented in 0.18 µm CMOS technology.

<table>
<thead>
<tr>
<th>Reference</th>
<th>BW (GHz)</th>
<th>Gain (dB)</th>
<th>Noise Figure (dB)</th>
<th>$S_{11}$ (dB)</th>
<th>$S_{22}$ (dB)</th>
<th>IIP3 (dBm)</th>
<th>Power Consumption (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>This Work (Simulation Results)</td>
<td>2 – 16</td>
<td>11.5 ± 0.8</td>
<td>&lt; 2.8</td>
<td>&lt; -8.3</td>
<td>&lt; -8</td>
<td>-7</td>
<td>18.14</td>
</tr>
<tr>
<td>LNA - 1 [1]</td>
<td>1.7 – 5.9</td>
<td>11.2 ± 2.3</td>
<td>&lt; 4.7</td>
<td>&lt; -11.8</td>
<td>&lt; -12.7</td>
<td>-12</td>
<td>10.34</td>
</tr>
<tr>
<td>LNA - 2 [1]</td>
<td>1.5 – 11.7</td>
<td>12.2 ± 0.6</td>
<td>&lt; 4.8</td>
<td>&lt; -8.6</td>
<td>&lt; -10</td>
<td>-11</td>
<td>10.34</td>
</tr>
<tr>
<td>[2]</td>
<td>3 – 10.6</td>
<td>15</td>
<td>&lt; 4.4</td>
<td>&lt; -7</td>
<td>NA</td>
<td>2.5</td>
<td>21.5</td>
</tr>
<tr>
<td>[3]</td>
<td>1 – 5</td>
<td>12.7 ± 0.2</td>
<td>&lt; 3.5</td>
<td>&lt; -8</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>[5]</td>
<td>0.4 – 10</td>
<td>12.4</td>
<td>&lt; 6.5</td>
<td>&lt; -10</td>
<td>&lt; -10</td>
<td>-6</td>
<td>12</td>
</tr>
<tr>
<td>[6]</td>
<td>3.1 – 10.6</td>
<td>10.8 ± 1.7</td>
<td>&lt; 6</td>
<td>&lt; -10</td>
<td>&lt; -9.3</td>
<td>-9.5</td>
<td>10.13</td>
</tr>
</tbody>
</table>
IV. CONCLUSION

In this paper, an excellent UWB LNA with a minimized noise figure over a wide range of frequency (2 GHz–16 GHz) was presented. The proposed LNA consists of two different cascaded stages. The first stage is a current reuse cascaded amplifier with shunt resistive feedback. This stage uses series resonant impedance matching technique. The second stage is a common gate amplifier with a resistive termination. The LNA is simulated using TSMC CMOS 0.18 µm technology. Simulation results indicate that the proposed UWB LNA achieves high performance. The next step is to implement this UWB LNA to have a comparison between simulation and measured results.

V. REFERENCES