Simplified quantitative stress-induced leakage current (SILC) model for MOS devices

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Abstract

A simplified quantitative model for the steady-state component of stress-induced leakage current (SILC) in MOS capacitors with ultrathin oxide layers has been developed by assuming a two-step inelastic trap-assisted tunneling (ITAT) process as the conduction mechanism. By using our model, we reduced the time of numerical calculations of SILC to 17% of the standard method while maintaining a high accuracy of the results. We also confirmed that the SILC component must not be neglected when calculating the gate current in modern devices, especially at low fields. Our simplified model helped us to investigate the dependence of SILC on the oxide field and the oxide thickness. We also shed some light on the reasons that cause the peak in the SILC–oxide thickness relation.

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1. Introduction

Stress-induced leakage current (SILC) is the increase in the low-level leakage across a thin gate oxide layer after the oxide has been subjected to a high electric-field stress [1]. SILC through the gate dielectric of a MOS transistor causes an additional power consumption which is unwanted especially in low power applications; there it may become a reliability issue in those deep-sub-micron technologies where SILC dominates over the direct-tunneling current [2]. It significantly worsen the retention properties of nonvolatile memory devices like electrically erasable programmable read only memory devices E²PROM and flash memories [3]. SILC consists of two components: steady-state component, which dominates in thin oxides (<8 nm) and transient component that dominates in thick oxides (>13 nm) [4]. In the present work, we consider the first one.

Several models have been proposed as possible mechanisms for SILC. However, it is believed now that inelastic trap assisted tunneling ITAT is the best choice for the conduction mechanisms for SILC [5,6].

The goal of this work is to give a quantitative simplified SILC model not only to explain the field dependence, but also to study the dependence of SILC on oxide thickness ($T_{ox}$).

2. Simplified model

Fig. 1 shows the trajectory of the tunneling electrons, from the cathode to the anode, via traps in SiO₂. Injected electrons travel along a tunneling distance between the cathode and trap sites under the influence of...
the applied electric field. Here, they are captured at the mentioned trap sites and relax to lower available energy states. Finally, trapped electrons enter the anode by a second tunneling step having an energy which is different from that of an elastic tunneling process by the relaxation energy, \( U_{\text{decay}} \).

In this figure, \( q\phi_b \) is the electron barrier height, \( T_{\text{ox}} \) is the oxide thickness, \( x \) is the position of neutral trap sites, \( U_{\text{trap}} \) is the relaxed trap state energy relative to the conduction band edge of the SiO\(_2\), \( Q_{\text{trap}} \) is the trapped charge, \( U_{\text{decay}} \) is the energy difference between the conduction band level of the cathode and the trap state energy \( U_{\text{trap}} \) (the relaxation energy), \( V_{\text{ox1}} \) is the oxide voltage between the cathode and trap sites (first tunneling region) and \( V_{\text{ox2}} \) is the oxide voltage between trap sites and the anode (second tunneling region). From Fig. 1, the trap energy \( U_{\text{trap}} \) is equal to \( q\phi_b + U_{\text{decay}} - qV_{\text{ox1}} \). SILC current density \( J_{\text{SILC}} \) based on ITAT is given by [6]:

\[
J_{\text{SILC}}(E_{\text{ox}}) = \frac{qN_{\text{peak}}}{\tau} \int_0^{T_{\text{ox}}} \exp\left(-\frac{(X - x_0)^2}{\Delta x^2}\right) \times \left(\frac{P_{\text{in}}P_{\text{out}}}{P_{\text{in}} + P_{\text{out}}}\right) dx
\]

where \( E_{\text{ox}} \) is the oxide field, \( q \) is the electronic charge, \( x_0 \) is the center of the distribution, \( \Delta x \) is its width, \( \tau \) is the relaxation time which is defined as the tunneling time from the cathode to the anode at zero oxide thickness, \( P_{\text{in}} \) and \( P_{\text{out}} \) are the probability of electrons to tunnel from the cathode to the trap or from the trap to the anode respectively and \( N_{\text{peak}} \) is the peak value of the Gaussian distribution used to model the trap density. It is given by [1]:

\[
N_{\text{peak}}(E_{\text{stress}}, T_{\text{ox}}) = \begin{cases} 
N_0 \times \exp \left[ - \frac{E_{\text{crit}}}{E_{\text{stress}}(T_{\text{ox}} - X_T) + E_{\text{stress}}} \right], & T_{\text{ox}} - X_T < \lambda \\
N_0 \times \exp \left[ - \frac{E_{\text{crit}}}{E_{\text{stress}}(T_{\text{ox}} - X_T)} \right], & T_{\text{ox}} - X_T > \lambda 
\end{cases}
\]

where \( N_0 \) is a constant, \( X_T = \frac{q\phi_b}{E_{\text{stress}}} \), \( q\phi_b = \text{Si/SiO}_2 \) barrier = 3.1 eV, \( E_{\text{crit}} \) is the energy necessary to create a trap, \( \lambda = 2.3 \text{ eV} \) and \( \lambda \) is the mean free path of electrons in SiO\(_2\) = 15 Å. Numerical integration of Eq. (1) yields the value \( J_{\text{SILC}} \) at a given \( E_{\text{ox}} \).

It is known that one of the merits of a device simulator is in its ability to reduce the time of calculations, especially when iterated solutions are needed. Accordingly, it will be better to simplify the last equation by changing integration to multiplication. So, the model of the most favorable trap position [8] was developed. The authors introduced the most favorable trap position \( x_t \), which gives the largest contribution to the leakage current. They calculated SILC due to traps located at this position by assuming that the value of the trap density is its peak value. Their simplified equation is:

\[
J_{\text{SILC}}(E_{\text{ox}}) = \frac{qN_{\text{peak}}}{\tau} P(E_{\text{ox}}, x_t)
\]

where \( N_1 \) (m\(^{-2}\)) is the area density at the most favorable trap position and \( P(E_{\text{ox}}, x_t) \) is the probability of tunneling at \( x_t \) at a certain oxide field \( E_{\text{ox}} \).

However, we found that this was on the expense of the accuracy and indeed the error introduced is too large as we will prove in the results. Our idea was to keep the privilege of reducing the time of calculation while maintaining a high accuracy for the results. In this regard, we introduced the concept of the equivalent oxide thickness \( T_{\text{ox-equ}} \) over which the spatial Gaussian distribution of traps in the oxide is replaced by its maximum value \( N_{\text{peak}} \) and the total probability \( P_{\text{in}}(x) = \frac{P_{\text{in}}(x)P_{\text{out}}(x)}{P_{\text{in}}(x) + P_{\text{out}}(x)} \) is replaced by its maximum value \( P_{\text{max}} = P_{\text{in}}(x_0) \), where \( P_{\text{in}}(x) \) and \( P_{\text{out}}(x) \) are calculated under the WKB approximation [7]. Note that in the integral of Eq. (1), the contribution of the traps far from the middle of the oxide is very small. This is due to that the total probability becomes smaller as we get far from the center of the oxide. This justifies the use of the peak value of the Gaussian trap distribution. So, for each value of oxide thickness and applied gate voltage, the total probability as a function of position is calculated and hence its maximum value is determined. The next step is to calculate \( T_{\text{ox-equ}} \) by equating the area under the exact curve and

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**Fig. 1.** Energy band diagram of a MOS capacitor, where \( U_{\text{trap}} = q\phi_b + U_{\text{decay}} - qV_{\text{ox1}} \).

**Fig. 2.** Modification of probability \( P_t(x) \) versus position \( x \) from bell-shape to rectangular-shape.
the approximated curve for the tunneling probabilities. The procedure is clarified in Fig. 2. Eq. (1) becomes

\[ J_{\text{SILC}}(E_{\text{ox}}) = \frac{qN_{\text{peak}}}{\tau} \int_{0}^{T_{\text{ox}}} P_1(x) \, dx \]

\[ \int_{0}^{T_{\text{ox}}} P_1(x) \, dx = \text{area under the curve} = P_{\text{max}} T_{\text{ox-eq}} \]

Therefore, Eq. (1) could be rewritten as:

\[ J_{\text{SILC}}(E_{\text{ox}}) = \frac{qN_{\text{peak}}(E_{\text{peak}}, T_{\text{ox}})}{\tau} \times P_{\text{max}}(E_{\text{ox}}, T_{\text{ox}}) \times T_{\text{ox-eq}} \]

So, instead of taking into account only the traps that are located at the most favorable trap position \( x_0 \), we enlarge our view and consider also the traps that are around \( x_0 \) in a thickness \( T_{\text{ox-eq}} \). The approximation now is that the probability of tunneling into all traps inside \( T_{\text{ox-eq}} \) is constant and is equal to the maximum value of the probability over the oxide thickness. So, again the integral in Eq. (1) is replaced by a multiplication. However, our results are much more accurate than those obtained by the most favorable trap model as we will see in the next section. The simplification of Eq. (1) into Eq. (5) permits a clear quantitative explanation of the SILC characteristics as we will see in the next section.

3. Results and discussion

This section contains a comparison between our model and the two other models as applied to MOS capacitors. We investigate the type of traps inside the oxide and the effect of the oxide field and the oxide thickness on \( J_{\text{SILC}} \). Also, the relation between the equivalent oxide thickness and \( E_{\text{ox}} \) is shown. Finally, a comparison between \( J_{\text{SILC}} \) and other current density components across the oxide is presented.

3.1. Proposed model validation

A comparison between the results obtained by Eq. (1), the model based on the most favorable trap position equation (3), and our new proposed model equation (5) is given in Fig. 3. We have used \( x_0 = \frac{L_{\text{ox}}}{2}, \Delta x = 0.7 \text{ nm} \) [1], \( \tau = 10^{-15} \text{ s} \) [8], and \( U_{\text{decay}} = 1.4 \text{ eV} \) [9]. This comparison is given from the point of view of accuracy and time of calculation.

Fig. 3 shows a large error between the results obtained by the most favorable trap position model and the integral formula. This large error in the case of the most favorable trap position model is due to neglecting the effect of all traps unless these are at a position that gives maximum probability. This error was almost eliminated in the new proposed model since we took into ac-
thickness is reduced, with the peak occurring near \( T_{ox} = 3.6 \) nm. This result is quite close to the 4 nm value found in the literature \([6,10]\). The bell shape is due to the two multiplied terms in the new proposed model (Eq. 5). As the oxide thickness decreases, the maximum probability of trap-assisted tunneling \( P_{\text{max}}(E_{ox}, T_{ox}) \) through the oxide increases which initially increases SILC. However, the trap density is constant above a certain oxide thickness which depends on \( E_{\text{stress}} \) and then decreases which reduces the number of sites for such tunneling to occur. Below 3.6 nm, this term dominates and further reduction in the oxide thickness decreases SILC as illustrated in Fig. 6. Hence, the combination of these two factors creates a peak in the \( J_{\text{SILC}} \) versus \( T_{ox} \) characteristics.

From Fig. 7, it is clear that the peak position is independent on the oxide field and depends only on the stress field \( E_{\text{stress}} \). The reason why the position of the maximum current is independent on the oxide field is that the only term in Eq. 5 of \( J_{\text{SILC}} \) which depends on \( E_{ox} \) is \( P_{\text{max}} \). It is reported in Ref. \([8]\) that the position of \( P_{\text{max}} \) is independent on \( E_{ox} \), which verifies our simulation results. And the reason why the position of...
maximum current depends on the stress field is the dependence of $N_{\text{peak}}$ on $E_{\text{stress}}$. Fig. 8 shows that when increasing $E_{\text{stress}}$, the position at which $N_{\text{peak}}$ begins to decrease will shift to smaller oxide thicknesses which decreases the value of the position of maximum current as seen in Fig. 7.

### 3.4. Equivalent oxide thickness $T_{\text{ox-eq}}$

We calculated $T_{\text{ox-eq}}$ (as explained before) with different values of oxide field as shown in Fig. 9. We note that $T_{\text{ox-eq}}$ varies slowly and has an average value of 0.34 nm.

A quite close result was obtained by the group in Ref. [9], but by another approach.

### 3.5. Comparison between $J_{\text{SILC}}$ and the normal tunneling current densities

The gate current density consists of two components, the normal tunneling current density (Fowler–Nordheim $J_{\text{FN}}$ or direct-tunneling $J_{\text{DT}}$ depending on oxide thickness of gate oxide) and the component due to $J_{\text{SILC}}$.
Fig. 10 shows the comparison between $J_{FN}$ and $J_{SILC}$, while Fig. 11 is between $J_{DT}$ and $J_{SILC}$. In the expressions for $J_{FN}$ and $J_{DT}$ [9], we have taken the Si–SiO$_2$ interface energy barrier for electrons = 3.1 eV. On the other hand, $J_{SILC}$ is calculated assuming a stress field of 11 MV/cm and $N_{peak} = 3 \times 10^9$ cm$^{-3}$ for $T_{ox} = 7$ nm in the comparison with $J_{FN}$. The value of $N_{peak}$ is taken $= 5 \times 10^8$ cm$^{-3}$ for $T_{ox} = 3.5$ nm in the comparison with $J_{DT}$. The difference in the values of $N_{peak}$ is due to the difference of oxide thicknesses, as shown in Fig. 6. Figs. 10 and 11 show that $J_{SILC}$ is the dominant one at low oxide voltages. It is worthy to mention that in MOS-transistor simulators, the gate current is either considered equal to zero or the fresh component ($J_{FN}$ or $J_{DT}$) is the only one taken into consideration. Our study suggested that $J_{SILC}$ may be larger than the fresh component, at least at low fields. Consequently, it cannot be neglected.

4. Conclusion

In our work, we have developed a simplified mathematical model for the steady-state component of SILC. We reduced the time of calculation to 17% while keeping higher accuracy. By using our model we clarified the reasons which cause the peak in $J_{SILC}$–$T_{ox}$ relation. We shed some light why that this peak is independent on oxide field $E_{ox}$ and depends only on the stress field. We found that $J_{SILC}$ is greater than the fresh component $J_{fresh}$ at low fields. Consequently, $J_{SILC}$ cannot be neglected and must be taken into account when calculating the gate current in modern simulators. Under development now is the application of our model in the calculation of SILC in MOSFETs.

References